INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

2023 UPDATE

METROLOGY

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METROLOGY

1. INTRODUCTION

The Metrology Chapter identifies emerging measurement challenges from devices, systems, and integration of new materials in the semiconductor industry and describes research and development pathways for meeting them. This includes but not limited to, measurement needs for extending CMOS, accelerating beyond CMOS technologies, novel communication devices, sensors, and transducers, materials characterization, and structure-function relationships. This also includes advances in metrology required for research and development, and process control in manufacturing environments[1-6].

With device scaling nodes projected to decrease below 5 nanometers, specifically to 2 nanometers [7] within the next 2 years, geometric scaling is expected to soon reach its physical limits or get to a point where cost and reliability issues far outweigh the benefits. Moreover, the physical scaling may no longer be the main technology driver for the industry going forward: applications such as internet of things (IoT), cyber-physical systems, autonomous vehicles, cloud computing and big data, green energy, and medical and health technologies among others are expected to influence the design and manufacturing approaches[8]. The use of complex 3D structures fabricated using new materials and processes with ever-decreasing dimensions is also projected to accelerate within the next few years[9] [10].

The metrology roadmap addresses some of the measurement science challenges caused by these new developments and aims to provide a long-term view of the challenges, potential solutions, technology, tools, and infrastructure needed to characterize new devices and materials for process control, and manufacturability. Since metrology solutions are preferably developed well in advance of when a specific technology goes into production, the information outlined in this chapter could serve as a guide for metrologists, equipment manufacturers, and researchers. It can also serve as input for standards organizations to develop solutions for key measurement challenges where the adoption of a standard or benchmark would help advance the technology.

1.1. CURRENT STATE OF TECHNOLOGY

Device and integrated circuit (IC) technology has rapidly evolved toward the use of complex 3D device structures frequently using new materials, patterning techniques, and processes that provide higher device performance with smaller feature sizes. The 3D nanoscale nature of these structures provides considerable challenges for all areas of metrology. The following examples of new process technology will help to illustrate the new challenges facing metrology. New patterning processes such as the use of extreme ultra-violet (EUV) lithography, multi-patterning, nanoimprint, and directed self-assembly (DSA) of block copolymers, among, all result in different challenges for measurement of critical dimensions (CD), overlay, defectivity, and material properties[6, 11]. Specifically, EUV (EUVL), and high NA-EUV, lithography induces stochastic variations and defects in patterned resist films as a new key metrology problem[12]. Overlay, with its continually shrinking budget, remains a constraint in increasing device yield.

The current dominant microprocessor device architecture is based on FinFET technology, but is transitioning to the nanosheets-based FET, such as gate-all-around, etc., with feature size below 3 nm [13]. The challenges associated with the 3D nature of the measurements in these architectures are amplified by shrinking dimensions[14]. The challenges facing front-end processes (FEP) metrology is control of the fabrication processes for memory structures that are among the most complex 3D device architectures such as 3D NAND flash memory, where the aspect ratio could be as large as 100:1. On-chip and off-chip interconnect materials continue to evolve, and interconnect metrology challenges continue to include process control for 3D interconnect. The metrology challenges emerging materials include characterization of 2D van-der Waals layers such as graphene and [15-17], as well as electrical characterization at the nano-scale[18, 19].

Metrology enables manufacturing process development, control, and improvement; processing tool improvements; ramping in pilot lines and factory start-ups; and improvement of yield in high-volume manufacturing factories. Metrology can reduce the cost of manufacturing, and the time-to-market for new products through better characterization of process tools and processes. The increasing diversity of semiconductor chip types will stretch thin the already limited metrology resources over a wider range of challenges. The metrology community, including manufacturing tool and material suppliers, chip manufacturers, consortia, and research institutions, must provide

cooperative research, development, and prototyping environments to meet the roadmap timeline. The lack of certainty in the structures and materials of future technology generations makes the definition of specifics for future metrology less clear today than in the past. Moreover, different materials may be used by different manufacturers at the same or similar technology generation, potentially requiring different metrologies. Metrology methods must routinely measure near- and atomic-scale dimensions, require a thorough understanding of nano-scale material properties and of the physics involved in making the measurement. Metrology development must be done in the context of these issues.

Measurement of relevant properties, such as stress or strain, in a nanoscale buried area such as GAA transistor channels or Si/SiGe multilayers is challenging[20, 21]. Often, one must measure a film property at the surface and then use modeling to determine the resultant property of a buried layer. Long-term needs at the sub-5 nm technology generation are difficult to address due to the lack of clarity of device design and interconnect technology. Although materials characterization and some existing in-line metrology apply to new device and interconnect structures, the development of manufacturing capable metrology requires more certain knowledge of materials, devices, and interconnect structures [2].

Metrology tool development requires early access to new materials and structures with a clear and deep understanding of measurement or inspection requirements for it to be successful. It requires state-of-the-art capabilities to be made available for fabrication of necessary standards and development of metrology methodologies in advance of mass production. The pace of feature size reduction and the introduction of new materials and structures challenge existing measurement capability. In some instances, existing methods can be extended for several technology generations[22]. In other cases, necessary measurements may be approximated with inadequate equipment. Long-term research into nanometer-scale devices may provide both new measurement methods and potential test vehicles for metrology. A greater attention to expanding close ties between metrology development and process development is needed. Increased integration of materials, processes, and measurement models with metrology data could help address some of the problems. In addition, newer and less expensive nanofabrication methods would require cheaper metrology solutions in order to be cost-effective [23]. An appropriate combination of well-engineered tools, modeling, and appropriate metrology is necessary to maximize productivity while maintaining an acceptable cost of ownership.

1.2. Drivers and Technology Targets

The new developments (new drivers and complex 3D structures) have implications for metrology with respect to the pace and timing by which new technologies are adopted. One of the main differences between the new drivers and scaling is that they are mostly top-down, in contrast to “bottom-up.” These new drivers are already reshaping the semiconductor technology market and by extension semiconductor technology roadmapping activities. The importance of cloud computing, AI technology such as deep learning, and their respective ecosystems, means that areas such as heterogeneous integration, security, and outside system connectivity are more important than ever. Although these drivers are important, currently, no single driver seems to have the preeminence of scaling. For example, the worldwide pandemic that started in 2020 has revamped demand in areas such as personal computing and accelerated the already robust growth of cloud computing.

At the same time, feature size, shape, and interface complexity will continue to play a major role in the timeline for metrology solutions. The introduction of different structures and processes such as gate all around (GAA)-nanowire/ nanosheet (NW/NS)/nanofork,[1] monolithic 3D heterogeneous integration using channel materials such as Si, SiGe, Ge/Si, III-V, GaN, and 2D materials, will not only increase the overall complexity of the measurement but will also redefine what measurand needs to be measured and at what juncture. Although scaling effects are usually presented with respect to transistor density and device performance, the same fundamental physical limits that affect device characteristics also affect the resolution and sensitivity of available metrology [3]. As such, feature sizes (and feature size variations) will always be a key driver for improvements in semiconductor metrology technology.

1.3. Vision of Future Technology

The variety of structures, materials, and processes that will likely be used in the next 15 years would be much more than the industry has used in any 15-year period. To complicate matters, different integrated circuit (IC) manufacturers may adopt technologies that would require different metrology solutions. The sheer difficulty of measuring certain parameters with the needed levels of precision could redefine what measurements are considered critical and at what stage they need to be measured.

Research is far along for the use of 2D materials and carbon nanomaterials, such as, MoS_2, graphene, and carbon nanotubes (CNT), [12-14] [24] in both-,- and back-end processes[10]. The use of such could lead materials will lead to next-generation atomically thin transistors, where the scaling limitations of current Si technology will be

traversed[15-17]. Recent examples include MoS_2 vertical transistor with sub-1-nm channel [25], and processing methods that yield low defect density [26]. Progress continues to be made in "fab" processing and integration of CNT field-effect transistors[27-29].

Beyond, and perhaps overlapping with, this 15-year roadmap period will be the insertion and implementation of a wide range of beyond-CMOS devices including tunneling, ferroelectric, and spintronic devices, spin- FETs, spin-torque oscillators[30-32]; heterogeneously integrated photonic devices; and new types of quantum-engineered field effect transistors[33]. Other computing approaches such as neuromorphic computing could employ structures with smaller than CMOS-based device dimensions. A crossbar-based memristor with a 6 nm half-pitch and 2 nm critical dimensions was recently demonstrated[34]. However, due to the large investment, knowledge base, and relatively high yields of current silicon processing technology, most new technologies will likely co-exist with CMOS-based technology. This means that future metrology solutions must accommodate a wider variety of technologies.

In the long term, the development of new computing models such as quantum, adiabatic, and neuromorphic, among others, will drive future metrology technology. Research on quantum-based computing, which requires the careful control of quantum effects (superposition, entanglement, and interference) to solve a complex set of problems, is progressing. A recent report shows the use of a 53-qubit processor to sample the output of a random quantum circuit[35], a task that would have taken a supercomputer years to perform. Although it is not clear what the overall metrology challenges will be, research on single-atom Si-based qubit devices shows that metrology will be indispensable in enabling the fabrication and precise positioning of well-defined, reproducible qubits, and control of their energy exchange[36, 37].

Based on current and projected trends, modeling and simulation, big data analytics and virtual metrology (VM) among others will continue to play a bigger role going forward and will also be integrated into all aspects of metrology. Understanding the interaction between metrology data and information, optimum feedback, feed-forward, and real-time process control are key to restructuring the relationship between metrology and process technology (i.e., digital twins[38]). Additionally, accurate model-based simulation is becoming important in the design and optimization of various measurements to make sure that the proper type and number of measurements are carried out within the required confidence in the results, and to avoid too many measurements (*loss of time and money*) or too few measurements (*loss of control*). As modeling and simulation resulted in spectacular advancement in crafting ICs, modeling and simulation in metrology will also bring similar rewards[39]. For example, due to the small number of atoms comprising the smallest features crafted (a 1 nm diameter Si sphere is made of 26 atoms), their signals generated are inherently small and therefore difficult and expensive to measure due to quantum and stochastic effects, among others. Thus, it is imperative to develop and use fully optimized measurement methods that provide the needed information only. For example, sparse (compressed) sensing or sampling is a newly developing powerful method, which can be applied to semiconductor production metrology and that can help to get the necessary information in the most economical way [40]. As such, the need to measure only what is needed is a reoccurring theme throughout this report.

The use of hybrid or combined metrology techniques would also increase. With respect to the number of measurands and the technology needed, it is clear that no one technique would be able to deliver the solutions needed for process control. Overall, better use of the large amount of process and metrology information that is already collected, as well as implementation of VM techniques would help metrologists acquire just the right amount of data.

International cooperation in the development of new metrology technology and standards will be required. Both metrology and process research and development organizations must work together with the industry including both the supplier and IC manufacturer. Earlier cooperation between IC manufacturers and metrology suppliers will provide technology roadmaps that maximize the effectiveness of measurement equipment. Research institutes focusing on metrology, and standards; standards organizations; metrology tool suppliers, and the academic community should continue to cooperate on standardization and improvement of methods and production of reference materials. Despite the existence of standardized definitions and procedures for metrics, individualized implementation of metrics such as measurement precision to tolerance (P/T) ratio is typical. The P/T ratio is used to evaluate automated measurement capability for use in statistical process control and relates the measurement variation (precision) of the metrology cluster to the product specification limits. Determination of measurement tool variations is sometimes carried out using reference materials that are not representative of the product or process of interest. Thus, the measurement tool precision information may not reflect measurement-tool-induced variations on product wafers. It is also possible that the sensitivity of the instrument could be insufficient to detect small but unacceptable process variations. There is a

need for metrics that accurately describe the resolution capability of metrology tools for use in statistical process control. The inverse of the measurement precision-to-process variability is sometimes called the signal-to-noise ratio or the discrimination ratio. However, because the type of resolution depends on the process, specific metrics may be required (e.g., thickness and width require spatial resolution while levels of metallic contaminants on the surface require atomic percent resolution). There is a new need for a standardized approach to the determination of precision when the metrology tool provides discrete instead of continuous data. This situation occurs, for example, when significant differences are smaller than the instrument resolution.

Although not directly under the purview of metrology, hardware and data security [41, 42] are now issues that affect all aspects of semiconductor process technology [43]. Key application drivers such as IoT not only have vulnerabilities that could be exploited by bad actors, but the sheer volume of components on the market opens opportunities for counterfeits. Although it is not clear how broad a role metrology would play, verifying the accuracy of specific design elements implemented to enhance hardware security could be one. An example is using the tuning, nonlinear conductance, reconfigurability, and variability properties of memristors[44] to create digital keys and fingerprints, where the encryption keys are derived from physical variations created during device fabrication [45].

Wafer manufacturers, process tool suppliers, pilot lines, and factory start-ups all have different timing and measurement requirements. The need for a shorter ramp-up time for pilot lines means that the characterization of tools and processes prior to pilot line startup must improve. However, as the process matures, the need for metrology should decrease. As device dimensions shrink, the challenge for physical metrology will be to keep pace with in-line electrical testing that provides critical electrical performance data.

2. SCOPE OF REPORT

The scope includes metrology for critical dimensions (CDs), microscopy, lithography metrology, front-end processes metrology, on-chip interconnect metrology, 3D interconnect metrology, materials characterization, metrology for emerging research materials and devices, reference materials, and outside systems connectivity needs and challenges.

As shown by the scope of the chapter, the breadth and depth of information and expertise needed to adequately address IC metrology issues are quite large. As such, some of the underlying information on instrumentation, characterization, device structure and physics, and process steps may not always make it into the chapter or in some cases are not suitable for a roadmap publication. Publications and conferences that focus on IC metrology provide some of this background information, e.g., *Metrology and Diagnostic Techniques for Nanoelectronics* (Zhiyong Ma and David G. Seiler eds.) [46] covers recent advances in research and industry practices on IC and nanoelectronics metrology, and is a good reference for a wide range of topics covered by the chapter.

Several conferences and associated proceedings are important sources for researchers in different areas of metrology for nanoelectronics and IC manufacturing. The Frontiers of Characterization and Metrology for Nanoelectronics (FCMN), the SPIE Advanced Lithography conferences, The Lithography Workshop, the IEEE International Electron Devices Meeting, the Electron, Ion, and Photon Beam Technology and Nanofabrication Conference, Advanced Semiconductor Manufacturing Conferences, and the VLSI Technology Symposium among others, are key venues for new research and development on nanoelectronics and nanoscale manufacturing/fabrication metrology. Papers and presentations from the FCMN (and predecessor conferences) covering more than 15 years are available [47]. Other sources of information include *SPIE's Journal of Micro/Nanopatterning, Materials, and Metrology (JM^3), Nature Electronics*, *IEEE Transactions on Semiconductor Manufacturing, IEEE Transactions on Electron Devices,* and *IEEE Electron Device Letters.* The National Institute of Standards and Technology (NIST) recently published a series of workshop reports on the needs of the industry that highlight the technical and investment needs required to support a robust semiconductor manufacturing sector [48, 49]. The listed sources and chapter references are by no means exhaustive, but they are good places to start.

In addition, the Metrology Focus Team (FT) will occasionally publish *White Papers* on IC metrology topics that are complementary to the roadmap. For example, the *IRDS Virtual Metrology Whitepaper*[50] developed by the Metrology and Factory Integration FTs several years ago is an example. The executive summary of that white paper has been updated and presented in the section on factory-level metrology.

3. SUMMARY AND KEY POINTS

This chapter presents the long- and near-term difficult metrology challenges. These challenges revolve around the impact of new drivers, device structure complexity, new materials, and the statistical limits of controlling sub-5-nm stochastic processes. A short section on metrology requirements for outside systems connectivity (OSC) is included. Also included is a section on virtual metrology requirements, its role, a summary of issues, and what needs to be done for wider adoption.

Reoccurring themes throughout the report include: 1) the influence of advanced data analytics; 2) the need for hybrid or combined metrology, and 3) the impact of new device architectures and new starting materials. These issues, which have been present in the roadmap over the years, take on a new urgency as market drivers shift. They are also outlined in the key messages below:

1. Device structure and new materials complexities are as important as feature size as key drivers of metrology needs and challenges.
2. Hybrid or combined metrology will play a bigger role moving forward. No single instrument has the capability or resolution needed to measure the large number of parameters and measurands needed to characterize some of the new device structures.
3. The use of advanced data analytics will span all areas of metrology including image and data analysis, inference, integration with modeling and simulation, prediction, and correlation with other process steps. Although this already happens in some form or the other, current methods, which involve autonomous or semi-autonomous evaluation of data to learn patterns, obtain key insights, and make decisions, could fundamentally change how metrology is currently performed in the factory.

4. CHALLENGES

Metrology requirements continue to be driven by advances in lithographic and multi-patterning processes, new materials, and beyond CMOS materials, new device architectures, and switching devices. EUVL has become a dominant patterning technology and is driving the development of new metrology equipment for masks, and research into metrology techniques for EUV resist. As the use of EUVL gains momentum, the presence of EUVL-induced stochastic variations and defects means that the sensitivity and resolution of metrology tools would need to improve. However, this will only be part of the solution. In addition to finding ways to mitigate stochastic effects, improvements in models that relate EUVL patterning parameters to stochastic variations are needed. Such models assist metrologists in developing suitable measurement methods and strategies for EUVL-induced defects and variations.

Existing CD metrology is approaching its limits and requires significant advances to keep pace with the needs of patterning. Another key challenge to CD metrology is tool matching. Near-term precision (measurement uncertainty) requirements for the next few years can be met using single tools. Overlay metrology capability lags the need for improved overlay control, especially for multi-patterning applications.

> The rise of 3D NAND technology has greatly stretched the capability of current metrology. Multilayered stacked structures of 3D NAND (with hundreds of layers) present unique challenges with respect to vertical gate control, CD channel/memory hole, defect control, stress, and material characterization, among others.

Front-end processes continue to drive metrology to provide measurements for new channel materials including SiGe/Si and III-V film stacks, higher dielectric constant materials, dual work function metal gates, and new ultra-shallow junction doping processes. 3D device structures, such as GAA, 3D NAND, and 3D dynamic random-access memory (3D DRAM), place significantly more difficult requirements on dimensional and doping metrology. For example, fins evolve into nanowires, nanosheets[51, 52], nanoribbons, or nanorods at future nodes[53]. 3D interconnect metrology requirements are largely driven by the activity in through silicon vias (TSV) R&D. Several solutions for bonded wafer overlay are now available. For beyond CMOS R&D, many areas of 2D materials metrology have advanced [10], but putting them into volume manufacturing will require challenging R&D. For example, the need for understanding large-area graphene uniformity is driving both physical and electrical metrology.

4.1. NEAR-TERM AND LONG-TERM CHALLENGES

To achieve desired device scaling, metrology tools must be capable of measuring properties on atomic distances. This includes inline metrology for dimensional, compositional, and doping measurements. Thus, many short-term (2022 to

2029) metrology challenges listed in Table MET-1 will continue beyond the 5 nm half pitch. Metrology needs are increasingly affected by the natural stochastic variation limits of the printing process, and by new structures, materials, and processes. These include nanosheets, SiGe, and stacking technologies such as 3D, wafer-to-wafer (W2W), and die-to-wafer (D2W). Shrinking feature sizes, tighter control of device electrical parameters (such as threshold voltage and leakage current) and new interconnect technology (such as 3D interconnect) will provide the main challenges for physical metrology methods. The increased use of multi-patterning techniques introduces the need to independently solve a large set of metrics to fully characterize a multi-patterning process[54]. Table MET-1 presents ten major challenges for IC metrology.

Table MET-1 Metrology Difficult Challenges

Near-Term Challenges: 2022 -2029	*Summary of Issues*
Control of new process technology and 3D interconnects.	• 3D device structures, such as GAA nanosheet and fork sheet transistors require an increased need for in-line metrology for dimensional, compositional, and doping measurements. Multi-patterning techniques introduce the need to independently solve a large set of metrics to fully characterize a multi-patterning process. • Multilayered stacked structures such as 3D NAND present unique challenges with respect to vertical gate control, CD channel/memory hole, defect control, stress, material characterization, and the high aspect ratio nature of the stacked memory cells, among others.
Statistical limits of sub-5 nm process control	• Controlling processes where the natural stochastic variation limits metrology will be difficult. Printed features are now small enough that random variations in the amount and position of molecules can now create small variations in pattern fidelity that have substantial effects on device performance.
Measurement of complex material stacks and interfacial properties.	• Capability for SOI, III-V, GeOI wafers needs enhancement. CD and film thickness are impacted by thin SOI optical properties and charging by electron and ion beams. • Reference materials and standard measurement methodology for complex material stacks and interfacial properties including physical and electrical properties are needed. • Optical measurement of gate and capacitor dielectric involves averaging over too large an area and needs to characterize interfacial layers.
Measurement of complex material stacks and interfacial properties.	• Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure a correlation between measurements in the scribe line and on-chip properties. Standards institutions need rapid access to state-of-the-art development and manufacturing capability to fabricate relevant reference materials.
Metrology needs for 3D multi-chip integration (3D chip stacking)	• Metrology is needed for 3D multi-chip (memory, chiplet, or tile) integration technologies for higher density scaling of transistors using techniques such as TSV, embedded silicon bridge, 3D chip stacking using multiple-sized micro solder bump, and hybrid bonding. • Some applications need interconnect access from the wafer backside, which needs TSVs to connect devices and power supply sources outside the chips. The backside power distribution network (BS-PDN) process requires new concepts of metrology over FEOL, BEOL, and A&P.
Long-Term Challenges: *2030 - 2037*	*Summary of Issues*
Nondestructive wafer and mask-level metrology for 3D structures.	• Nondestructive, production-worthy wafer and mask-level metrology for CD measurement for 3D structures, overlay, defect detection, and analysis. • Potential metrology solutions need to be able to characterize complex shape structures with sub-atomic resolution (without surface charging

	and contamination). These include vertical gate all-around (VGAA) nanowire, lateral gate all-around (LGAA) nanowire, and monolithic or sequential 3D FETs.
Lab to Fab Metrology Strategy	• Correlation of test structure variations with in-die properties is becoming more difficult as devices shrink. Sampling plan optimization is key to solving these issues. Techniques must provide mapping across the chip and across wafer variation.
Metrology for sub-3 nm multiple patterning EUVL, high-NA EUVL	• Controlling processes where the natural stochastic variation limits metrology will be difficult. Printed features are now small enough that random variations in the amount and position of molecules can now create small variations in pattern fidelity that have substantial effects on device performance. Examples include EUV resist-induced surface, sidewall, and edge roughness, and stochastic effects.
Structural and elemental analysis	• Materials characterization and metrology methods are needed to control interfaces, dopant placement, defect density, and elemental concentration relative to device dimensions. Measurements of self-assembling processes are also required.
Metrology needs for 3D device integration and 2D channel materials	• 3D integration technologies for transistor-level 3D structures are in the R&D phase toward mature process integration. Metrology for the characterization of subsurface structures (dimensional and compositional measurements) is needed. • Metrology for integration of proposed structures such as ferroelectric-FET (e.g., FeFET or NCFET) and memristors for neuromorphic applications. Metrology for CFET (monolithic/sequential), and photonic chip integration. • Metrology for 2D channel material: atomic defect characterization and monitoring (vacancies, substitutions and ad-atoms, grain boundaries, dislocations, strain, local variation of the band structure, and contamination, among others), and potential/carrier distribution.

5. TECHNOLOGY REQUIREMENTS

5.1. SUMMARY

This section gives a summary of the technology requirements over the next 15 years, and by extension the types of device structures and materials that would need to be measured. Table MET-2 shows a subset of the More Moore – Logic Core device technology roadmap for select years between 2022 and 2037. Gate all around (GAA) are structures where the gate material completely wraps around the device, which in this case is made up of nanowires. In a lateral configuration, they are referred to as lateral-gate-all-around (LGAA). This configuration would not only use the same layout as FinFET, but they are also visually like FinFETs with multiple nanowires where the fins would have been. In the vertical congratulation, known as vertical gate-all-round (VGAA), the gate length is vertical with respect to the source and the drain.

5.2. TECHNOLOGY TRENDS AND EVOLUTION

As device structures evolve from FinFETs to GAA-based on nanowires, and to monolithic 3D devices, the metrology needed to evaluate these devices would need to contend with smaller target volumes and larger backgrounds leading to low signal-to-noise ratios[3, 6, 55]. In addition, the channel materials would evolve from Si to Ge and 2D materials over the same period. The combination of new structures and materials, smaller targets, and larger backgrounds amongst other constrains would require metrology techniques with the resolution, depth of focus, and appropriate energy levels to non-destructively measure all the needed parameters.

For memory devices, techniques capable of measuring very high aspect ratio structures made from multiple and disparate material stacks are needed for DRAM and 3D NAND flash memory. Parameters include vertical gate control, CD channel/memory hole, defect control, stress, and material characterization, among others.

This includes not just the resolution, but the range and the material sensitivity needed for high aspect ratio (HAR) features made of tens to hundreds of layers. In addition to the broader shape and materials issues, the ability to characterize specific parameters (such as height, and sidewall angle) for different aspects of FinFETs and GAA devices is driving the technology requirements[4]. Table MET-2 shows the logic device structure requirements from the IRDS More Moore focus team for the years 2022 to 2037. The table (based on 2022 IRDS More Moore information) has projections of when devices from different technologies will be produced and some of the requirements needed for implementation.

*Table MET-2 Logic Device Structure Requirements**

YEAR OF PRODUCTION	2022	2025	2028	2031	2034	2037
	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4	G38M16/T6
Logic industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET LGAA	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM	LGAA-3D CFET-SRAM
Platform device for logic	finFET	LGAA	LGAA CFET-SRAM	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D	LGAA-3D CFET-SRAM-3D
LOGIC TECHNOLOGY ANCHORS						
Device technology inflection	Taller fin	LGAA	CFET-SRAM	Low-Temp Device	Low-Temp Device	Low-Temp Device
Patterning technology inflection for Mx interconnect	193i, EUV DP	193i, EUV DP	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV
Beyond-CMOS as complimentary to platform CMOS	-	-	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET
Channel material technology inflection	SiGe50%	SiGe60%	SiGe70%	SiGe70%, Ge	2D Mat	2D Mat
Local interconnect inflection	Self-Aligned Vias	Backside Rail	Backside Rail	Tier-to-tier Via	Tier-to-tier Via	Tier-to-tier Via
Process technology inflection	Channel, RMG	Lateral/AtomicEtch	P-over-N N-over-P	3DVLSI	3DVLSI	3DVLSI
Stacking generation inflection	3D-stacking, Mem-on-Logic	3D-stacking, Mem-on-Logic	3D-stacking, CFET, Mem-on-Logic	3D-stacking, CFET, 3DVLSI	3D-stacking, CFET, 3DVLSI	3D-stacking, CFET, 3DVLSI

*Note: Information from 2022 IRDS More Moore Table MM-8

5.3. MICROSCOPY

Microscopy is used in most of the core technology processes where 2D distributions, which are digital images of the shape and appearance of IC features, reveal important information. Usually, imaging is the first, but many times is the only step in the "being able to see it, measure it, and control it" chain. Microscopes typically employ light, electron beam, X-ray, or scanning probe methods. Beyond imaging, online microscopy applications include CD and overlay measurements along with detection, review, and automatic classification of defects and particles. Because of the high value and quantity of wafers, the need for rapid, non-destructive, in-line imaging and measurement is growing. Due to the changing aspect ratios of IC features (besides the traditional lateral feature size (for example, linewidth measurement)), full 3D shape measurements are important. New metrology methods that take full advantage of advanced digital image processing and analysis techniques, and networked measurement tools are now used to meet the requirements of IC technologies but require continual improvements as the problems get more complex. Microscopy techniques and measurements based on these methods must serve the technologists better, giving fast, detailed, and adequate information on the processes in ways that help to establish better process control. Although improvements in the underlaying imaging or spectroscopic techniques are necessary, equally important is the ability to develop methods that apply current capabilities to new problems.

Electron Microscopy—There are different microscopy methods that use electron beams as sources of illumination[39]. These include scanning electron microscopy (SEM), transmission electron microscopy (TEM), scanning transmission electron microscopy (STEM), and low-energy and high-energy electron microscopy. Scanning electron microscopy is discussed below, and transmission electron microscopy, scanning transmission electron microscopy, and low-energy electron microscopy are discussed in the sections on *Materials Characterization* and *3D Nanometrology Needs and Challenges*.

Scanning Electron Microscopy (SEM)—continues to provide at-line and in-line imaging for characterization of cross-sectional samples, particle, and defect analysis, in-line defect imaging (defect review), and CD measurements. Improvements are needed for effective CD and defect review (and SEM detection in pilot lines) at or beyond the 5 nm generation[56]. Studies are underway to quantify suitable imaging parameters for ultra-thin resist required for high-

NA EUV[57]. New in-line SEM technology, such as the use of ultra-low-energy electron beams (<250 eV) and high-energy SEM (typically 10 keV–200 keV, but in some cases as low as 5 keV) may be required for overcoming image degradation due to charging and radiation damage of the sample surface while maintaining adequate resolution and depth of field. Improving the resolution of the SEM by the reduction of spherical aberration leads to an unacceptably small depth of field, and thus SEM imaging with several focus steps and/or the use of algorithms that take the beam shape into account might be needed. Aberration correction lens technology has migrated from TEM to SEM providing a significant increase in capability. There are effective methods to eliminate instrument-origin contamination, so only sample-origin contamination might remain an issue. Suitable management of atomic-level surface cleanliness is now necessary and with further research is becoming possible. Super-low, <200 eV landing energy high-resolution imaging is now possible, it should be explored for CD measurements, especially for targets consisting of shrinkable materials such as photoresists[58]. A new alternative path could be high-pressure or environmental microscopy, which opens the possibility for higher accelerating voltage, improved resolution imaging, and metrology. Binary and phase-shifting chromium-on-quartz optical photomasks have been successfully investigated with this mode of high-resolution SEM. It has been found that the gaseous sample environment minimizes sample charging and contamination. This methodology also holds promise for the inspection, imaging, and metrology of wafers.

It is becoming increasingly important to develop measurand-based, optimized, non-raster scanning capability for the SEMs to acquire raw size, shape, and composition information. Due to the small signals generated by the small number of atoms comprising the devices under test (*and even fewer atoms that represent their variations)*, and for throughput reasons, significantly better measurement results can be obtained by scanning the primary electron beam only over those locations that contain the required information. This will minimize sample damage while substantially increasing time-to-results. Like light-based measurements, electron beams with optimized "illumination" and the generated signals are becoming indispensable for imaging and measurements of atomic-scale devices and structures. The physics of electron-sample interaction must be understood and taken advantage of, in selecting appropriate measurement parameters. This can be accomplished by fast and accurate simulation with so-called computational-SEM (CSEM). Reliable material proprieties (such as n and k values, secondary electron yields, etc.) must be determined for atomic level 2D (layer-) and 3D structures as these are not yet satisfactorily known for relevant samples. SEM manufacturers should provide more, detailed information about the SEM column and its detectors, allowing modeling and optimization of the measurement process. 3D beam parameters, incidence angle (stray tilt) detector energy, trajectory sensitivity acceptance angle, and other parameters should be provided to the users to allow better optimization.

Data analysis methods that adhere to the physics of the measurement and use all information collected have been demonstrated to be better than arbitrary methods. Measured and modeled images and fast and accurate comparative techniques are likely to gain importance in SEM dimensional metrology. A better understanding of the relationship between the physical object and the waveform analyzed by the instrument is expected to improve CD measurement. Sample damage, which arises from direct ionization damage of the sample and deposition of charge in device structures, may set fundamental limits on the utility of all microscopies relying on charged particle beams. Shrinkage, another form of damage often caused by electron beams on polymer layers (including photoresists), is now better understood and in many cases can now be predicted and compensated for in CD measurement values[58].

Model-based SEM measurements can deliver useful 2D contour and 3D profile information on 10 nm and smaller IC structures with resolution approaching that of TEM[59-61]. The combination of aberration-corrected lens, low-energy SEM columns, and model-based-library analysis methods can also provide a significant boost to critical dimension SEM (CD-SEM) measurement capabilities, and allow for better 3D information from top-down 2D images[62]. Further efforts are needed to implement strategies that use multiple images taken from different angles [63] to determine the 3D shape of the various IC structures, including embedded sample features as the smallest structures are partially transparent under electron beam irradiation. Research on the use of multiple SEM columns[64-66] and the use of detected backscattered electrons from multiple primary beam energies to reconstruct the 3D structure of features[67] are progressing. The SEM is useful for determining the 3D shape and size of both individual and large number (average) of features and is much faster than TEM investigations. The inline use and nondestructive nature of top-down SEM makes it useful for a wide range of applications, therefore it is important to explore and develop optimized, sound physics-based measurement methods.

Determination of the real 3D shape for smaller contacts/vias, transistor gates, interconnect lines, or damascene trenches will require continuing advances in existing microscopy and sample preparation methods. Fully automated cross-sectioning by focused ion beam (FIB) and semi-automated lift-out for imaging in a TEM or a STEM has been successfully demonstrated[68]. Solutions for imaging bottoms of HAR vias and trenches have been demonstrated using higher energy SEMs and low-loss backscattering electron detection modes. High-energy SEM with energies >10 keV

offers potential solutions for the improved resolution needed for in-line CD-SEM roles at the upcoming nodes, although such beams cause known local electrical damage at the measurement site. However, such tools have recently been commercially introduced and are starting to gain acceptance for some roles, especially for HAR via measurement and CD-SEM-based overlay for some applications[4, 56]. As the increase of 3D NAND flash memory, in-line SEM is now applied to measure the channel/memory holes, especially for the bottom hole CDs by using a highly accelerated primary electron beam. Given that dual beam FIB[69] is now commonly used in-line and improved resolution CD-SEM is a critical need, use of high-energy SEM in-line on non-electrically active targets, such as scatterometry gratings, kerf features, dedicated SEM features, or even sacrificial die, are now reconsidered in the industry[6, 55].

Scanning Probe Microscopy (SPM)—may be used to calibrate CD-SEM measurements. Scanning probe microscopies, such as the atomic force microscope (AFM), offer 3D measurements that are insensitive to the material scanned. Flexing of the probe degrades measurements when the probe is too slender. The probe shape and aspect ratio must, therefore, be appropriate for the probe material used and the forces encountered. High-stiffness probe materials, such as short carbon nano-tubes, may alleviate this problem. In addition to size, another limit to the use of AFMs for dense features is profile fidelity at feature bottoms (semi-enclosed area) where the tip is exposed to forces from multiple directions. Other types of scanning probe microscopy are discussed in the sections for *Emerging Research Materials and Devices* and *3D Nanometrology Needs and Challenges*.

Far-field Optical Microscopy—is limited in resolution by the wavelength of light. Deep ultraviolet sources and near-field microscopy are being developed to overcome these limitations. Improved software allowing automatic classification of sub-wavelength-size defects is needed[70]. Traditional optical imaging will continue to have applications in the inspection of large features, such as solder bump arrays for multi-chip modules. Also, other new experimental optical applications that move beyond direct measurement from images have the potential to detect smaller features either for measurements or other aspects of process control. More work is needed to understand if they have a place for inline metrology[71, 72]. Optical methods that determine the geometry of features $1/30^{th}$ of the wavelength of light by addressing limitations in the measurement and normalization of the complex set of amplitude, phase, and spatial frequency propagation errors have been reported[73], and could be applied to a variety of industry-relevant samples.

For *Defect Detection*—each technology has limitations. A defect is defined as any physical, electrical, or parametric deviation capable of affecting yield. Existing SEMs and SPMs are considered too slow for the efficient detection of defects too small for optical microscopes, and existing optical techniques lose some sensitivity to defects smaller than 20 nm[74]. High-speed scanning has been demonstrated with both arrayed and single-probe SPMs [75] (that might be faster than SEMs) but issues associated with probe lifetime, uniformity, characterization, and wear need to be addressed. This technology should be pursued both by expanding the size of the array and in developing additional operational modes. However, the expected speed improvements are substantial—some implementations have experimentally demonstrated single-probe scan speeds as fast as a few micrometer^2 image in under 5 seconds[76]. Arrayed micro-column SEMs have been proposed as a method of improving SEM throughput[65] and the operation of a single micro-SEM has been demonstrated. Research is needed into the limits of electrostatic and magnetic lens designs. An optical method that uses volumetric analysis to process focus-resolved images of defects as small as 16 nm has been demonstrated[77]. The effects of wavelength scaling on defects as small as 8 nm have been simulated[78-80]. Another optical method, through-focus scanning optical microscopy (TSOM), demonstrated the detection of sub-20 nm defects using a visible wavelength of 546 nm. Simulations show the potential to detect defects as small as 5 nm using 250 nm wavelength. TSOM also shows promise for patterned defect detection and classification[81],and sub-surface defect detection using near-infrared microscopy[82].

In addition to the techniques outlined above, surface analysis techniques such as scanning Auger nanoprobe (complementary to scanning electron microscopy/energy dispersive X-ray spectroscopy (EDS) or TEM/EDS) offer surface-sensitive elemental quantification from tens of nanometers to micron scales. X-ray photoelectron spectroscopy (XPS) and Angle-resolved photoemission spectroscopy (ARPES) techniques are used for diagnostic measurements of novel materials (2D and epitaxial channel materials for example) and help process optimization and control. Applications range from surface chemical composition to metrology of key quantities related to electronic/structural properties such as work function, hole effective mass, and in-plane lattice parameter. This information could be correlated with in-plane X-ray diffraction (XRD) or electrical measurements. Overall, these techniques address both the optimization of large-scale material deposition parameters and the engineering of device fabrication processes.

Defect Detection is more extensively discussed in the Yield Enhancement chapter.

5.4. LITHOGRAPHY METROLOGY

Lithography metrology continues to be challenged by the rapid advancement of patterning technology. New materials in all process areas add to the challenges faced by lithography metrology. The advent of EUVL poses major challenges to lithography process control, because EUVL employs a broad range of other lithography components including mask, resist, and scanner, among others, each of which needs to be qualified for a wide range of applications. EUVL is also being implemented at extremely small device sizes (where feature variability is on the order of a few atoms), with complex structures and a host of new materials (*see Table MET-2*). These factors contribute to a range of process control challenges, such as the introduction of stochastic effects such as line edge roughness, line width roughness, local critical dimension uniformity, and printing failures[83-85]. These challenges will greatly challenge available metrology; thus, both fundamentally new measurement approaches, as well as novel application of existing capabilities are needed.

Proper control of the variation in transistor gate length starts with mask metrology. Although the overall features on a mask are four times larger than as printed, phase shift and optical proximity correction features are roughly half the size of the printed structures. Indeed, larger values for mask error factor (MEF) might require a tighter process control at the mask level, too; hence, a more accurate and precise metrology must be developed. Mask metrology includes measurements that determine that the phase of the light is correctly printed. Both on-wafer measurement of CD and overlay are also becoming more challenging. CD control for transistor gate length continues to be a critical part of manufacturing ICs with increasing device performance measures such as clock speeds. The metrology needs for process control and dispositioning of product continue to drive improvements in measurement uncertainty. The acceleration of research and development activities for CD and overlay measurements is essential to providing viable metrology for future technology generations. All of these issues require improved methods for evaluation of measurement capability.

On-product monitors of effective dose and focus extend the utility of conventional microscopy-based CD metrology systems in process control applications. The same system can output CD and overlay measurements, as well as lithography process monitors. Process control capability and efficiency of such metrology are improving. The infrastructure to support such new applications is generally available. Monitors of effective dose and focus for lithography process control have also been developed for conventional optical metrology systems, such as those used in overlay metrology. Similar capabilities, in addition to CD, sidewall, and height metrology, are now emerging in scatterometry. In all cases, rather than measure CD for process control, with every feature's CD being a complex function of both dose and focus, these systems output measurements of process parameters themselves, with metrology errors as low as 1% (3 σ) for dose and ~10 nm (3 σ) for focus. Current process monitors performance levels boast P/T = 0.1 for the lithography process window, with 15% for dose and 200 nm for focus, enabling further reduction of k_1 in high-volume manufacturing and extending the utility of optical microlithography. While the demands on metrology systems' stability and matching are likely to increase, work in this area has already initiated the development of tighter control and matching, being a pre-requisite of accurate CD metrology, not just of process control applications and dedicated process monitors. As device sizes shrink, there is also a move to specify displacement deviations such as CD, overlay, and line edge roughness as a composite value represented by the edge placement errors (EPE). EPE provides some flexibility in allocating the individual error components while maintaining the overall error budget[86].

Capable and efficient direct process monitor-based lithography process control has the potential to overcome the technology limitations of conventional CD metrology. Solutions to the ongoing change of lithography process control methodology can be accelerated by industry collaboration to define the expectations in direct process control, with tests of performance and standards for both new metrology applications and applications environment. This change will, likely, result in lithography metrology where capable and efficient means of process control are supplemented by and are differentiated from, superior CD metrology proper. New levels of absolute accuracy are required to meet measurement requirements for next-generation technology, especially in the areas of CD metrology for calibration and verification of compliance for advanced mask designs (for example, 1D and 2D/3D CD metrology through pitch and layouts, in the presence of optical proximity correction (OPC) and resolution enhancement technology, at various printing conditions).

Often, dedicated metrology test structures instead of active device are measured devices during manufacturing. In such cases, CD-SEM continues to be used for wafer and mask[87] measurement of lines and via/contact. A considerable effort has been aimed at overcoming electron beam damage to photoresist used by 193 nm exposures and that will continue when alternative lithography techniques, like EUVL, are introduced[88] as discussed above in the microscopy section, these efforts are starting to yield real results. Stack materials, surface condition, line shape,

and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects, unless they are accurately modeled and corrected, increase measurement variation and total uncertainty of CD-SEM measurements. Developments in electron beam source technology that improve resolution and precision are being tested. CD-SEM is facing an issue with poor depth of field unless a new approach to SEM-based CD measurement is found. High-voltage CD-SEM and low-loss electron detectors have been proposed as means of extending the use of the CD-SEM.

It is essential to collect the right kind and amount of information to be able to make statistically sound SEM measurements[89]. The collection of excess information leads to loss of throughput, and on the contrary, the collection of insufficient or the wrong type of information leads to loss of process control. It is important to develop metrology methods that reveal and express the needed information with the indication of the validity of the measurements. Larger usable image field-of-view at image resolution-level pixel density allows for much greater utilization of multiple feature measurement (MFM) applications for increased information per unit time, and thus improved validity of measurement results, through increased sampling without throughput penalty. It is indispensable to employ custom scanning methods to acquire and measure only the information sought in the shortest possible time. Techniques that leverage automated analysis of SEM images by a deep-learning (artificial intelligence) procedure based on convolutional neural networks (CNNs) [90] may also help optimize the data collection- throughput conundrum.

For CD-SEMs, design-based metrology (DBM) applications, which include automatic recipe setup from design information, allow for the practical use of SEMs for large-scale verification of design intent, through the collection of feature 2D contour[91] shape information and comparison to GDS files. DBM applications are becoming very important for the development and verification of lithographic OPC, as the number of measurements for successfully developing OPC is expected to grow exponentially with technology generation. Also, DBM applications for multiple patterning are being explored. This is a major role where metrology interfaces with the design for manufacturing (DFM) community. Also, collecting and applying CD information from reticle measurements for comparison to wafer CD measurements is an important application in some cases, and would be most efficient if done through contours.

However, much work remains to be done in defining contour error source testing methodologies, contour reference metrology, and SEM modeling for contours. Model-based metrology—again—could help solve these problems[92]. Contour fidelity is a prevailing challenge where improvements in the state of the art could yield incremental value to the industry[93, 94]. Gaps or missing segments in contours can occur for reasons related to both the sample and the metrology tool. Major contributors are weak signal and breaks along edges parallel to the (fast) scan axis and contrast variation along the contour, which could be due to underlying variations in the structure (e.g., changes in sidewall angle or reentrance) or instrumental artifacts, such as edge proximity effects in a SEM[95]. In some cases, breaks in the contour are inherent when referencing one level to another (e.g., poly over active area). This subject of contour integrity is closely related to the accuracy of contour extraction. Contour extraction algorithms employ 2D image processing and thus function differently than conventional single-measurand CD extraction algorithms, which are applied to individual line scans. There are known significant differences specifically with regard to edge detection and the inherent degree of signal averaging. Model-based measurement methods can alleviate these problems. Sampling can also have a large impact, as averaging as few as five contours can significantly improve precision and, due to averaging out local roughness effects in discrete features, also improve agreement between extracted contours and simulation.

Attention must also be paid to the requirements for registration between the SEM contours and the design for successful OPC[91]. Models must be able to compensate for rotational and lateral offsets between the SEM contour and the design, as well as for potential field distortions. This relates somewhat to the question of metrology accuracy versus production accuracy; the extent to which it is acceptable to remove metrology errors when matching contours to the design is not agreed upon. For example, a uniform magnification error removed by stretching the contour could be less problematic than non-linearity across the SEM field of view.

Another area in which useful improvements could be made in contour metrology accuracy in the statistical sophistication of the contour extraction and modeling software, for example, the inclusion of a 95% confidence interval for the extracted contour. A machine-learning -based method for contour extraction of SEM images has been demonstrated [96]. It should be noted that the final metrics in measuring contours should be compatible with the same conventional linewidth metrics used in this roadmap.

Scatterometry—Routinely provides line shape metrology and statistically valid average values for large numbers of features. Scatterometry refers to both multi-wavelength—single angle optical scattering and to single wavelength—multi-angle methods. Recent advances have resulted in the ability to determine CD and line shape without the aid of a

library of simulated results. For in-line applications, scatterometry provides a tighter distribution of key transistor electrical properties when used for advanced process control. Scatterometry is now used for contact and via structures[97] and for more complex features[98, 99] where as many as 10 parameters are modeled. Work on EUV-based sources continues and could extend the capabilities of scatterometry to material properties, interfacial properties, and roughness[100-102]. Other methods, such as interferometric-based scatterometry, have been proposed and could be applied to both front and back-end applications [103].

Scatterometry models typically assume uniform optical properties of line and background materials, although surface anomalies and non-uniform dopant distribution may affect scatterometry results. Scatterometry models are often calibrated with periodic verification using reference metrology such as SEM and critical dimension AFM (CD-AFM)[84, 104, 105]. Lithography and etch micro-loading effects may noticeably affect line CD. Since scatterometry currently makes measurements on special test structures, other CD metrology techniques (such as SEM, AFM, or TEM) may be employed to establish a correlation between CD and the shape of the scatterometry structure and CDs of the circuit. As in most aspects of IC metrology, the use of machine learning and other semi-autonomous data analytics techniques in scatterometry continues to increase[106-108] and could help reduce the dimensionality of the modeling data. Current development is pushing scatterometry target size to enable the measurement of smaller test structures while improving measurement precision[109-112]. The usage of multiple patterning steps creates complexity when measuring multi-patterned features, as more parameters must be measured and controlled, including statistically distinct CD, sidewall, roughness, and pitch (overlay) populations. In some schemes, an antireflective coating (ARC) may prevent the UV light from penetrating deeper layers. Recent efforts are focused on applying scatterometry to overlay[113] metrology including a new class of image-based[114] scatterometry capable of multi-layer measurements. Implementations using Mueller-matrix-based scatterometry[115] have applications in DSA[116, 117], for shape metrology with improved sensitivity to contour asymmetries and pitch walking [118, 119], and selective etching of multi-nanosheet FET for sub-5 nm nodes[120], among others. As feature density continues to decrease, quantum confinement effects may yield dimensionally dependent shifts in the optical properties. All of these issues could contribute to the main challenges of achieving successful scatterometry metrology on a given process: Parameter cross-correlations when modeling complex features[6], although multi-tool inspection using hybrid metrology may mitigate this challenge[121, 122]. Optical scattering techniques could still be useful for sub-5 nm metrology, however a good understanding of materials, interfaces, geometries, resulting uncertainties, advanced test structures, and increased use of hybrid metrology would be needed[123, 124].

Small angle X-ray scattering (SAXS)—is an analytical technique that is routinely used to measure structural features on the order of 1–100 nm with the potential for measuring complex periodic nanostructures such as FinFETs and 3D NAND cells. The method is similar to optical scatterometry, but at a much smaller wavelength and with the scattering contrast proportional to changes in the electron density instead of the electronic structure. SAXS can measure CD, height, pitch, multiple patterning errors, line edge roughness, and average cross-sectional profile of both logic and memory structures[125-127]. There are two main types of SAXS techniques, transmission-based SAXS, commonly called critical dimension SAXS (CD-SAXS), and grazing incidence SAXS (GI-SAXS).

In transmission-based SAXS (T-SAXS) or CD-SAXS, a high energy (i.e., greater than 15 KeV) X-ray beam is passed through a semiconductor wafer and scattered from a periodic nanostructure. The scattered intensity is measured on an area detector. The wafer is then tilted through a series of different incidence angles to determine the angular dependence of the scattering pattern. Transmission through the 750 μm silicon wafer requires X-ray energies greater than 15 keV to minimize absorption loss. The path length through the structure is typically on the order of 100 nm, so multiple scattering events are and the Born approximation is valid. The intensity of the scattered radiation measured by the detector is proportional to the square of the Fourier transform of the electron density distribution, making CD-SAXS sensitive to changes in both the atomic number and the mass density. The signal is strongest for samples with large changes in electron density and weakest for low atomic number films such as carbon-based photoresist. The signal also depends on the square of the height of the structure, so tall samples such as HAR memory[128] scatter orders of magnitude stronger than logic structures. CD-SAXS modeling is considerably less computationally demanding than the rigorous coupled-wave analysis (RCWA) used in optical scatterometry enabling real-time regression rather than the use of pre-computed libraries. Simple shape models are usually based on stacks of trapezoids [129] and complex shapes have been successfully modeled using more sophisticated models using volumetric meshing approaches.

Most reported demonstrations of CD-SAXS for logic applications have utilized large synchrotron facilities for the X-ray source. Laboratory-based CD-SAXS can be used for reference metrology, but in-line metrology for logic applications will require significant improvements in compact X-ray sources to get the required throughput (<1 min) with a small spot size (<100 μm). High throughput CD-SAXS measurements are demanding for X-ray sources because

they require both a small spot and a small divergence (less than the angular spacing between scattering peaks, e.g., <1 mrad). This is because the only way to reduce both the spot size and the divergence for a given source is to aperture the beam and consequently reduce the flux. Current X-ray sources do not have a high enough X-ray brilliance to enable high throughput in-line metrology for logic application [130]. Future X-ray sources need to be developed with at least 100 × increases in brightness over current commercial lab sources. One possible solution is the use of inverse Compton scattering X-ray sources[131-134] in which a high-energy electron beam is used to scatter optical photons and up-convert them into the hard X-ray regime. Very tall structures such as 3D-NAND and DRAM scatter much stronger and CD-SAXS has the required throughput for characterization of HAR contact holes and commercially available in-line tools have recently been introduced to the fab [128, 135, 136].

Since CD-SAXS is a transmission through wafer measurement, it works best on the front end as all current periodic structures in the stack will contribute to the scattering pattern. Orthogonal structures such as gates and fins scatter in different orientations and thus will not interfere with each other. Modeling more complex stacks will require prior knowledge of the previous structures in the stack. The small absorbance of the high energy X-rays and the short path length results in a small absorbed dose in the characterized structures. Research is needed to see if shrinkage or other forms of damage occur in photoresists at these X-ray doses.

In GI-SAXS[137-139], the X-ray beam is incident on the wafer close to the critical angle of total external reflection and the sample is rotated azimuthally to produce an angle-resolved data set. In addition, the grazing angle can be tuned to probe either the surface structure or at different depths into the structure. The grazing angle is typically a few tenths of a degree and results in a very large projected spot on the sample in the beam propagation direction (~cm's). The much larger spot size on the sample compared to CD-SAXS and signal enhancements related to the grazing geometry result in measurement times much shorter than transmission CD-SAXS. GI-SAXS has been used to determine the size distribution of nanoparticles in thin films, the average diameter of nanowires, and the CD, pitch, sidewall angle, and height of simple silicon gratings[140]. Reflection and refraction at the surface and thin film interfaces must be incorporated into the data modeling such as is done in the distorted wave Born approximation (DWBA). The long path length of the X-ray beam through the highly periodic structure in grazing incidence geometry results in multiple scattering events that also need to be considered in the data models. This is not done using conventional DWBA theory, and modeling improvements are needed for robust quantitative analysis of more complicated structures representative of those found in modern logic devices. High throughput GI-SAXS measurements have been conducted on memory structures where the large spot size and restrictions on complex shape models are less of a problem[141].

GI-SAXS can use much lower X-ray energies than transmission CD-SAXS since substrate absorption is not a concern. The lower X-ray energies are advantageous because the critical angle of total external reflection is higher, resulting in a smaller projected spot size on the sample. Additionally, the scattering angles of the diffraction peaks and the angular spacing between the peaks is larger, so the divergence requirements are relaxed in the scattering direction (e.g., >1 mrad).

In other areas, the use of "feed-forward" control concepts must be extended to lithography metrology taking data at least from resist and mask pattern measurements and controlling subsequent processing, such as etching, to improve product performance. "Feedback" controlling strategy is required as well to set proper process parameter setup from a huge amount of previously collected data.

CD-AFM measurements can be used to verify line shape and calibrate CD or contour measurements. New probe tip technology and a 3D tilt-able scan heads [142] may be required if CD-AFM is to be applied to dense line measurements below 15 nm. Focus–Exposure correlation studies (especially for contact/via) can be used by all of the above methods as well as by the dual column focused ion beam (FIB) (SEM plus focused ion beam) where there is an immediate correlation with line shape. Electron holography has been proposed as a long-term CD measurement technology.

Although non-planar devices such as FinFETs are now the standard CMOS device architecture, they still pose metrology challenges. These challenges will only increase as fins evolve into nanowires or nanosheets. 3D NAND flash memories will continue to increase in aspect ratios and through hundreds of different material layers. The possibility of DSA lithography raises potential metrology problems, depending on whether the metrology is done before or after the removal of the sacrificial component. In addition, complex periodicities resulting from multi-patterning, low signal-to-noise ratio from smaller dimensions, and an increased number of process control variables from multiple locations on the feature present additional challenges. Thus, true 3D metrology with increased sensitivity is required. Figure MET-1 gives a summary of the capabilities of different imaging and spectroscopic metrology techniques [55]. (See section "3D Nanometrology needs and Challenges").

	<--Imaging Techniques			Spectroscopic Techniques-->			
Application	LV CD-SEM	HV-SEM / LLBSE-SEM/ E-SEM	CD-AFM	OCD	T-SAXS	GI-SAXS	MBIR
2D/3D Litho apps	7/5 * shrinkage, need profile	severe shrinkage	10 dns <5/3 iso	7/5 * thin PR, smallCD n&k	≤ 5/3	≤ 5/3	
2D Planar Etch & MP apps	7/5 * need profile	Impractical	10 dns <5/3 iso	7/5 * smallCD n&k complex periodicities	≤ 5/3	≤ 5/3	
2D+ Multi-layer planar etch apps	7/5 * need profile	5 * need profile	10 dns <5/3 iso	7/5 * smallCD n&k	≤ 5/3	≤ 5/3	
3D FinFET, Nanowire & Nanosheets	7/5 * need profile	Impractical	10 dns <5/3 iso	7/5 * smallCD n&k	≤ 5/3	≤ 5/3	
3D HAR apps	7/5 * need profile	5 * need profile	No tip access to HAR	7/5 * smallCD n&k, large depth limit?	≤ 5/3	Beam samples ≤400nm depth	10 * no depth limit
See-thru apps	No signal from depths	5 *	modulus AFM needs study	7/5 * smallCD n&k, large depth limit?	≤ 5/3	Beam samples ≤400nm depth	10 * no depth limit

Color Key: ≤5 nm limit; 5 nm limit; 7 nm limit; 10 nm limit; not possible; unknown

*All values are in nanometers; LLBSE, low-loss backscattered electrons; MBIR, model based infra-red; HV, high voltage; E-SEM, environmental SEM; *There are significant gaps for this technique for some metrics within this application group.*

Figure MET1 Metrology Capabilities and Gap Analysis[1]

5.4.1. LINE-EDGE ROUGHNESS/LINEWIDTH ROUGHNESS

Line edge roughness (LER) and line width roughness (LWR) are important parts of lithography and etch process control. The Lithography Roadmap provides metrics for both LER and LWR. Stochastic variations that lead to roughness can have a wide range of impacts on the yield, reliability, and performance of devices. Until recently, LER and LWR were determined using a SEMI Standards definition[143], however, this standard is being currently updated by the SEMI Standards Committee. The main addition to this new standard will be the difference between biased and unbiased roughness measurement. It is important to note that the precision requirements for LER and LWR are several years ahead of those required for CD as indicated below.

LER/LWR is evaluated by two methods: spectral analysis and measurement of LER/LWR amplitude/degree (generally, 3σ of residuals from an average position or average CD). Although amplitude parameters (such as 3σ) are still the most useful index for practical in-line metrology, to fully describe roughness, the power spectrum should include a roll-off exponent and autocorrelation parameter[144-146]. In evaluating LER/LWR, the length of the inspected edge, L, sampling interval of edge-detection, Δy, and noise removal are all important. Spectral analysis, for example, using the power spectral density (PSD), allows analysis of the roughness frequency components, which gives the user important information related to device performance. These frequency ranges can also be related to local CD uniformity and local edge placement errors (EPE)[147].

Another important factor in the measurement of LWR/LER on imaging tools is edge detection noise. This noise has the effect of adding a positive bias to any roughness measurement. This is shown by the equation $LWR_{meas}^2 = LWR_{actual}^2 + \sigma_\varepsilon^2$ where LWR_{meas} is the measured value, LWR_{actual} is the actual (unbiased) roughness of the target, and σ_ε^2 is the noise term, defined as the reproducibility of locating an edge along one single sampling point. LWR_{meas} is the biased roughness because it contains σ_ε^2 The size of σ_ε^2 is in the range of 0.5 nm — 2 nm, which means that this measurement artifact in some cases could mask the actual roughness to be measured depending on technology generation. A methodology has been demonstrated to remove this noise term, leading to an unbiased estimation of the roughness. Use of this is deemed very important to ensure the accuracy of roughness measurement in the future and should be a key ingredient in allowing for inter-comparison of data across the litho-metrology community. It should be noted that LWR metrology becomes more challenging when the resolution of the metrology tool becomes close to the LWR requirement. LER/LWR metrology would greatly benefit from improved imaging resolution by CD-SEMs and other instruments. Due to the process-dependent origins of edge and pattern roughness, and the advent of EUVL and its

[1] *Based on information from: [5] B. Bunday, N. Orji, and J. Allgair, "High volume manufacturing metrology needs at and beyond the 5 nm node," in Proc. SPIE, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2584555. [Online]. Available: https://doi.org/10.1117/12.2584555*

associated stochastic effects, standards and evaluation methods for LWR and LER remain an area of active research[47, 146, 148-158].

5.4.2. MEASUREMENT UNCERTAINTY

Critical dimension measurement capability does not meet uncertainty requirements that include measurement variation from individual tool reproducibility, tool-to-tool matching, and sample-to-sample measurement bias variation. Reproducibility includes repeatability, variation from reloading the wafer, and long-term drift. In practice, reproducibility is determined by repeated measurements on the same sample and target over an extended period.

There is no single metrology method or technique that can deliver all the needed information. Therefore, to compare the results of various dimensional metrology tools and methods meaningfully, parameters beyond repeatability and precision need to be addressed. Each measurement application requires consideration of the need for relative accuracy (sensitivity to CD variation and insensitivity to secondary characteristic variation), absolute accuracy (traceability to absolute length scale), LER and sampling, and the destructive nature of the measurement.

Although the precision requirements for CD measurement in the roadmap have always included the effects of line shape and material variation, repeated measurements on the same sample would never detect measurement uncertainty related to sample-to-sample bias variation. Therefore, with the current methodology, the measurement uncertainty associated with variation of line shape, material, layout, or any other parameters will not be included in the precision. Typically, reference materials for CD process control are specially selected optimum or "golden" wafers from each process level. Thus, industry practice is to define measurement precision as the reproducibility of the measurement for each process level. The measurement bias is not detected by this approach, as it misses the bias variation component of measurement uncertainty. In light of this, a metric, total measurement uncertainty (TMU) can be used. The TMU is determined using a technologically representative set of samples that accounts for variations in measurement bias associated with each process level. This idea can be extended to use with a production fleet of tools through another metric fleet matching precision (FMP). These metrics assume accuracy for all tools, and that a fleet of tools behave as well as a single tool would be required. It should be noted that other metrics for accuracy and matching are also available.

It would be ideal to have all metrology tools properly characterized for measurement uncertainty including a breakout of the leading contributors to this uncertainty. It is recommended to use internationally accepted methods to state measurement uncertainty. This knowledge would help to make the most of all metrology tools, and it would prevent situations in which the measured results do not provide the required information. Finally, once the largest contributors to measurement errors are known, a faster development of better instruments could take place. It is now recommended to state the measurement uncertainty of various dimensional metrology tools according to internationally accepted methods and to identify (quantify) the leading contributors[159]. Another possibility is the combination of information from multiple metrology techniques into "hybrid metrology", where separate, different dimensional metrology tools not only are calibrated together but can either communicate with each other to share extra information to improve each other's uncertainties and rectify inter-variable correlations[160]. (See more information in the "Combined Metrology" section.)

Calibration of in-line CD metrology equipment requires careful implementation of the calibration measurement equipment referred to as reference metrology. For example, laboratory-based TEM or CD-AFM[161, 162] must have a precision that matches or exceeds in-line CD and have to be frequently calibrated. Reference materials used during manufacturing must be representative of the actual process level and structure and reflect the pertinent process variations to be evaluated by the tool under test. Reports of this approach already exist.

CD measurement has been extended to line shape control. Tilt beam CD-SEM, comparison of line scan intensity variation versus line scans from a golden wafer, scatterometry, CD-AFM, dual beam (electron and Gallium ion beam systems), and triple beam (electron, Gallium ion beam, and Argon ion beam systems) have all been applied to line shape measurement. The sidewall angle has been proposed as the key process variable. Already, photoresist lines have shapes that are not well described by a single planar description of the sidewall. Line edge and line width roughness along a line, vertical line edge roughness, and rounded top shapes are important considerations in process control. As mentioned above, precision values change with each process level. This adds to the difficulty in determining etch bias (the difference in CD before and after etch). Electrical CD measurements provide monitoring of gate and interconnect line width, but only after the point where reworking the wafers is no longer possible and does not allow a real-time correction of process parameters. Electric CD measurements are limited in their applicability to conducting samples.

Mask metrology is moving beyond the present optical technology. Binary and phase-shifting chromium on quartz optical photomasks have been successfully investigated with high-pressure/environmental SEM. Environmental SEM instrumentation equipped with high-resolution, high-signal, field emission technology in conjunction with large chamber and sample transfer capabilities is in use in the semiconductor industry for mask CD. The high-pressure SEM methodology employs a gaseous environment to help compensate for the charge build-up that occurs under irradiation with the electron beam. Although potentially very desirable for charge neutralization, this methodology has not been seriously employed in photomask or wafer metrology until now. This is a new application of this technology to this area, and it shows great promise in the inspection, imaging, and metrology of photomasks in a charge-free operational mode. This methodology also holds the potential for similar implications for wafer metrology. For accurate metrology, high-pressure SEM methodology also affords a path that minimizes, if not eliminates, the need for charge modeling.

Lithography metrology consists not only of overlay and CD metrology, but also includes the process control and characterization of materials needed for the lithography process, especially photoresists, phase shifters, and ARCs. As these lithography materials become more complex, the materials characterization associated with them also increases in difficulty. Additionally, most non-lithography materials used in the wafer fabrication process (gate oxides, metals, low-κ dielectrics, SOI substrates) enter the lithography process indirectly, since their optical properties affect the reflection of light at a given wavelength. Even a small variation in process conditions for a layer not normally considered critical to the lithography process (such as the thickness of the buried oxide in SOI wafers) can change the dimensions or shapes of the printed feature if this process change affects the optical response of the layer.

As a minimum, the complex refractive index (refractive index n and extinction coefficient κ) of all layers needs to be known at the lithography wavelength. Literature data for such properties are usually not available or obsolete and not reliable (derived from obsolete reflectance measurements on materials of unknown quality followed by the Kramers-Kronig transform). In ideal cases, n and κ can be measured in-line using spectroscopic ellipsometry at the exposure wavelength. Especially below 193 nm, such measurements are very difficult and usually performed outside of the fab by engineering personnel. EUV optical properties can only be determined using specialized light sources (such as a synchrotron or an EUV source for an EUV lithography tool). Therefore, materials composition is often used as a figure of merit, when direct measurement of the optical properties is not practical. But even two materials with the same composition can have different optical properties (take amorphous and crystalline Si as an example).

Additional complications in the determination of the optical properties of a material arise from surface roughness, interfacial layers, birefringence, optical anisotropy (often seen in photoresists or other organic layers responding to stress), or depth-dependent composition. For some materials for a wafer fab, it is impossible to determine the optical properties of such material, since the inverse problem of fitting the optical constants from the ellipsometric angles is underdetermined. Therefore, physical materials characterization must accompany the determination of optical properties, since physical characteristics, materials properties, and optical constants are all interrelated.

Overlay measurements are challenged by phase shift masks (PSM) and OPC masks, and the use of different exposure tools and/or techniques for different process layers will compound the difficulty as varied EPE often result. Future overlay metrology requirements, along with problems caused by low contrast levels, will drive the development of new optical or SEM methods along with SPM[163]. The need for new target structures has been suggested as a means of overcoming the issues associated with phase shift mask, OPC alignment, and edge placement errors not detectable with traditional targets. Overlay for on-chip interconnect will continue to be challenging. The use of chemical mechanical polishing for planarization degrades target structures. Thus, as requirements for tighter overlay control are introduced, the line edge of overlay targets in interconnect are roughened. The low-κ materials used as insulators will continue to make overlay more difficult.

Furthermore, meeting the very tight overlay budget driven by advanced applications in DRAM and NVM, calls for a flexibility of overlay metrology setups, faster implementation of alternative measuring solutions, like high-voltage SEM and scatterometry techniques, and also means that overlay metrology will continue to be an active research[163-180]. Given that overlay error includes contributions from process and non-process-induced sources, measurement errors, and material among others[181], solutions and models that incorporate a broader view of error sources and possible solutions are needed[182, 183]. Special test structures with arrays of lines and arrays of spaces that adequately capture all the anticipated sources of measurement artifacts would also be required.

The Lithography Technology Requirements tables include the specific metrology requirements such as uncertainties. Apart from heading information, items in white indicate that manufacturing solutions exist, and are being optimized. Yellow indicates that manufacturable solutions are known. A mix of yellow and red indicates that interim solutions

are known, and red indicates that manufacturable solutions are not known. A move to a more extreme color in subsequent years without a change in requirement means that the underlying dimension has changed.

5.4.3. EXPLANATION OF UNCERTAINTY IN TABLE MET3

The preceding concepts are summarized by the following consideration for the precision of patterning metrology: the definition of precision critically depends on the application. Given the application and the metrology instrument, a sampling plan needs to be defined. The precision specification needs to be interpreted relative to the application, instrument, and sampling plan. The application defines the accuracy, single tool precision, and matching requirements. In some applications, relative accuracy and single-tool precision are paramount. In some applications, tool matching and single-tool precision are paramount. In some applications, a single measurement event is not sufficient to provide the needed measurement; rather the average of multiple measurement events constitutes the critical measurement episode; in this case, the precision should be interpreted as the uncertainty requirement of the average. The precision numbers in the tables are changed to uncertainty numbers. The relation to precision and uncertainty (σ) is given in formula (1).

$$\sigma^2 = \sigma_P^2 + \sigma_M^2 + \sigma_S^2 + \sigma_{other}^2 \quad (1)$$

Uncertainty (σ) contains the following components: σ_P (Precision), σ_M (Matching), σ_S (Sample variation) and σ_{other} (inaccuracy and other effects). We assume normal distributions where each factor is independent and only random variations occur[159].

Table MET-3 Lithography Metrology (Wafer) Technology Requirements

Figure MET2 Lithography Metrology Potential Solutions

5.5. FRONT END PROCESSES METROLOGY

The industry continues to find means of extending CMOS as a logic platform technology. FinFET transistors are already in high volume manufacturing and considerable research and development efforts are paid for by extending the life of FinFET and lateral gate-all-around (LGAA) nanowire/nanosheet transistors will be the succeeding transistor after FinFET in near future. It is expected that the following CMOS device configuration will be a vertical GAA (VGAA) nanowire, however, the device might be complimentary to LGAA and/or used as a selector of emerging memories. The following candidate is the 3D VLSI constructed by sequential integration. These are described in More Moore's chapter in detail. Several processes are proposed to achieve 3D VLSI including the wafer bonding process. From the standpoint of process control, metrologists should understand those future device architectures since new process control needs will be raised from device and process communities. One desirable request is a “non-destructive” manner for the metrology and inspection.

Even in the 3D VLSI era, mobility enhancement through local stress will remain a key means of increasing transistor performance. New channel materials will further enhance carrier (electron and hole) mobility. FinFET and planar transistors use high κ and metal gates while increases in mobility will be achieved using different technology than that used for planar CMOS. The metrology community continues research and development to fill these measurement needs. It is important to note that characterization and metrology must be tailored to the specific process used to fabricate the transistor. In this section, the specific metrology needs for starting materials, surface preparation, thermal/thin films, doping technology, and front-end plasma etch technologies are covered. Process integration issues such as variability, the need to control leakage current, and the reduction in threshold voltage and gate delay and their tolerances will interact with the reality of process control ranges for gate dielectric thickness, doping profiles, junctions, and doses to drive metrology needs. Modeling studies of manufacturing tolerances continue to be a critical tool for transistor metrology strategy. Potential solutions for FEP are shown in Figure MET-3.

The impact of shrinking dimensions on FEP metrology is already at the point where research devices and materials exhibit material properties associated with nanoscience. For example, the properties of nanowire-like shapes such as LGAA and VGAA are quantum-confined in two dimensions. Also, how to characterize parasitic capacitance and resistivity is a key challenge for FEP metrology. Methods to accurately measure contact resistance, and to characterize and understand their formation process with respect to new materials and processes are needed. Overall, a key challenge for FEP metrology in the next 15 years will be the integration of new materials (including 2D materials) to a wide variety of processes. Nondestructive and fast in-line metrology solutions with the required sensitivity are needed.

Figure MET3 FEP Metrology Potential Solutions

5.5.1. STARTING MATERIALS

Many of the metrology challenges related to starting materials involve the emerging class of layered materials such as SOI and strained silicon on SOI. The trend toward thinner layers, along with multiple layer interfaces, poses a challenge to most material metrology techniques.

Areas of concern include the following:

Bulk Ni and Cu measurement on p+, silicon on insulator (SOI), strained silicon (SSi), and strained silicon on insulator (SSOI) wafers

Measurement of 10^{9}–10^{10} cm^{-3} Fe (and other bulk metals) in the top Si of thin SOI wafers

Thickness and uniformity of very thin SOI layers (<20 nm)

Defectivity of thin layers (e.g., threading dislocations, “HF defects”)

- Particle detection (<100 nm) on layered surfaces

Silicon-On-Insulator (SOI) is entering the mainstream of IC device applications, and this is expected to grow further along the roadmap. Recent device work has motivated a prediction of an increase in SOI thickness at 22 nm ½ pitch from 7 nm of Si to ~ 10 nm. This is predicted to follow another decrease in thickness for several ½ pitch nodes. This prediction may not follow the FEP roadmap SOI timing. An unmet challenge is the measurement of SOI uniformity inside die-sized areas; across; across-wafer uniformity to the within-die level must also be characterized. An expectation has been that the materials specifications for polished silicon substrates would be transferred to SOI specifications. However, the underlying insulator structure in SOI negatively affects many of the metrology capabilities used for polished silicon substrates. Thus, there is some difficulty to measure and control SOI material properties at the level desired. The metrology community has addressed this, but some issues remain. For more details on these metrology challenges see the FEP chapter on Starting Materials.

5.5.2. SURFACE PREPARATION

In situ sensors for particles, chemical composition, and possibly trace metallics are being introduced to some wet chemical cleaning tools. Particle detection is covered in the *Yield Enhancement chapter.* Some aspects of particle/defect and metallic/organic contamination analyses are covered in the Materials Characterization Section of the *Metrology* chapter.

5.5.3. THERMAL/THIN FILMS

Next-generation high κ / metal gate technology will likely use nano-crystalline Hf-based oxides. As these alternative oxides continue to advance, new metrology challenges are emerging. The high κ gate stack contains several significant challenges that require further research and development. The Metrology roadmap previously discussed the challenges associated with the measurement of nitrogen concentration in high-κ dielectrics. The nanocrystalline film crystal structure has been characterized for phase composition and texture for a variety of new processes currently in research. The composition of work function adjusting films must also be characterized. The films used to adjust the gate work function are very thin and as a result, nanoscale roughness and non-uniformity may be of the same dimensions as the film thickness, thus making it impossible to use some traditional measurement methods. Materials characterization of annealed gate stacks is challenging for all the methods including ultra-high-resolution TEM. In addition, new DRAM structures that use mixed high-κ dielectrics and even ultra-thin layers of stacked high-κ dielectrics will also challenge the metrology development.

Metrology research and development is required for the advancement of new channel materials including germanium and III-Vs. Measurement needs are driven by the challenges associated with producing defect-free crystal structures due to lattice mismatch with the silicon substrate. X-ray diffraction reciprocal space maps have observed pitch walking and stress relaxation of a fin having top layers of silicon germanium alloy. The same method can apply to III-V fin structures. Measurement needs include observation and quantification of defect states in the band gap and dislocation densities. Many current measurement techniques require blanket films, and the correlation of measurements of blanket films with channel layers in transistors will require the use of cross-sections which may not be representative of the total transistor structure.

5.5.4. STRAINED SI PROCESSES

Carrier mobility enhancement through structure-induced local stress is a critical means of improving drive current and thus transistor performance [184]. Typically, NMOS transistors are given tensile stress by applying Si_3N_4 stress liner film over the gate electrode. Strain in PMOS transistors may be achieved using several different strategies. For example, the replacement of silicon around the source-drain with selectively grown SiGe induces compressive stress in PMOS transistor channels. Other strategies for inducing compressive stress include the use of compressive Si_3N_4 stress liner,, and shallow trench isolation (STI). Here, the pattern layout of the active area, gate electrode, and contact hole must be carefully designed, and the processes should be tightly controlled. A combination of techniques and selection of Si crystal orientation in the channel have also been proposed. New processes in the development phase require stress characterization and metrology. These include a Si:C (heavily carbon-doped silicon) replacement source-drain process, which is under consideration for NMOS. Si:C would induce tensile stress in the NMOS channel region. Changing the materials of gate electrodes and introducing the so-called Gate Last process, sources of stress have been increasing. Thus, the necessity of local stress metrology techniques is highlighted. It is known that TSV is another source of stress. To eliminate the negative effect on transistors near TSVs, a metric of keep-out zone (KOZ) is introduced. Another explanation of stress measurement is shown in the sub-chapter of 3D interconnect metrology.

To accelerate the design of the pattern layout and process conditions, a non-destructive direct measurement of the stress in the nano-sized area is desired. Recently, a synchrotron x-ray diffraction-based non-destructive approach was used to map Si/SiGe nanosheets for GAA structures [21], providing insight that could help understand the carrier mobilities of such future devices. A laboratory-to-fab transition of such techniques is needed to help accelerate technology development.

The importance of Finite Element Simulations of stress and resulting electrical properties has already been shown to be a key aspect of process development and metrology. Accurate stress metrology can help calibrate these simulations. As new processes are introduced with new technology generations, the challenge reintroduces itself. It is expected that a test pad would be used for in-line stress/strain measurement and its size is estimated at around 50 μm × 50 μm. This test pad size should be reduced the same as another metrology test pad for accurate film thickness measurement or OCD measurement.

A review of Stress Measurement Methods is shown in Figure MET-4. The information in Figure MET-4 is a revised version of data that was first published in 2011[185] is still current as of 20232023. This review shows a clear contrast in spatial localization capability between off-line methods such as nanobeam diffraction (NBD) and potential in-line methods from the standpoints of off-line destructive metrology and in-line non-destructive metrology. In the case of Raman spectroscopy[52, 186], the area of measurement depends not only on microscopic spatial resolution but also wavelength of illumination light. This is due to the penetration depth of the light. (*For further discussion, please see the "Materials Characterization for Strain-Based Devices" and "3D Nanoscale Characterization of Single Devices" sections.*) Tip Enhanced Raman Scattering or Spectroscopy (TERS) is one of the techniques to improve spatial resolution and sensitivity, a combination of surface-enhanced Raman spectroscopy (SERS) with the SPM probe. A review of transistor strain measurement techniques and applications is presented by Kuhn et al. [187]. Recently, a polarization-dependent in-line Raman spectroscopy was used to characterize the strain and chemical composition in GAA structures. Such information could be used as additional data for hybrid metrology [188].

Area of Interest	Measurement Method	Sensitivity Stress	Sensitivity Strain	Measurement Area	Sample Thickness	
Transistor Level						
	EBSEM (SEM)					Non-destructive
	CBED (TEM)	20 Mpa	0.02%	10 nm - 20 nm	>200 nm	Destructive
	NBD (TEM)	100 Mpa	0.10%	≈ 10 nm	<200 nm	Destructive
	TERS (Raman)	50 Mpa	0.05%	<50 nm		Non-destructive
Micro-Area Level	Confocal Raman	20 Mpa	0.02%	≈ 150 nm		Non-destructive
	XRD	10 Mpa	0.01%	100 µm		Non-destructive
	Photo Reflectance Spectrosopy	<20 Mpa	0.02%	1 µm		
Die						
	Die Level Flatness Laser Interferometry Coherent Gradient Sensing					Non-destructive
Wafer						
	Laser Interferometry Coherent Gradient Sensing					Non-destructive
	*Stress- Strain relation need to be clarified					

Figure MET4 Review of Stress/Strain Measurement Methods

5.5.5. DOPING TECHNOLOGY

Improved in-line process measurements to control active dopant are required beyond the 10 nm logic node. Presently, 4-point probe measurement is used for high-dose implant and photo-modulated optical reflectance (PMOR) is used for low-dose implant process control. PMOR has been shown capable of measuring active dopant profiles. Advances in PMOR are needed to extend it to thin SOI. A new technique that provides direct *in situ* measurement of dose, dopant profile, and dose uniformity would allow real-time control. New methods for control of boron (B), phosphorus (P), and arsenic (As) implants are also needed, and several in-line systems based on X-ray/electron interactions optimized for B, P, and As dose measurement have recently been introduced. Offline secondary ion mass spectrometry has been shown to provide the needed precision for current technology generations including ultra-shallow junctions. The range of applicability and capability of non-destructive measurement methods such as carrier illumination (an optical technology) are under evaluation. Two- and preferably three-dimensional profiling of active dopant concentrations is essential for achieving future technology generations. Activated dopant profiles and related technology computer-aided design (TCAD) modeling and defect profiles are necessary for developing new doping technology. Nanoscale scanning spreading resistance (SSRM) measurements done in high vacuum have proven capable of achieving the necessary spatial resolution for dopant concentration gradients. Recent results indicate that HV-SSRM is capable of measuring between 1 and 1.5 nm/decade in carrier concentration with a precision of between 3 to 5%.

The measurement of dopant profiles in 2D/3D structures, such as FinFETs, remains a challenge that needs dedicated techniques for the extraction of electrical properties in confined volumes [189, 190]. Indirect methods such as fin resistivity in test structures may detect process changes, but the direct determination of the dopant profile and its conformality is difficult.

Most techniques for 2D carrier distribution measurement technology can be broadly divided into SPM and TEM-based techniques. In addition, the 3D Atom Probe Tomography (APT), which provides information on atomic species and their spatial distribution, is promising for 2D carrier distribution measurement. A comparison of SPM[18, 191, 192], TEM and APT[193, 194] is shown in MET-5[195]. Although the techniques in MET-5 all measure carrier density, the measurement physics are different. Scanning spreading resistance microscopy (SSRM)[196] measures resistance; scanning nonlinear dielectric microscope (SNDM)[197] and scanning capacitance microscopy measure capacitance-related parameters; and scanning microwave microscope (SMM) is based on the microwave frequency material interaction. For TEM- and STEM-related techniques, energy dispersive X-ray spectroscopy (EDS) observes characteristic X-rays; electron energy loss spectroscopy (EELS)[198] observes energy loss of transmitted electrons; holographic and differential phase contrast (DPC) observes electric potentials.

As shown by the information in Figure MET-5, there are advantages and disadvantages for each method or family of methods. Broadly speaking, TEM/STEM and 3DAP methods have the highest resolution, while SPM based methods have the most sensitivity across B, P, and As. As in hybrid metrology (*discussed later*), some of the weaknesses of each method could be addressed by combining multiple techniques where possible [189, 194].

		PN	Quantitative	Sensitivity			Spatial Resolution
				B	P	As	
SPM	SSRM	×	✓	1E14 to 1E21	1E13 to 1E20	1E13 to1E20	1nm
	SNDM	✓	×	1E13 to 1E20	1E13 to 1E20	1E13 to 1E21	1nm
	SCM	✓	×	1E14 to 1E20	1E14 to 1E20	1E14 to 1E20	10nm
	SMM	×	✓	1E14 to 1E20	1E14 to 1E20	1E14 to 1E20	30nm
TEM	EDX	✓	×	Over 5E20	1E19 to 1E21	1E19 to 1E21	1nm
	EELS	✓	×	1E19 to 1E21	-	-	1nm
	Holography	✓	✓	1E19 to 1E21			1nm
3DAP		✓	✓	over 1E18			0.2 nm

Figure MET5 Carrier Density Profile Metrology[2]

5.6. 3D Interconnect Metrology

3D Interconnect process technology is covered in the Assembly and Packaging, Interconnect, and Emerging Research Materials metrology sections. The development of manufacturable 3D processes is also dependent upon a broad range of existing semiconductor metrologies including but not limited to thin film metrology, packaging metrologies, and electrical tests. These metrologies are not addressed in this section of the roadmap. See Dias and Goyal [199], De Wolf [200], Yun et al. [201] for reviews of 3D Interconnect measurement methods, processes, and materials.

The application specificity of 3D integration introduces a wide range of vertical interconnect densities and aspect ratios [202]. [203] [204], films of varying thicknesses, and structural features such as Cu pillars. Major challenges for 3D metrology include making measurements in high aspect ratio features, and the opaque nature of materials involved (i.e., silicon, copper, etc.) that limit optical microscopy techniques. Characterizing the reliability of these 3D interconnects, primarily due to thermal stress evolution, is a major concern. Currently, these challenges are addressed using destructive analysis while non-destructive techniques would be preferred. Destructive sample preparation tends to alter the sample under test so that the final measurement may not reflect the true value of the measurand, for example, underestimating the stress in Cu TSV and the surrounding Si [205]. A key challenge of 3D interconnect metrology is that any given technique would need to capture relatively small variations with a larger field of view. Hence, methods that strike a good balance between range and resolution (or sensitivity) or find ways to extend the range of the instrument without losing resolution or can be combined with other methods are desired.

5.6.1. Bonding Overlay

In-line overlay metrology is necessary to identify poorly aligned wafer pairs that are unlikely to provide electrically yielding interconnects. The optimized metrology strategy, with properly aligned closed feed- back loop, for bonding process control could avoid financial- and time associated with subsequent wafer processing.

Validation of the performance of process equipment for bonding wafers for 3D interconnects will require the use of infrared (IR) microscopy to measure alignment fiducials at the interface of the bonded wafer pairs (BWP), comparing overlay error to overlay tolerance, then determining if overlay accuracy is sufficient for electrically yielding interconnects. Silicon is transparent to IR radiation, which can penetrate through full thickness (775 microns thick for 300 mm diameter wafers) silicon wafers, enabling the measurement of overlay.

[2]*Information from reference [195] K. Nikawa, "Introduction to Panel Discussion: Dopant Visualization," in NANO Testing Symposium 2015, pp. 275-280*

Currently, there are many IR microscope tools capable of supporting in-line overlay metrology requirements for bonded wafer pairs in high-volume manufacturing (HVM). They use either broadband IR (typically from a halogen lamp) or a specific IR laser-generated wavelength (typically 1310 nm). An IR metrology tool for this purpose has demonstrated repeatability of overlay measurements on bonded wafer pairs with 1 sigma repeatability of less than 0.1 μm. The spatial resolution of this system based on the Rayleigh criterion is ~ 0.5 μm. In the case where the carrier substrate is transparent to visible light, the use of metrology equipment with a top and bottom microscope configuration can also be an alternative solution. This configuration can also demonstrate the 1 σ repeatabilityof less than 0.1 microns.

Overlay performance is an inherently 2D parameter. Circular via features are bonded to circular bond pads, in patterns that span the full size of the wafer pair. Most statements of overlay performance focus on performance in a single axis. Definitions of overlay that are consistent with the multi-dimensional nature of the actual requirement and test methods that account for overlay performance throughout the entire wafer area should be defined.

5.6.2. BONDED INTERFACE DEFECT DETECTION

Good bonding at the interface of a bonded wafer pair, and in hybrid bonding, is critical to ensure that the pair does not separate during subsequent operations like wafer thinning and wafer bevel edge trim. Using in-line defect metrology is necessary to identify bonded pairs that have the potential to separate during subsequent wafer thinning and edge bevel trimming operations. Bonding wafers for 3D interconnects and packaging will require the use of IR microscopy to locate and review defects at the interface of a bonded wafer / chip pair. These defects are present on individual wafers prior to bonding (particles, chemical-mechanical planarization (CMP) damage) or generated during the bonding process (voids, adhesive anomalies, dendritic structures). BWP defect review tools will need to be able to merge individual wafer defect maps into a combined BWP map and will require the ability to add any new defects randomly observed during defect review. The “nano-voids” associated with the annealing step to strengthen the interface in hybrid bonding are currently only detectable by off-line TEM.

Bonding wafers for 3D interconnects will require the use of IR microscopy to locate and review defects at the interface of a bonded wafer pair due to particles, chemical-mechanical planarization (CMP) damage), generated during the bonding process (voids, adhesive anomalies, dendritic structures), or due to the surface reconstruction of the metallic pads at the bonding interface.

BWP defect review tools will need to be able to merge individual wafer defect maps into a combined BWP map and will require the ability to add any new defects randomly observed during defect review. Currently, there are defect review tools using an IR microscope capable of supporting defect review requirements for bonded wafer pairs in high volume manufacturing. An IR microscope is not useful as a defect identification tool as outlined in section 2.3. The field of view of the microscope is relatively small, and 100% inspection of the entire wafer is not feasible. However, defects can be manually identified at the interface of the BWP and added to its defect map. Although there is no BWP defect review requirement specified in roadmap, it is recommended that it be included in the future revision.

Scanning acoustic microscopy (SAM) [201] has proven useful to detect and characterize bond “macro” voids at bonded pair interface. These macro defects are usually linked to design singularities which lead to manufacturing issues (such as too much erosion, protrusion or dishing during CMP) during the surface preparation step. SAM resolution for BWP voids approaches 60 microns (using a 110 MHz transducer). SAM resolution is improved by using higher frequency ultrasound and thinning wafers to decrease ultrasound attenuation, but thinning wafers to achieve improved SAM resolution is not a manufacturable solution for metrology in HVM. The throughput of this method must also be improved for volume production.

Currently, there are a number of SAM tools capable of supporting in-line void metrology requirements for bonded wafer pairs in high-volume manufacturing. Dry-in, dry-out SAM systems that use a nitrogen stream to remove couplant liquid from the external surfaces of a bonded wafer pair are available. There is some concern for added defectivity because of the couplant liquid used (particles, metallics), but subsequent thinning operations and the cleaning steps that follow are expected to be sufficient for reducing SAM-induced defects. Another concern is the lack of hermeticity at the interface of the bonded wafer pair that can allow couplant liquid incursion into the interface via capillary action. The use of a liquid spray instead of complete immersion could be an attractive alternative.

There are no metrology tools capable of supporting in-line bonded wafer pair defect identification with defect mapping in a Cartesian coordinate system for subsequent defect review. Although there is no BWP defect identification requirement specified in the roadmap, it is recommended that it be included in the future revision.

Edge bevel inspection is required to identify defects in a bonded wafer pair that can lead to subsequent wafer breakage. Edge bevel defects can be problematic at bonding. Edge bevel chips can initiate cleave lines for silicon wafer breakage when the forces associated with bonding or thinning wafer pairs are applied. The control of the notch alignment of bonded wafer pairs with an accuracy of less than 50 microns is also needed. Wafer edge bevel trim operations that precede bonded wafer pair thinning can be another source of edge bevel defects.

There are a number of edge bevel inspection tools capable of supporting in-line metrology requirements for bonded wafer pairs in high-volume manufacturing. Although there is no edge bevel defect requirement specified in the roadmap, it is recommended that it be included in the future revision.

5.6.3. BOND STRENGTH UNIFORMITY

Although there is no BWP strength uniformity requirement specified in the roadmap, it is recommended that it be included in the roadmap by specifying micro-chevron testing as described in SEMI standard MS-5[206].

Currently, there are no in-line tools to assess bonded wafer pair strength uniformity. Micro-chevron testing for BWP strength uniformity uses a wafer with an etched pattern (micro-chevron), bonded to a blanket film wafer that is subsequently divided into individual dies and tested for adhesion strength using a pull-tester. Mapping bonding strength results for multiple dies on a BWP allows calculations for within-wafer pair non-uniformity and indicates adjustments to the wafer bonding hardware are required when strength uniformity results drift outside of established control limits. Micro-chevron testing is more sensitive and repeatable than other bond strength tests like a 4-point bend. A technique for the evaluation of the surface energy of the bonding between silicon wafers and SOI, based on crack propagation theory [207] has been developed. Similarly, recent technique, derived from the standard Double Cantilever Beam (DCB) method in combination with interferometry in confocal IR laser, assesses direct bonding energies, at the wafer scale. [207]

5.6.4. BONDED WAFER PAIR THICKNESS

The total thickness and intra-wafer total thickness variation (TTV) of the BWP are crucial for the bonding and grinding operation. Currently, there are several metrology tools capable of supporting in-line measurement. The traditional capacity method technique has limitations in the case of non-conductive substrates. The white light or IR chromatic, as well as interferometry technique, can provide a very good alternative for total thickness measurement when implemented in a top and bottom dual mode configuration.

The measurement of individual layers consisting of the BWP will generally require the use of an IR light source to pass through the silicon layers. A major drawback of the IR interferometer technique is the lack of resolution for thin layers. With improvement in detection treatment algorithm, thin layers such as the adhesive layer itself could be measured.

5.6.5. TSV ETCH DEPTH

Depending on the application, through-silicon vias (TSVs) can have very high aspect ratio of via diameter to etch depth, approaching 10:1–20:1. These HAR features challenge, and limit, the use of optical metrology techniques for measuring smaller diameter TSVs.

Currently, there are several TSV etch depth metrology tools capable of supporting in-line metrology requirements in high-volume manufacturing. Depending on the principle of the techniques involved and its spot size, the measurement can be done on individual TSV, on an average number of TSVs, or will require a specific periodic array of TSVs.

White light interferometry and backside infrared interferometry can be used for measuring the etch depth of individual TSVs for 5 µm and larger diameter TSVs with less than 10:1 aspect ratio. For the white light interferometer and smaller diameter, improvement in sensor configuration is needed to get paralleled collimated light to able to be reflected down to the bottom TSV. Backside infrared interferometry has been demonstrated as capable for TSV etch depth metrology for sub-micron features and is not limited by aspect ratio.

The model-based infrared reflectometry on an array of TSVs could be another alternative for depth measurement of diameter below 5 micrometers on the condition the density of vias is high enough to get a diffracted signal. This technique is not a direct technique and will require cross-section analysis for calibration.

5.6.6. TSV ETCH PROFILE

Currently, there are no in-line TSV etch profile metrology tools suitable for use in high-volume manufacturing. Through-focus scanning optical microscopy (TSOM) method shows potential for this application [208-211]. TSOM

is a method that collects and uses the entire through-focus optical intensity information in 3D space using a conventional optical microscope [212]. The 3D shape of a target can be inferred by analyzing the additional information (e.g., intensity variations with focus) present in the 3D optical data using TSOM images. TSOM has demonstrated good sidewall angle sensitivity [213] and could be used as a high-throughput [211], low-cost, and nondestructive 3D shape metrology method suitable for HVM. Both isolated and dense TSV/HAR targets could be measured using the TSOM method. Target sizes (depths/heights) ranging from sub-10 nanometers to over 100 µm can be analyzed, making it suitable for TSVs and other HAR targets. Improved sidewall sensitivity can be expected using IR wavelengths that can penetrate much deeper into Si (*see the section on Hybrid Metrology for addition information*).

In applications such as the TSV etch profile, TSOM compliments the other tools by enabling measurements over a larger measurement range. TSOM potentially reduces or eliminates optical cross correlations improving measurement uncertainty. TSOM can be deployed in-line in the increasingly complex manufacturing process making it suitable for computational process control (CPC) [208]. More broadly speaking, instruments for the TSV etch profile should be able to capture variation over the full range of the etch profile.

5.6.7. TSV LINER, BARRIER, SEED THICKNESS

The deposition of liner, barrier, and seed films is challenged by the high aspect ratio of the TSV and directional film deposition processes. Continuous, pin-hole-free films in the TSV are required to electrically isolate, prevent copper migration, and encourage good copper fill in the subsequent copper plating process.

Currently, there are no in-line tools suitable for TSV liner, barrier, and seed thickness metrology for use in high-volume manufacturing. Cross-section SEM and TEM analysis can be utilized for process development but are destructive techniques. Electrical test structures can be utilized for measuring leakage and electromigration. Cu diffusion into substrate can be monitored with techniques such as: TVS+BTS and/or TDDB. The information from test structure lag process flow; they are obtained long after liner, barrier, and seed deposition.

Although there are no TSV liner, barrier, and seed thickness metrology requirements specified in the roadmap, it is recommended that they be included in the future revision.

5.6.8. TSV VOIDS

Micro-voiding in the TSV metal fill or in the interconnect bond region could lead to electrical or reliability failures. Using standard cross- sectioning or FIB/SEM techniques it is possible to destructively evaluate the condition of a selected bonded vias. Non- destructive methods to identify these defects would provide significant benefits for both process development and failure analysis [214], but may require specialized test structures.

TSV void metrology is challenged by the opaque nature of copper; optical metrology techniques for void detection are not available. Acoustic wave techniques are also investigated through the change in the total volume of the copper lines. The capability to scan the whole TSV depth as well as the sensitivity to micro-void has to be demonstrated. Copper plating is challenged by the high aspect ratio of the TSV; any tendency towards conformal plating must be carefully controlled by plating bath additives to ensure bottom-up filling.

X-ray techniques [201] have proven useful in revealing voids within copper-filled TSVs, but are slow and require destructive sample preparation. X-ray tools cannot be considered as in-line TSV void metrology for high-volume manufacturing, but are useful for feedback on TSV plating process development, especially when coupled with rapid data analyses [215].

5.6.9. SHAPE AND STRESS

The shape of the BWP is usually controlled through bow and warp measurements over the process flow. This is critical not only for process monitoring but also for all aspects related to handling of thin wafers in a manufacturing context. Currently, there are many metrology tools capable of supporting these in-line measurements. Various techniques such as laser deflection, capacity, chromatic and interferometer techniques, and coherent gradient sensing (CGS) can give the shape of the BWP. As it stands, the results strongly depend on the way the wafer is held and at some point, can be impacted by the gravity effect. Coherence between metrology semiconductor suppliers needs to be improved through SEMI standard recommendations. This will allow comparable results between techniques.

The introduction of large-scale TSV in a CMOS environment is also raising the question of stress induced by the TSV themselves. Raman spectroscopy [200] can measure stress distribution in the silicon around the TSVs using small spot but the technique needs to move to longer wavelengths to get information from deep silicon. Off-line analysis such as

synchrotron XRD and Electron Backscatter Diffraction (EBSD) techniques are also implemented alternatives to get the strain measurement.

5.6.10. 3D METROLOGY FOR COPPER NAILS AND PILLARS

For 3D interconnect technologies, such as stacking circuit blocks and 3D IC, there is a need to control the height, diameter, and coplanarity of the copper pillars that will connect the top and bottom of the stacked dices. This request pretty much equivalent to bumps measurements in backend manufacturing plants becomes now also critical at the wafer level for IC manufacturing.

There are a number of metrology tools capable of measuring those parameters at a production scale. Techniques such as laser triangulation or confocal interferometry are very well adapted. Nevertheless, there is clearly a lack of reference standards available to address deficiencies in 3D metrology.

5.7. INTERCONNECT METROLOGY

New processes, novel structures, and aggressive dimensional scaling continue to drive metrology research and development for interconnect technology. Increasingly porous low κ dielectric materials are moving into manufacturing, and 3D Interconnect is being used in a great variety of applications. Air gap structures are being adopted in flash due to resistance-capacitance (RC) constraints. All areas of metrology including materials characterization, in-line measurements, and advanced equipment and process control are used for interconnect research, development, and manufacturing. As copper/low κ interconnects continue to scale by reducing dimensions and increasing porosity, the metrology challenges become more difficult. In particular, barrier conformality of 2 nm films, the presence of 3 nm sized voids in copper lines, the size and crystallographic orientation of nm-size copper grains, the size and connectivity of nm-size pores in dielectrics and the characterization of etch residue, etch damage and barrier penetration into porous low-k films all become more challenging. As dimensions approach the 5 nm scale, interfacial effects can drive very large perturbations in dielectric constant, grain boundary scattering, thermal conductivity, and barrier effectiveness. The need to integrate multi-layer stacks of low κ dielectrics with ever-decreasing mechanical and chemical stability requires techniques that can characterize the stress and chemical states of these amorphous materials. Air gaps bring their own unique set of metrology challenges with respect to measuring the air gap itself and the process sequence to fabricate the air gap.

In addition to scaled copper/low -κ interconnects, new and alternative interconnect solutions such as optical, carbon- and spin-based interconnects have their own metrology challenges. While the characterization of the optical properties of blanket dielectric films is routine to the semiconductor industry, the determination of optical loss due to sidewall roughness and measurements of the electro-optic effect of optical modulator materials is far from routine and usually requires complex, integrated test structures. While progress has been made to determine the chirality of carbon nanotubes, there are challenges to determining the bandgaps of narrow graphene ribbons and scattering lengths for spin-polarized transport in more speculative interconnect options.

Development of interconnect tools, processes, and pilot line fabrication all require detailed characterization of patterned and un-patterned films. Currently, many of the in-line measurements for interconnect structures are made on simplified structures or monitor wafers and are often destructive. Small feature sizes including ultra-thin barrier layers will continue to stretch current capabilities. Interconnect metrology development will continue to be challenged by the need to provide physical measurements that correlate to electrical performance, yield, and reliability. More efficient and cost-effective manufacturing metrology requires measurement on patterned wafers. Cost and efficiency improvements require fast in-line identification and minimal intervention on good wafers; as well as quickly identifying bad wafers for further analysis.

Interconnect needs for metrology include continuing evolutionary advances in existing metrology techniques, as well as the increasing need for novel metrology approaches for more radical interconnect structures. The following sections will describe some of the needs and status of existing metrology techniques for copper and low-κ interconnects. The preceding section focused on the needed advances for future directions in 3D interconnects. Some potential solutions for interconnects are shown in Figure MET-6.

5.7.1. CU – LOW K METALLIZATION ISSUES AND METROLOGY NEEDS

5.7.1.1. CU METALLIZATION ISSUES

Copper (Cu) metallization has been used in high-volume manufacturing for over six generations. With each shrink, the challenges of defect-free filling of trenches and vias must be addressed. In addition, barrier conformality, nm-size voids, determining, the size and orientation of Cu grains, and the need for precise control of electrochemical deposition

baths must be characterized. Voids in metal lines and vias that occur during processing have been identified as significant yield loss initiators. Voiding problems can show up after deposition/CMP/anneal, or from agglomeration of micro-voids due to electro or stress migration. Another significant problem relating to voids is the need to be able to identify relatively small, isolated voids in large fields of patterned Cu conductors. These isolated voids often do not show up as yield loss but can be an incipient cause of later reliability failures. These voids may be on the surface of the conductors but are often buried within the conductor pattern or in vias. Techniques such as incoherent bright-field STEM tomography has been applied to void detection[216], but additional refinements are needed. Additional issues with Cu metallization arise from the use of thin barriers to isolate Cu from underlying dielectrics. These thin barriers raise significant needs for measurement capabilities of ultra-thin layers, interface properties, and defects and materials structure on sidewalls in very narrow channels. These needs require the ability to not only establish physical properties and structure of these layers with thicknesses <2 nm but also identify and characterize defects in the films. An additional problem area is the characterization of the interfaces between the Cu electroplated layer, the Cu seed, the barrier layer, and the dielectric. As the Cu conductors become smaller, both grain boundary and sidewall interface scattering will cause significant increases in the resistivity of very narrow lines. SiCOH and pSiCOH have been successfully integrated in VLSI devices since the 90 nm technology node. Metrology is needed to understand the SiCOH metastable intermediates which can shed light on the ultimate stability and scalability of these materials[217, 218].

5.7.1.2. Cu Metallization Metrology

Copper electroplating systems need a quantitative determination of the additives, byproducts, and inorganic contents in the bath to maintain the desired properties in the electroplated copper film. Process monitoring requires *in situ* measurements of additives, byproducts, and inorganic content that result from bath aging. Cyclic voltammetric stripping (CVS) is widely used to measure the combined effect of the additives and byproducts on the plating quality. Liquid Chromatography can be used to quantitatively measure individual components or compounds that are electrochemically inactive and volumetric analysis using titration methods can be used for the monitoring of inorganics.

Barrier layer metrology needs include measurement of thickness, spatial uniformity, defects, and adhesion. In-line measurement for 3D structures continues to be a major gap. Measurement of materials on the sidewall of low-κ trenches is made even more difficult by the roughness along the sidewall. There is some concern about the application of statistical process control to very thin barrier layers. Barrier layers for future technology will be <2 nm thick. Presently, a number of measurement methods are capable of measuring a barrier layer under seed copper when the films are horizontal. These methods include acoustic methods, X-ray reflectivity, and X-ray fluorescence. Some of these methods can be used on patterned wafers. For measuring both vertical and horizontal liner/ barrier/ seed layers on patterned wafers, mass metrology is used to provide an in-line measurement for the stability of the process. Extended X-ray Absorption Fine Structure (EXAFS) measurements have also been applied to the characterization of the properties of self-forming barriers in integrated structures. In-line measurement of crystallographic phase and crystallographic texture (grain orientation) of copper/barrier films is now possible using X-ray diffraction and electron back-scatter diffraction-based methods. This technology is under evaluation for process monitoring, and the connection to electrical properties and process yield is being investigated.

Detection of voids in copper lines is most useful after the CMP and annealing processes. A metric for copper void content has been proposed in the Interconnect roadmap and in-line metrology for copper voids is the subject of much development. However, these efforts are focusing on the detection of voids only and not on the statistical sampling needed for process control. Many of the methods are based on the detection of changes in the total volume of the copper lines. The typical across-chip variation in the thickness of copper lines will mask the amount of voiding that these methods can observe. Interconnect structures, which involve many layers of widely varying thickness made from a variety of material types, pose the most severe challenge to rapid, and spatially resolved multi-layer thickness measurements.

Some measurements remain elusive. For example, the measurement of barrier and seed copper film thickness on sidewalls is still difficult. However, mass change measurement is extremely sensitive to sidewall thickness variations.

Recently crystallographic texture measurements on sidewalls have been reported. Adhesion strength measurements are still done using destructive methods. Endpoint detection for etching must be developed for new etch-stop materials for porous low-κ films. Other areas of metrological concern with the new materials and architectures include in-film moisture content, film stoichiometry, mechanical strength/rigidity, local stress (versus wafer stress), and line resistivity (versus bulk resistivity). In addition, calibration techniques and standards need to be developed in parallel

with metrology. See Weiss et al.[219] and Zhou and Li [220] for reviews of Interconnect characterization methods and properties of Interconnect materials.

5.7.2. Low κ Dielectrics Issues and Metrology Needs

5.7.2.1. Low κ Dielectrics Issues

The move from SiO_2 to porous low κ dielectrics in interconnect structures has proven to be a more difficult challenge to the semiconductor industry than the move from Al metallization to Cu. A significant part of the difficulties has come from the fact that low κ materials available thus far have significantly different physical and mechanical properties than the prior SiO_2. Among the primary differences are more complex deposition chemistries, significantly different mechanical properties, and the presence of pores in the material. The lower mechanical strength has resulted in a new set of issues stemming from problems resulting from materials and processes used in back-end manufacturing showing up as problems at assembly and packaging. A significant part of the problem is that there are no convenient and competent metrology tools and methodologies to qualify materials at the back-end process stage for assembly and packaging viability. A second major issue has been identified with the characterization of porous materials. At present, there are no metrology techniques and methodologies to identify anomalously large or significantly connected pores (so-called "killer pores") in otherwise smaller pored materials. There are also no available metrology techniques to characterize the materials on the sidewalls of low κ patterns for physical properties, chemical structure, and electrical performance. This capability needs to be able to identify and quantify very thin layers on these sidewalls related to physical layers and damage due to processes such as pore sealing and plasma etch damage. These features need to be quantifiable both on continuous sidewall surfaces and into pores on porous materials. Pore sealing processes generate metrology challenges as only a very thin layer (2 nm or less) has to be deposited on top and/or along the low-k film. Most of these pore sealing processes also generate some damage in the low-k film which should also be analyzed. In order to characterize accurately both pore sealing and possible damage, extremely precise measurement techniques are needed.

The issues noted above, along with the standard measurements associated with dielectrics, need to be addressed not only for today's dielectrics but also for those that will be used in the few nanometer generations of the not-too-distant future.

5.7.2.2. Low κ Metrology

In-line metrology for non-porous low κ processes is accomplished using measurements of film thickness and post-CMP planarity. *In situ* sensors are widely used to control CMP. Metrology continues to be a critical part of the research and development of porous low κ materials. The need for the transition of some of the measurements used during process development into volume manufacturing is a topic of debate. Examples include pore size distribution measurement. Pore size distribution has been characterized off-line by small angle neutron scattering, positron annihilation, a combination of gas absorption and ellipsometry (ellipsometric porosimetry), and SAXS[221, 222]. SAXS and ellipsometric porosimetry can be used next to (at-line) a manufacturing line. The need for moving these methods into the fab is under evaluation. Detection of large, "killer," pores in patterned low κ has been highlighted as a critical need for manufacturing metrology by the Interconnect Roadmap.

High-frequency measurement of low κ materials and test structures has been developed up to 40 GHz to determine both frequency-dependent dielectric constants and losses. This meets the need for clock rates of up to about 5 GHz. In general, low-κ materials seem to have nearly constant dielectric functions over the frequency range of interest (from 1 GHz to 10 GHz).

Thinning of porous low κ during chemical mechanical polishing technology must be controlled, and available flatness metrology further developed for patterned porous low-κ wafers. Stylus profilers and scanned probe (atomic force) microscopes can provide local and global flatness information, but the throughput of these methods must be improved. Standards organizations have developed (and continue to develop) flatness tests that provide the information required for statistical process control that is useful for lithographic processing. Pore stuffing and subsequent unstuffing of low-κ films is a promising technique in order to minimize damage induced in the low-κ by processes such as plasma etching and pore sealing. An important issue is the fact that after unstuffing, the low-κ film should be as comparable as possible to the pristine/original low-κ film, for example, no stuffing residues should remain inside the film. Even minute remainders will affect the performance of the film significantly. Characterization of these remainders will continue to be a challenge for metrology.

Interconnect-specific CD measurement procedures must be further developed for control of etch processes. Key gaps include the ability to validate post-etch clean effectiveness, sidewall damage layer, and properties. Angle-resolved

photoelectron spectroscopy has shown some success at characterizing nm thick residue and chemical modifications on sidewalls. Rapid 3D imaging of trench and contact/via structures must provide profile shape including sidewall angle and bottom CD. This is beyond the capabilities of current in-line CD-SEMs. Etch bias determination is difficult due to the lack of adequate precision for resist CD measurements. One potential solution is scatterometry, which provides information that is averaged over many lines with good precision for M1 levels, but this precision may degrade for higher metal levels. Furthermore, scatterometry must be extended to contact and via structures. Other techniques with potential include 3D AFM[223] and He ion microscopy. Electrical test structures continue to be an important means of evaluating the RC properties of patterned low-κ films.

Figure MET6 Interconnect Metrology Potential Solutions

5.8. MATERIALS CHARACTERIZATION

The rapid introduction of new materials, reduced feature size, new device structures, and low-temperature processing continues to challenge materials characterization and contamination analysis required for process development and quality control. Correlation of appropriate offline characterization methods, with each other, and with in-line physical and electrical methods, is often necessary to allow accurate measurement of metrics critical to manufactured device performance and reliability. Characterization accuracy requirements continue towards tighter error tolerances for information such as layer thickness or elemental concentration. Characterization methods must continue to be developed toward whole wafer measurement capability and clean room compatibility.

The declining thickness of films, moving into the sub-nanometer range, creates additional difficulties to currently available optical and opto-acoustic technologies. Shorter wavelengths of light even into the X-ray range are currently being investigated to overcome the challenge of in-line film thickness and composition detection. Complimentary techniques are often required for a complete understanding of process control, for example, X-ray reflectometry can be used to determine film thickness and density while UV ellipsometry can determine thickness, optical index, and bandgap.

Often, offline methods provide information that in-line methods cannot. For example, TEM and STEM can provide the highest spatial resolution or cross-sectional characterization of ultra-thin films and interfacial layers. STEM systems equipped with X-ray detection and electron energy loss spectroscopy (EELS) have provided new information about interface chemical bonding. High-performance secondary ion mass spectroscopy (SIMS), and its variant time-of-flight (TOF) SIMS, provide contamination analysis of surfaces and thin film stacks. Grazing incidence X-ray reflectivity (XRR) provides a measurement of film thickness and density, while grazing incidence X-ray diffraction provides information about the crystalline texture of thin films. The importance of using diffuse scattering in addition to specular scattering during XRR seems to be critical to building interfacial models from XRR that can be compared to interfacial models from other methods such as TEM/STEM, SIMS, and ion backscattering. Field emission Auger electron spectroscopy (FE-AES) provides composition analysis of particulate contamination down to less than 20 nm in size. Offline characterization of physical properties such as void content and size in porous low-κ insulators, film adhesion, and mechanical properties, for example, is required for the evaluation of new materials. Many of these tools are now available for full wafers up to 300 mm in diameter.

Continued development of TEM and STEM imaging capability is required. TEM/STEM methods require sample preparation methods that can result in metrology artifacts if care is not taken. The choice of detection angle for annular detectors employed in STEM instruments allows imaging contrast to vary from incoherent imaging sensitive to mass-thickness variations to coherent imaging sensitive to crystal orientation and strain. Several technologies are being applied to materials and process development for critical areas such as high and low κ. Electron energy loss spectroscopy (EELS)[198] can achieve spatial resolution of atomic columns for oriented crystalline samples. With this greatly improved spatial resolution, EELS can be used to characterize interfacial regions such as that between high κ dielectrics and the silicon substrate. STEM with annular dark field imaging and EELS are becoming routine in manufacturing support labs, however spatial resolution in regular practice is often limited by real device samples where amorphous and disordered interfaces increase probe interaction volumes beyond those afforded by channeling along atomic columns in perfect crystals. Further routine site-specific sample preparation conducted by a focused ion beam generally produces samples in the 100 nm thickness range. For certain applications such as lithographic cross-section metrology of photoresist and gate side wall angle measurements, this is sufficient. More challenging applications require a thickness of below 50 nm for optimal spatial resolution in imaging and analysis. Great advances have been made using *in situ* argon beam thinning of samples. Advances in image reconstruction software have also improved image resolution and thus interfacial imaging. Several improvements in TEM/STEM technology are now commercially available including lens aberration correction and monochromators for the electron beam. Recent

breakthroughs in aberration-corrected scanning TEM look very promising and reveal details such as single misplaced atoms in a junction. Further, via combined application with high-brightness electron sources, improved resolution may be achieved at reduced incident beam acceleration potentials allowing TEM measurements below the damage threshold energies that have plagued high-resolution characterization of fragile materials including carbon nanotubes and graphene. These TEM/STEM tool improvements require much improved sample preparation; thinner samples and reduced surface-damage layers.

Electron tomography, producing 3D models of device structures, may play an increasingly important role in metrology but is currently cost prohibitive. Tomography has less stringent sample preparation conditions as surface damage regions may be removed from reconstructions and thicker samples are generally desired.

Advances over traditional energy dispersive X-ray spectrometers (EDS) and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room. New X-ray detectors will allow the resolution of slight chemical shifts in X-ray peaks providing chemical information such as local bonding environments. Prototype microcalorimeter EDS and superconducting tunnel junction techniques have X-ray energy resolution capable of separating overlapping peaks that cannot be resolved with current-generation lithium-drifted-silicon EDS detectors. Although beta site systems have been tested, unfortunately, these have not become widely available. These detectors can also be implemented in micro XRF (X-ray fluorescence) systems, using either an electron beam or a micro focus X-ray beam as the excitation source. XPS (X-ray photoelectron spectroscopy) is now widely used to determine the thickness and composition of thin (up to 50 nm) films.

While these and other offline characterization tools provide critical information for implementing the Roadmap, there are still many challenges. Characterization of high-κ gate stacks is difficult due to the length scales for which electrical properties are determined. For example, chemical intermixing by reactions forming intermetallics or alloys may be easily confused with physical roughness at an interface. Characterization techniques that probe the local atom-atom interactions including electron energy loss spectroscopy, and X-ray absorption near edge structure spectroscopy are often required. In addition, as device features continue to shrink and new non-planar MOS devices are developed, the applicability of characterizing planar structures as representative of device features becomes more questionable. Furthermore, ongoing scaling makes the analysis of contamination in high aspect ratio structures even more difficult.

The introduction of new materials will raise new challenges in contamination analysis, such as what happened with copper metallization where the very real possibility of cross-contamination has led to the need to measure bulk copper contamination down to the order of 10^{10} atoms/cm^3 and surface copper contamination even in the edge exclusion and bevel regions, all because of the high diffusivity properties of this deleterious metal. Device shrinking also tends to lower the thermal budgets allowed for processing so that the behavior of metal contamination and how to reduce its negative effects are changing the characterization needs. For example, low-temperature processing is changing which surface contamination elements, and at what levels, need to be controlled and therefore measured. A key example is the role of surface calcium on very thin gate oxide integrity and the difficult challenge of measuring this surface element at the 10^8 atoms/cm^2 level. Traditional methods such as vapor phase decomposition followed by ion-coupled plasma mass spectrometry (ICP-MS) can have day-to-day limitations at this level. In addition, low-temperature processing is changing how metal contamination gettering is achieved, challenging the way to characterize material properties to ensure proper gettering.

Metallic contamination has long been known to be a key detrimental factor to device yield, causing degradation of electrical parameters like gate oxide breakdown voltage and background noise in charge-coupled devices (CCD) for instance. Historically, monitoring has been achieved in-line through the use of monitor wafers and a combination of total reflectance X-Ray Fluorescence (TXRF) and post-anneal surface photovoltage (SPV). Unfortunately, with the ever-increasing sensitivity of new technologies to trace metal contaminants and the more stringent quality criteria imposed by certain applications, this type of control scheme often has limitations both in terms of sensitivity and detection capabilities. A technique like automated vapor phase decomposition/ion coupled plasma mass spectrometry (VPD /ICP-MS) can be powerful in this context as ultimate detection limits can be reached (down to a few 106 at/cm^2 for some species). Full or semi-local wafer measurement can be performed, and tool automation enables insertion as a true monitoring tool in a production line. In addition, bulk analysis can also be achieved through adequate chemistries which in combination with deep-level transient spectroscopy (DLTS) can offer a full range of analytical capabilities both in terms of identification and quantification.

5.8.1. MATERIALS CHARACTERIZATION FOR STRAIN-BASED DEVICES

The accelerated use of strained silicon without SOI has resulted in new metrology and characterization requirements earlier than predicted. Gate oxide metrology becomes even more complex when strained Si channel structures are used as the starting material instead of bulk Si or SOI wafers. Strained Si is either grown on thick relaxed SiGe buffer layers on bulk Si or on compliant substrates consisting of thin SiGe layers on SOI. In both cases, the metrology of the starting material is crucial with a large number of parameters to be controlled: 1) thickness and Ge profile of the SiGe buffer, 2) thickness of the strained Si channel, 3) roughness of the Si/SiGe interface and the Si surface, 4) magnitude and local variation of stress in the Si channel, 5) threading dislocation density in the Si channel (high sensitivity of the measurement is needed since the desirable dislocation density is very low (at $<10^3$–10^4 cm^{-2})), 6) density of other defects, such as twins, dislocation pile-ups, or misfit dislocations, particularly at the SiGe/Si channel interface, and 7) distribution of dopants in channel and buffer (particularly after thermal annealing). Several methods employing TEM/STEM have been developed to measure and map strain distributions in strained-channel devices. It has been noted that thinning of a TEM sample may allow relaxation of some of the strain, and finite element modeling has been useful in understanding how strain may be relaxed during sample thinning, however strain measurement by TEM/STEM has had many successes. Both threading and misfit dislocations can be measured by TEM, but the limited sample size area is often a problem for the required statistical analysis of dislocation densities. Atomic force microscopy determines the surface roughness of the Si channel. Optical microscopy has been successful for etch pit density (EPD) measurements to determine the density of threading dislocations intercepting the wafer surface. Clear prescriptions for EPD are needed to select the etch depth. The meaning of lines and points in the EPD optical images need to be explained. X-ray tomography is another technique offering promise for defect detection. The Ge and dopant profiles can easily be measured with SIMS. A high sputtering rate is needed for thick SiGe buffers, while high-depth resolution (possibly with a low-energy floating ion gun) enables the analysis of the thin Si channel and the channel/buffer interface. Optical carrier excitation using a red photodiode directed at the sputtering crater has been used to avoid SIMS charging artifacts; this is particularly important for strained Si over SOI and for undoped layers.

Unique properties associated with strained silicon are being addressed with a variety of metrology methods. Stress is the force required to create lattice strain which affects the electronic band structure to provide mobility enhancement of electrons or holes. Raman spectroscopy can measure stress, while TEM and XRD measure strain. Raman spectrometry measures the energy of the Si-Si vibration in the Si channel which depends on changes in stress. However, the phonon deformation potential (describing the variation of the Si-Si phonon energy with stress) is not firmly established for thin Si channels. Such Raman measurements need to be performed using a UV laser to avoid penetration of the laser into the Si substrate. At 325nm wavelength, the entire Raman signal stems from the thin Si channel, simplifying data analysis. For longer wavelengths, the Si- Si vibration in the SiGe buffer complicates the signal. The energy of the Si-Si vibration in SiGe depends on alloy composition and stress, which complicates the problem. Raman mapping yields the stress distribution across the wafer with a maximum resolution of about 0.5 μm, thus allowing prediction of transistor-to-transistor variations in mobility enhancement. It would be desirable to improve this resolution, possibly using solid or liquid immersion techniques. Micro-XRD is also applied to measure the stress in small structures, but currently, the analysis spot is in the 5-10 micron range, making device analysis not yet feasible. Analysis of ellipsometry data for strained Si channels is complicated, since the dielectric function of Si depends on the stress. This relationship (described by the piezo-optical or elasto-optical tensors) is qualitatively understood, but sufficiently accurate quantitative data for fitting ellipsometry data of strained Si channels is lacking. When only considering the UV portion of the ellipsometry spectra, there is some hope in the capability to determine the gate oxide thickness, at least for sufficiently smooth surfaces. For rougher surfaces, there is an additional source of error, since surface roughness enters the ellipsometry analysis in a similar fashion as the native or gate oxide. For accurate gate oxide metrology, the Si surface roughness should be an order of magnitude less than the gate oxide thickness. This is satisfied for bulk Si starting materials but may cause concerns for measurements on strained Si channels. Confinement effects in the thin Si channel are not yet an issue in the visible and UV portions of the ellipsometry spectra. In principle, ellipsometry should not only be able to determine the Si channel thickness but also the Ge content of the SiGe buffer underneath. In practice, however, the Ge content determined from ellipsometry data is much too low, possibly due to ignoring the strain effects on the Si dielectric function. On pseudomorphic Si/SiGe heterostructures, ellipsometry is much more successful.

X-ray reflectivity is an attractive alternative to spectroscopic ellipsometry to determine strained Si channel thickness since the refractive index for X-rays is very close to 1 and does not depend on stress. For Si channel thicknesses of the order of 10–20 nm, a clear series of interference fringes (sometimes accompanied by an additional large-angle peak of unknown origin) is obtained. However, determining the Si channel thickness using commercial software fitting

packages does not always yield the correct value (in comparison to TEM). Possibly, this is related to surface roughness that is more difficult to handle for X-ray reflectivity than for spectroscopic ellipsometry because of the smaller wavelength. Experimental concerns about X-ray instrument reliability and alignment are similar to those described for measurements on high-κ gate dielectrics. High-resolution triple-axis X-ray diffraction has been used successfully (using lab and synchrotron X-ray sources) to determine the vertical Si lattice constant in the channel, another measure for the stress in the structures. In addition, resonant reflectivity measurements of DSA material can be done using synchrotron X-ray sources[224, 225].

Several microscopy methods are in the research and development phase. These include the point projection microscope (electron holography) and low-energy electron microscopy. Low-energy electron microscopy has been used to study surface science for several years. The application of this method to materials characterization and possibly to in-line metrology needs to be studied. A discussion of these methods is provided in the Microscopy Section of the Metrology Roadmap.

One of the five long-term difficult challenges for metrology is structural and elemental analysis at device dimensions. Fulfilling this need will require developing materials characterization methods that provide maps of elemental or chemical distributions at an atomic scale in three dimensions. 3D Atom Probes[193, 226] and similar methods hold the promise of providing atom-by-atom maps for small (50–150 nm diameter) needle-shaped samples that may be prepared by FIB lift-out techniques. LEAP technology needs further method and data analysis development, and currently has difficulties in measuring non-conductive and heterogeneously conductive structures with both conducting and non-conducting features. One challenge will be obtaining near 100% detection of each element during data acquisition. Electron tomography is a growing region of interest and is being pursued by both tilt-series and focal-series methods in both STEM and TEM. Aberration-corrected TEM currently shows promise in this area as smaller and more intense probes may allow increased resolution and signal-to-noise required for tomographic analysis.

5.9. Metrology for Emerging Research Materials And Devices

This section covers the materials and device characterization as well as in-line measurement needs for emerging materials and devices. Considerable progress has been made since the last update to the roadmap. This section of the Metrology Roadmap complements the cross-cutting Metrology needs described in the ERM roadmap by describing the status and research needs for many key measurement methods. This section is divided into sub-sections on 3D Atomic Imaging and Spectroscopy, other Microscopy needs including Scanned Probe Microscopies, Optical Properties of Nanomaterials, and Electrical Characterization for Emerging Materials and Devices.

5.9.1. Comment on the Impact of Nanoscale Dimensions on Metrology

One of the most overlooked challenges in metrology is the need for nanoscale materials properties. The materials properties used to measure process variation not only change at the nanoscale but are themselves altered by surrounding materials. These changes include optical properties (complex refractive index), carrier mobility, and numerous others. For example, the optical properties of the top layer of SOI are thickness-dependent below 10 nm. Furthermore, recent data have shown the optical properties depend on layers deposited above the top SOI film. This dimensional and materials stack dependence points to the need for developing databases of these properties with entries for critical materials stacks. In some instances, it seems that both carrier and phonon confinement impact numerous properties including dielectric function (complex refractive index), carrier mobility, and thermal transport.

5.9.2. 3D Atomic Imaging and Spectroscopy

5.9.2.1. Aberration Corrected TEM and STEM w/ELS

Aberration-corrected lens technology has revolutionized transmission and scanning transmission electron microscopy. Commercially available TEM and STEM systems have demonstrated sub 0.1 nm resolution and electron energy loss spectra have located atoms in an atomic column. Aberration-corrected STEM systems are approaching 3D atomic resolution as increased convergence angles reduce the depth of focus. This technology has already been applied to nanotechnology. Recently, single-layer graphene has been imaged along with defects in the stacking configuration of multilayer graphene[227, 228]. Some of the achievements of aberration-corrected electron microscopy of nanotechnology include:

Imaging of single-layer graphene, layer corrugation, and defects.

ELS spectra of a single Sr atom in an atomic column of $CaTiO_3$

Imaging both K and I atoms of a KI crystal inside a carbon nanotube

Observation of the movement of atoms in nanodots

- Observation of the relationship between the gold atoms in the nanodot gold catalyst and a silicon nanowire.

Advances in *image and spectral modeling* will enable the full potential of aberration correction and associated advances such as energy filters for the electron source and higher energy resolution/electron energy loss. Multi-slice simulations are already being modified for nano-dimensional materials and other applications. These first simulations indicate that the observation of twinning defects in nanowires requires the use of multiple angles of observation. The impact of nano-dimensions on electron diffraction patterns is also interesting. Microscopy of carbon-containing samples has moved beyond carbon nanotubes into single-layer graphene. Despite all of the above-mentioned advances, microscopy of soft matter remains exceedingly difficult as bonds are more readily broken in molecular samples. Higher energy resolution for ELS is critical to understanding molecular samples.

5.9.2.2. 3D TOMOGRAPHY AND 3D ATOM PROBE

See the section on Trends in Nanoscale Tomography.

5.9.3. OTHER MICROSCOPY NEEDS INCLUDING SCANNING PROBE MICROSCOPY

Assumption—There is a need for characterizing the structure and local properties of current CMOS devices as they scale down in size, as well as for anticipating the metrology requirements of post-CMOS device technologies.

5.9.3.1. PROBES OF LOCAL PROPERTIES WITH HIGH SPATIAL RESOLUTION: OPPORTUNITIES

Scanning Probe Microscopy (SPM) is a platform upon which a variety of local structure/property tools have been developed with spatial resolution spanning 50 nm to 0.1 nm. Scanning Capacitance Microscopy, Spreading Resistance Microscopy, Conductive Atomic Force Microscopy, and Scanning Microwave Impedance Microscopy have been optimized for dopant concentration profile measurement[195] with spatial resolution dependent on dopant concentration. Recent developments in SPM involving frequency-dependent signals on the sample and tip, and simultaneous perturbation with more than one frequency and/or probe expand the range and resolution of measurements.

Local Measurements Related to Charge and Transport – It is increasingly important to characterize devices in situ and during operation, particularly as a function of frequency. Scanning Impedance Microscopy and Nano Impedance Spectroscopy span 8 orders of magnitude in frequency to quantify interface and defect properties, including charge trapping. Individual defects in molecular nanowires can be detected with these tools, as well as local contact potential. Scanning Surface Potential Microscopy (also called Kelvin Force Microscopy) can easily map work function variations at the tens of nm scale and can be exploited to characterize FET and interconnect structures. There is recent evidence that the spatial resolution of this technique can be extended to atomic scales. Surface potential variations on high-κ dielectric films can be characterized providing insight on interface properties both before and after metallization with a high energy and spatial resolution. Recent SPM observations of quantum dots demonstrated single electron detection indicating the potential for increased energy resolution in highly specialized environments.

Local Measurements Related to Spin – A scanning probe tool, Magnetic Resonance Force Microscopy, has recently demonstrated the detection of single spins with magnetic probes. Further development will determine limitations on spatial resolution and the potential to study spin polarization and characterize spin-based devices. At lower sensitivity, Magnetic Force Microscopy can be used to map current flow through devices. To be generally useful the limits of field detection and development of standardized commercially available magnetic tips are required.

Complex Properties – Future generation devices will likely involve wider materials set, perhaps including organic and biomolecular constituents, and require additional property measurements. Utilizing high frequencies in various detection configurations yields local dielectric constant, electrostriction, piezo-electric coefficient, switching dynamics, etc. These measurements are critical in the development of capacitor-based memory and for hybrid device structures, as well as dielectric characterization.

Multiple Modulation and Combined Probes – The combination of multiple measurements is sometimes necessary to isolate properties and is sometimes useful to maximize information. For example, electrostatic interactions that occur during magnetic force measurements can be incapacitating. By measuring surface potential at high frequency, nulling it, and measuring magnetic forces at low frequency, the interactions are separated and quantified. This approach can be applied to produce generalized metrology tools.

5.9.3.2. PROBES OF LOCAL PROPERTIES WITH HIGH SPATIAL RESOLUTION: CHALLENGES

The challenges are implementing these tools on increasingly miniaturized active devices and complex materials systems in an industrial environment and time scale.

General Accessibility—The time it takes to bring a metrology capability from lab development to commercialization results in a large gap between capability and accessibility. In some instances, the design timeline is on the order of 6 years. This is particularly critical now since device research is encompassing new materials for high-k dielectrics, exploring alternative geometries, and looking toward post-CMOS technologies. Other mechanisms of accessibility are necessary to meet roadmap requirements.

Increased resolution—In the era of shrinking electronics, a trend toward higher spatial resolution is desirable. For some SPM tools, fundamental principles will limit ultimate resolution. Other tools are so new that limits have not been examined. Recent results in Scanning Kelvin Probe Microscopy suggest that atomic-scale resolution is possible for some of the complex property probes. If so, new physics will emerge, and theory will be required to interpret the output. There is a potential to increase the energy resolution of most of the measurements, as demonstrated by inelastic tunneling and single electron detection. The maximum energy resolution will be achieved at low temperatures, which is a trade-off with throughput and convenience.

Tip and Cantilever Technology—Commercial vendors have developed a large toolbox of specialized SPM cantilevers and tips. Reproducibility is often an issue; in some cases, yields of good tips are on the order of 30%. More important is the gap between commercially available cantilevers/tips and those required for tool development[229]. This becomes more difficult as the tips envisioned for tool development involve embedded circuitry and complex tip geometries[230, 231].

Calibration Standards—The lack of calibration standards for nm-size physical structures is a significant problem. At high spatial resolution and under specialized circumstances, atomic structure can be used. Carbon nanotubes have been suggested as a general alternative and can be used for electrostatic property calibration as well. Standard calibration processes should continue to be developed at the nanometer length scale[232-235].

5.9.4. OPTICAL PROPERTIES OF NANOMATERIALS

The optical properties of nano-scale crystalline materials, especially semiconductors, are modified by quantum confinement and surface states. The fundamental expression of the optical response of a material is its dielectric function. The imaginary part of the dielectric function is directly related to the absorption of light. For both direct and indirect band gap materials, the optical response is characterized by critical points where electrons are excited from the top of a valence band to the conduction band. Certain transitions have a strong excitonic nature. These transitions change as one moves from bulk to thin film to nanowires and then nano-dots.

The symmetry of a bulk sample strongly influences both the band structure and the joint density of states. Quantum confinement in one, two, or three dimensions changes the energy of the critical points and the joint density of states. Thus, the shape of the imaginary part of the dielectric function of nano-sized materials is altered by the change in the joint density of states and the appearance of new critical points due to the confinement. One interesting example is the emergence of strong anisotropy in silicon nanowires less than 2.2 nm in diameter and the theoretical prediction of new absorption peaks for light polarizations along the wire axis[236]. The nature of optical transitions with a strong excitonic nature is not well understood, and further theoretical and experimental work is required to understand the role of excitons in nanoscale materials.

5.9.5. ELECTRICAL CHARACTERIZATION FOR EMERGING MATERIALS AND DEVICES

Many emerging nanoelectronic devices exhibit non-conventional behavior such as negative differential resistance and hysteretic switching[237-239]. New electrical measurement methodologies and analyses will be required to characterize the behavior of these new emerging materials and devices. Certain traditional parameters, such as mobility, are much more challenging to extract at the nanoscale[240]**.** It is important to determine what parameters determine final device performance for a given emerging device technology. In addition, the behavior of some categories of emerging devices is based upon completely different mechanisms than those in traditional CMOS. For example, certain devices intrinsically have quantum mechanical behavior, while others do not utilize charge transport to change the computational state, but rely upon other mechanisms such as magnetic flux changes. Salient device parameters and their extraction methods will need to be defined for such new devices that switch by different physical principles than standard MOSFET structures. Methodologies will need to be established to characterize the stability and reliability of new device structures and circuit architectures. In contrast to the inherent macroscopic canonical

assembly average character of I-V curves, new metrology that probes atomistic fundamental properties of the materials of construction are needed. For example, microwave-based techniques, such as Broadband Dielectric Spectroscopy (BDS) and Scanning Microwave Spectroscopy appear to afford such capability[241, 242].

In addition to advances in electrical test methodologies, viable test structures are critically needed to reproducibly measure nm-sized interfacial elements (such as individual molecules and nm-sized semiconductor quantum dots) incorporating larger electrodes and leads that can be electrically contacted by probes or wire bonds. Methods to contact sub-lithographic components of emerging nanoelectronic devices are perhaps the greatest challenge for the electrical characterization of emerging materials and devices. Furthermore, parametric test structures need to be developed that interrogate the interface between metal interconnect and the active region of nano-scale devices, especially those fabricated with organic materials. Parameters such as work function, barrier height, and transport processes need to be investigated and defined for devices fabricated with unconventional materials.

5.10. Reference Materials

Reference materials are physical objects with one or more well-established properties typically used to calibrate metrology instruments. Reference materials are a critical part of metrology since they establish a "yardstick" for comparison of data taken by different methods, by similar instruments at different locations (internally or externally), or between the model and experiment. Reference materials are also extremely useful in testing and benchmarking instrumentation.

There are two basic kinds of reference materials:

1. A reference material can be a well-calibrated artifact that gives a reference point for the metrology under test.
2. Another equally important reference material tests how accurately the tool under test (TuT) measures a key process control parameter. The most relevant reference materials are products that come from the manufacturing process. The TuTs are designed to measure a feature of a given product such as linewidth accurately, for example. This product contains subtle but important process changes that may affect measurement accuracy. It is the responsibility of the metrologist to understand the important process variations that can be difficult to measure by the TuT and to incorporate them into a meaningful set of test artifacts. These test artifacts must then be accurately measured with an appropriately qualified and documented reference measurement system.

Reference materials of the first kind can be obtained from a variety of sources and come in a variety of forms and grades. These types of standards are important and useful, but they tend to be limited in their usefulness because of a limited likeness to the customers' manufacturing process and the lack of relevant induced process variations. Depending on the source, they may be called Certified Reference Materials (CRM), Consensus Reference Materials, NIST Traceable Reference Materials (NTRM®), or Standard Reference Materials (SRM®).[3] The US National Institute of Standards and Technology (NIST) is one of the internationally accepted national authorities of measurement science in the semiconductor industry. Commercial suppliers can also create and submit calibration artifacts to a rigorous measurement program at NIST for the purpose of developing an NTRM; reference material producers adhering to these requirements are allowed to use the NTRM trademark for the series of artifacts checked by NIST.[4]

Another approach is the measurement certification of reference materials through interlaboratory testing under the supervision of recognized standards developing bodies, such as ASTM International. The National Metrology Institutions (NMI) in different countries develop and maintain standards that might be suitable and should be consulted. There is an effort among many of the leading NMIs, including NIST, to coordinate cross-comparisons of their measurements and standards to arrive at a mutual recognition sometime soon to avoid duplication of efforts.

There are several technical requirements related to reference materials of the first kind and their measurement certification, as follows:

Reference materials must have properties that remain stable during use; both spatial and temporal variations in the certified material properties must be much smaller than the desired calibration uncertainty.

3 NTRM® and SRM® acronyms are registered trademarks of NIST
4 Use of the NTRM mark on a subsequent series of artifacts, even of the same type, requires additional verification testing by NIST

Measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. In some areas of metrology, no current method of measurement is adequate for the purpose. When the basic measurement process has not been proven, reference materials cannot be produced.

The final measurement uncertainty in an industry measurement employing a reference material is a combination of uncertainty in the certified value of the reference material and additional uncertainties associated with comparing the reference material to the unknown. For this reason, the uncertainty in the reference material must be smaller than the desired uncertainty of the final measurement. An industry rule of thumb is that uncertainties in the certified value of the reference material be less than ¼ of the variability of the manufacturing process to be evaluated or controlled by the instrument calibrated using the reference material.

- For applications where accurate measurements are required (such as dopant profiling to provide inputs for modeling), the reference material attribute must be determined with an accuracy (including both bias and variability) better than ¼ of the required final accuracy of the measurement for which it will be used.

Additional training of process engineers in the field of measurement science is essential to avoid misuse of reference materials and misinterpretation of the results obtained with their use.

5.11. 3D Nanometrology Needs and Challenges

The simultaneous decrease in feature dimension and increase in 3D structural complexity of advanced device architectures is imposing daunting challenges to the semiconductor metrology community. In fact, the need for better electrostatic control has led to fully depleted silicon-on-insulator (FDSOI) devices as well as the replacement of relatively planar structures with devices with much greater topological complexity such as FinFETs, tri-gates, gate-all-around structures or even stacked gate all-around-structures[243, 244]. For instance, evaluation of structural parameters of 3D shapes requires measurement of many parameters beyond traditional CD, including sidewall angle, top corner rounding and footing, roughness, recesses, and undercuts. Now all are indispensable, as are thin film parameters such as thicknesses on horizontal and vertical surfaces, compositions, dopant distributions, strains, and other parameters and materials properties within device structures. Future 3D memory devices will also include multiple gate-level structures defined by HAR trenches and holes in multilayer stacks with as few as 4 alternating gate/dielectric periods, but possibly as many as 256. The lack of suitable metrology of HAR features is currently a major gap, as in-line non-destructive methods do not have the needed sensitivity and resolution to image or measure CD, depth, profile, or contamination at or near feature bottoms[81]. Furthermore, these problems are compounded by the very small dimensions of the devices, where only a few atoms yield extremely small signals, and by limited sample resilience, random distributions of dopant atoms, non-uniform nanometer-scale strain fields, and quantum confinement effects. Thus, 3D characterization at sub-nanometer and maybe atomic resolution levels is increasingly required to understand the physics of devices controlled by surface and interface effects, and such characterization will become critical for process development if not high-volume manufacturing.

Today, advanced devices are characterized at the nanometer level, with mainly offline, TEM-based techniques such as NBD, dark field holography, EELS, etc. However, the intrinsic 2D cross-section information (or projection) of all these techniques is not complete since the assumption of conservative information through the third dimension is no longer applicable. This makes it difficult to use 2D information to extend to the 3D parameterization of the devices. Thus, some new approaches like tomography reconstruction will need to be implemented. All the above-mentioned techniques bring about issues with sample preparation and characterization yield due to the increased number of off-line characterizations and with the link and balance between in-lab and in-fab metrology.

TSOM is inherently a 3D metrology method. It has been applied to study 3D shape of sub 40 nm features. From simulations and limited measurements, the TSOM method shows promise for 3D shape metrology but needs further study beyond simulations for applications in production[213].

In the following section, an overview of the state-of-the-art of promising techniques for nanometrology is presented, along with their potential for tomography 3D information reconstruction. Also, the need to combine the different 3D information, linked to die-level and wafer-level maps for HVM metrology control, will be discussed.

5.11.1. 3D Nanoscale Characterization of Single Devices

There are basically three approaches to mitigate the 3D complexity: true 3D imaging techniques, 3D reconstructions from 2D images, and simplified test structures designed to enable the extraction of 3D information from several 2D measurements.

5.11.1.1. STRUCTURAL: (DIMENSIONAL, CRYSTAL QUALITY)

To get access to structural properties at the device level, TEM-based techniques have the advantage of easy positioning for local analysis. TEM is widely used to accurately measure device dimensions due to its excellent, sub-0.05 nanometer resolution while scanning electron microscopy (SEM) has a resolution limited to approximately 0.5 nm. Focused ion beam (FIB) technology allows the preparation of thin lamella or tip-shaped samples of a specific device from a cleaved/diced or a full wafer[245]. With these two types of sample preparation, it is possible to use high-resolution (S)TEM imaging for 2D structural analysis at the atomic scale, or electron tomography to measure the dimensions of the 3D architecture of the advanced nodes. Moreover, with the recent development of parallel nanobeam diffraction (NBD) and electron precession, mapping of crystal orientation (e.g., copper interconnection lines) is possible with an increased spatial resolution (around 3 nm). Even if there is now an industrial solution with FIB systems to be able to automatically prepare and extract samples for TEM imaging, and use dedicated imaging software, usually the technique is time-consuming and site-specific, with lamella that are 100 nm thick and a few μm long[246].

FIB/SEM 3D refers to the acquisition of high-resolution scanning electron microscopy (HRSEM) images combined with FIB slicing. Today's state-of-the-art has been shown with a volume of an array of 22 nm node transistors. Despite its potential, some problems still need to be solved. The resolution of the reconstructed volume depends strongly, but not only, on the SEM resolution. In addition, such metrology is very time-consuming and might present a problem of low success rate due to sample drift and tool instability over a long period of time. Software solutions already hit the market to partially overcome this problem, but for a reliable in-line 3D metrology with SEM, dedicated equipment still needs to be designed.

Atom probe tomography (APT) is particularly well suited for measuring composition at the atomic scale in semiconductor devices. The ability to detect all elements with detection limits as low as 10^{17} atoms/cm^3, for B in Si host makes it an attractive technique. The sample must be prepared as a tip shape, e.g., by FIB milling, to enable laser-assisted field evaporation. Placing a complex transistor structure at the end of an atom probe tip may be challenging, but in most cases is possible by a skilled FIB user. The tip shape and field evaporation impose an analyzed volume of, typically, some 80 nm × 80 nm × 200 nm, which although small, matches well with current and future device dimensions. Although reconstruction image distortion is a key error source, the use of *in situ* TEM or SPM could help reduce such errors[247].

Analytical TEM allows identification, and in some cases, quantification of elements to an atomic resolution with C_s aberration correctors[248] but with a lower sensitivity than APT or secondary ion mass spectrometry (SIMS)—around 1%. Electron energy loss spectroscopy is traditionally well suited to analyze lighter elements, with energy-dispersive EDS for heavier elements, but EELS is the only technique able to differentiate the chemical bonding of probed elements. Recently the speed of spectral acquisition has been increased with the development of silicon drift detectors (SSD) for EDS, and the time to acquire elements or bonding states has been dramatically reduced (by a factor of 10 or more) with fast electronics for EELS imaging filters also. Thus, as far as analytical electron tomography is concerned, the results now are encouraging[249].

5.11.1.2. PHYSICAL: (STRAIN, STRESS, ELECTRICAL)

True 3D imaging techniques include coherent X-ray diffraction and small-angle X-ray scattering. For coherent X-ray diffraction, the use of coherent X-rays simplifies the phase problem of inverse Fourier transforms and permits the extraction of 3D scattering features from the recorded intensity of their diffraction patterns. SAXS in transmission at multiple angles can provide full 3D information but provides the average of feature geometries over the X-ray spot size. However, as of today, only synchrotron facilities can provide this kind of analysis[250, 251]. (*See the Lithography Metrology section for a description of CD-SAXS*)

TEM techniques for 2D strain measurements are now available, depending on the instrument's performance and stability and on the area to analyze: dark-field holography (3–10 nm resolution and a sensitivity of ± 0.06%)[252], Nanobeam electron diffraction (NBED) (3–6 nm resolution and an excellent sensitivity of ± 0.02%), high-resolution TEM and now STEM high angle annular dark field (HAADF) with geometrical phase analysis (1 to 5 nm resolution and sensitivity of ± 0.1%)[253] and convergent beam electron diffraction (1 to 5 nm resolution and excellent sensitivity of ± 0.02%). Today, NBED in precession mode (N-PED) seems to provide the best combination of spatial resolution, sensitivity, and robustness from artifacts. In addition, it is very insensitive to thickness variations in the specimen, and thus time-consuming preparation techniques such as backside milling are not required. The experiment and processing can take between a few minutes to several hours depending on the size of the map acquired. This will speed up in the future by improvements in imaging cameras and real-time data processing. Currently, NPED is not widely available in electron microscopes using the imaging capabilities of the CCD camera. However, it is possible to use a

commercially available off-axis television camera to measure the positions of the diffraction spots for deformation mapping and a sensitivity of 0.03% and 4 nm spatial resolution has been reported on a pre-aberration correction generation microscope[254]. The challenge is to have well-controlled sample preparation to achieve good reproducibility of measurements[255]. In addition, more precise quantification of the metrology performances (accuracy and precision) should be discussed[256,257]. (*See the section on Strained Si Processes*).

Electrical tomography using scanning spreading resistance microscopy (SSRM) has been recently developed[191, 258]. It is an emerging solution to address 3D carrier mapping. The methodology consists of using an AFM probe to remove material by successive scanning and to record at every scan the 2D carrier map, similar to a slice-and-view methodology. The resulting stacked images are interpolated and are used to generate a 3D. This method requires a hard-conductive probe (such as a full-diamond tip) to ensure material removal without significant damage to the probe. This approach has been highlighted in carbon nanotube-based interconnects and various emerging memories. By increasing the accuracy in the tip-induced material removal, sub-nm removal rates have been obtained leading to the characterization of volumes in the order of 100 nm^3[259]. This approach is referred to as scalpel SPM and has been used for the experimental observation of conductive filaments in integrated resistive switching devices, thus enabling the 3D characterization of confined volumes in oxides such as Al_2O_3 and HfO_2 with removal rates between 0.2–0.5 nm/scan[260, 261]. The fast Fourier transform-SSRM (FFT-SSRM) appears also as an emerging method to image highly doped samples[189]. By modulating the load force applied to the tip, only the contribution of the spreading resistance is measured[189]. This is extracted by an FFT-based lock-in deconvolution method. This approach has been recently illustrated for a FinFET structure with a highly doped (1–4 mΩ.cm) raised source/drain region. In this example, FFT-SSRM allows to detect the highly doped SiGe and the undoped Ge regions without saturation induced by parasitic resistance as obtained with the standard SSRM technique[190, 262].

5.11.2. TRENDS IN NANOSCALE TOMOGRAPHY

All the above-mentioned techniques have been developed at different length scales for morphological, chemical, electrical, and structural imaging, and their 3D characterization capabilities are to a large extent based on tomography. Important tomographic techniques for 3D imaging at microscopic and nanoscopic length scales are:

X-ray tomography

FIB/SEM 3D

TEM/AFM

Electron tomography

- Atom probe tomography

In any case, sample preparation is crucial; experimental techniques and sample preparation methods for tomography are both reviewed elsewhere[263]. Hard X-ray nano-tomography at 20 nm resolution may now come of age, as it is an ideal technique because it has the potential of non-destructively providing high-resolution images of buried devices. However, because of physical constraints, no commercial system exists that simultaneously allows for high resolution (100 nm or less), penetrating X-rays (15 keV or more), and high throughput, and the technique is currently confined to 3rd generation synchrotron sources. Commercial systems can either accommodate high resolution at low energy or medium resolution at high energy in the case of large samples[231]. The construction of dedicated nanoelectronics synchrotron end-stations for 3D imaging is currently the only solution to get routine and fast access to the technique[264].

Electron tomography using STEM-HAADF contrast is now a routine and mature technique operating at about 1 nm resolution for those samples having a cross-section of 100 nm or less[216, 265-267]. Atomic resolution has been proved[268] but on simple, isolated objects like nanoparticles. Obtaining atomic resolution on complex objects is a real upcoming challenge, which could be overcome by improving the overall stability of the microscopes, optimizing the depth-of-field, the sample preparation (which is crucial, yet time-consuming), and data pre- and post-processing, presumably with machine learning (ML) and artificial intelligence (AI).

FIB/3D SEM is a technique of choice: it allows for relatively high-resolution (20 nm–50 nm) investigation of large objects with different contrast modes simultaneously, in such a way that the 3D sample shape, chemical composition, and even crystalline distribution can be retrieved[269, 270]. Neither X-ray tomography nor electron tomography can provide all this at the same time at such a resolution. It requires limited sample preparation (no need to prepare needle-like samples) but is destructive: this is not a severe limiting issue in nanoelectronics except for those cases where imaging modalities need to be cross-correlated. However, the method is still time-consuming and can be limited by

drift issues, but so far it offers the best compromise among price, information, time, resolution, and sample size. One could think of a cluster of dedicated dual-beam systems for automated 3D high-throughput analyses. For compositional analysis, such cluster systems could include both EDS and SIMS detectors.

Recently, TEM and AFM have also been combined for 3D imaging beyond topography. Using the 3D analysis capability of scalpel SPM and a dedicated TEM sample preparation, nm-resolved 3D electrical and chemical analysis of Si- and Ge-based structures for sub-20 nm technology nodes have been studied[271]. This method is destructive, and it requires a sample preparation comparable to FIB/SEM. However, for site-specific studies such as failure analysis, this approach can be extremely effective in offering a solution to sense multiple material properties by using the entire spectrum of different AFM modes including electrical and non-contact. In addition, microwave tomography, e.g., electro-capacitive tomography (ECT), may be useful in the visualization of subsurface defects; however, the data processing requires situation-specific algorithms and numerical models.

The 3D Atom Probe or Atom Probe Tomography (APT) is an advanced version of a field ionization microscope combined with a mass spectrometer capable of atom-by-atom three-dimensional reconstruction of a small needle-shaped sample. The sample may be prepared from a device-specific site by chemical or plasma etching, or focused ion beam lift-out techniques similar to those commonly used for TEM sample preparation. In the 3D Atom Probe experiment, a needle-shaped sample is placed near an electrode and a strong applied field ionizes atoms from the sample tip, ejecting atoms from the sample, and accelerating them through a position-sensitive mass spectrometer. The original position of atoms in the sample is determined from geometric considerations and the atomic mass is determined from the time of flight. 3D Atom Probe provides a means of measuring the atomic arrangement of free-standing wires allowing a method to characterize doping density in nanowires.

APT is the most spatially-resolved mapping technique, featuring 0.1–0.3 nm resolution [272-274]. While not as mature as some of the techniques discussed above, the results are obtained from extremely small volumes (100 nm^3). However, the wide variety of materials now used in advanced devices complicates atom probe analysis because the evaporation field is different for each material and these differences lead to artifacts in the reconstructed volume, but progress has been made with the addition of laser pulsing.

Overall, APT brings us closer to the dream of atomic mapping in three dimensions. Current detection efficiency is approximately 80% of the atoms ionized and there has been much progress in developing an understanding of local field effects that affect resultant 3D models. It must be emphasized that it is not enough to know just the position, identity, and chemical nature of all atoms in a material; it must be accompanied by microstructural information to discern the materials' properties and behavior. Thus, synergy is expected between the experimental determination of atom positions, identities, and chemical nature and computational material science to obtain the optimum utility of APT[226].

These reconstruction artifacts limit the accuracy of APT composition profiles, and the data requires careful calibration by other techniques, such as TEM and electron tomography. As the sample preparation for APT is similar to electron tomography, one interesting possibility is to perform electron tomography and then APT on the same sample, allowing the APT volume to be corrected using the morphology measured by electron tomography. These types of measurements can also be correlated with other measurements (SPM[195], SIMS, etc.), combining the advantages of measuring many devices at once with nm-scale compositional measurements in 3D. The uptake of atom probe tomography for semiconductor analysis is increasing and with future improvements in detectors, reconstruction algorithms and tip shape monitoring will become an increasingly essential tool.

The emergence of the related technique of FIB/ToF-SIMS tomography allows complementary (better detection of light elements, isotopic information) chemical information with respect to FIB/SEM-EDS to be acquired[275]. Both serial sectioning techniques can be combined with X-ray nano-tomography to assist in targeting the region of interest and in reducing artifacts.

The accommodation of the operando experiment is illusory so far, but ex-situ or even in-situ experiments may be doable using X-ray probes. A generic technique does not exist, and the choice of the tomographic probe is largely sample-dependent; however, dual beam FIB-SEM serial sectioning gives a satisfying trade-off provided samples are not precious. For high-throughput 3D nanoscale characterization, the tools need to be more stable, more user-friendly, automated, more flexible, and versatile. It must also be emphasized that sample preparation is crucial for each of the discussed techniques.

5.11.3. HYBRID METROLOGY

It seems inevitable to use more than one type of measurement, tool, and method, and take advantage of the rich, multi-faceted set of data by combining the most reliable information gained from each source. This combined (complementary, hybrid) metrology would be necessary for sub-10 nm dimensional metrology. Hybrid metrology has shown promising advantages in significantly reducing the overall uncertainties, i.e., augmenting the confidence in the results, and in the optimization of various complementary measurement methods for cost[121, 160, 276-280]. More specifically, 3D data acquired for dimensional metrology will need to be compared and merged to that coming from other parameters (e.g., chemical, strain, electrical). In this sense, correlative microscopy recently has shown the advantages of such an approach while characterizing nano transistors[281]. They will not necessarily have the same resolution, as they will come from different tools. Therefore, modeling data analysis and treatment algorithms to merge data will need to be tested to ensure against artifacts resulting from the stitching/merging process.

Both CD-SAXS and GI-SAXS could be used to improve optical scatterometry through combined or hybrid measurements. Often there are high correlations between model parameters used in optical scatterometry or parameters to which optical scatterometry is insensitive. Deeper layers or buried metal layers are often opaque to optical metrology techniques but can easily be measured by CD-SAXS or GI-SAXS. Parameters that are easily measured using a small amount of SAXS data such as multiple patterning errors can be incorporated into the optical models, improving the optical measurements and reducing parameter correlations, while maintaining a high throughput measurement. 3D-AFM data[282] is already used with both SEM and scatterometry[121, 160, 283] but given the intrinsic capabilities of probe microscopy, a 3D-AFM with material contrast would be a good hybrid tool. Certainly, some feedback with sample preparation will be needed to avoid or diminish such artifacts and accomplish the ultimate goal of complete 3D information describing the device properties. Additional efforts are needed in quantifying uncertainty and error analysis in combined metrology where data fusion from different instruments is non-trivial. As the technique gets widely adopted, a common evaluation guideline for uncertainty on combined metrology would be needed.

An application of combined metrology is the Reference Measurement System (RMS), where one of the instruments provides traceability to the others. An RMS could be a single instrument or a set of several instruments. An RMS is well characterized using the best the science and technology dimensional metrology can offer, applied physics, sound statistics, related standards, and proper handling of all measurement error contributions based on the best protocols available. Because an

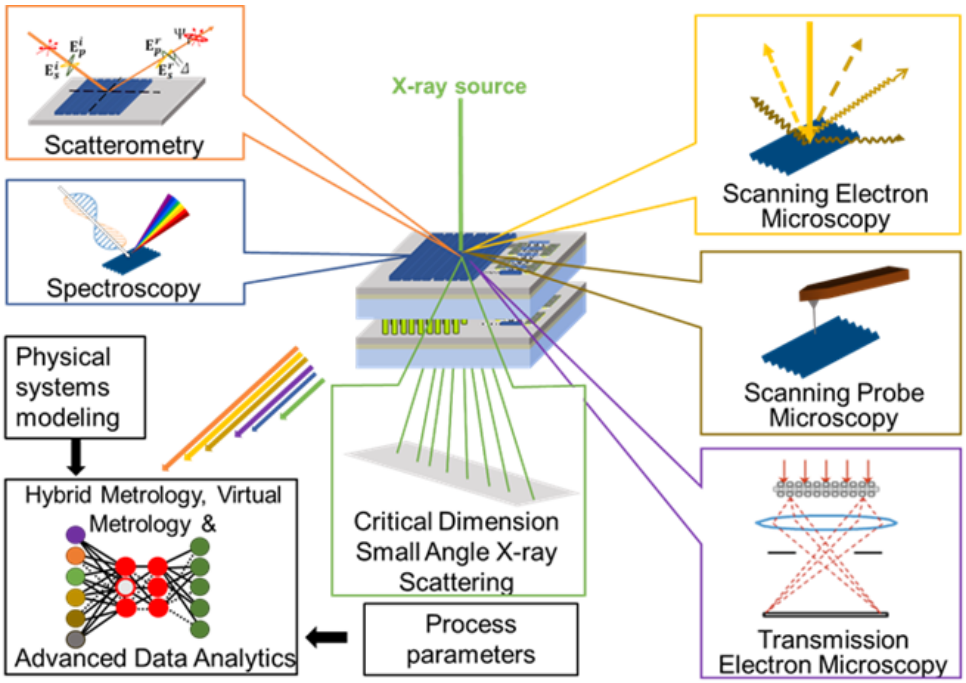

Figure MET7 A Multiple Techniques Approach to Device Metrology

RMS has been well characterized, it is more accurate, perhaps by an order of magnitude, and more precise than any instrument in a production fab[278]. An RMS must be sufficiently stable that other measurement systems can be related to it. An RMS can be used to track measurement discrepancies among the metrology instruments of a fab, control the performance and matching of production metrology instruments over time, and introduce absolute traceability to the measurement process if desired. Due to the performance and reliability expected from this instrument, the RMS requires a significantly higher degree of care, scrutiny, and testing than other fab instruments. Through its measurements, this "golden" instrument can help production and reduce costs. The main difference between RMS and combined metrology in general is the relationship between the instruments. In other applications of combined metrology, each instrument is better suited for a specific measurand, but may not necessarily derive their traceability from the group. (*See the section on Measurement Uncertainty.*)

5.11.4. IN-LAB. VERSUS IN-FAB

For in-fab metrology, it is necessary to map nanometer-scale material properties over the entire wafer (e.g., optical properties, strain, critical composition), critical shape, and other critical functions. These properties are all measurable on conventional flat films, but the various properties in the device features often will not correlate well to those on traditional solid test pads; thus, many of these properties will need to be measured on complex 3D structures. When included within the more complex architectures that influence such properties, extracting these from among the many other unknown parameters will likely be difficult. As has been shown previously the only techniques available today for 3D nanometrology are more in-lab techniques. However, performing such metrology non-destructively is the ultimate challenge for cost-effective HVM[52].

Presently, the industry is using available traditional failure analysis laboratory techniques, but it is increasing the amount and speed of collected data through automation. The drawback of using such "brute force" methods is the obvious loss of wafers to further processing, which not only increases costs and cycle times for learning but also increases the uncertainty in the correlation between the measured properties and final device performances due to needs to compare results from different wafers. The industry must decide if this strategy is to be used in the long term; it might be feasible to build tools, which only damage a very small area on a wafer. This small region, after the measurements, can be neutralized to allow further processing. As indicated previously, such a tool would include milling and several imaging and analysis techniques bundled together. It would be expensive but might offer a solution for better 3D nanometrology at a lower cost per site with faster cycles of learning. While such a solution might not be ideally suited to HVM, if a truly non-destructive solution is not found to be feasible or possible, it could still offer a large improvement over the "brute force" methods in use now. Additionally, for many image-based tools, it is likely that high-resolution laser interferometry-based navigation and signal acquisition will be necessary.

There is a need to combine the nanometer scale information obtained in single devices with destructive and low-throughput, in-lab techniques with those with lower spatial resolution but non-destructive and high-throughput methods on representative test vehicles, e.g., device arrays inside die or inscribe lines (i.e., design for metrology) at wafer level. This will help to balance the need of nano- and atomically-scaled measurements of materials properties at development or in failure mode analysis with the needs of HVM metrology. It is also likely that, as with crafting the various devices, measuring them will also benefit greatly from the use of physics-based modeling to understand the coupling of the different scale information from nano- to macro-scale. This can considerably improve the measurements, both for throughput and for quality. Overall, formidable but surmountable 3D nanometrology challenges are ahead for the industry. Fortunately, partial solutions already exist, but a lot of work must be done to make future process development and production possible. We have entered a time when metrology is indispensable and a truly enabling part of integrated circuit production.

5.12. FACTORY LEVEL METROLOGY

The fundamental challenge for factory metrology will be the measurement and control of atomic dimensions while maintaining profitable HVM. In manufacturing, metrology is connected to factory-wide automation that includes database and intelligent information from data.

Off-line materials characterization is also evolving toward compatibility with factory-wide automation. All areas of measurement technology are being combined with computer-integrated manufacturing (CIM) and data management systems for information-based process control. Although integrated metrology still needs a universal definition, it has

become the term associated with the slow migration from offline to in-line and *in situ* measurements. The proper combination of offline, in-line, and *in situ* measurements will enable advanced process control and rapid yield learning.

A key aspect of meeting some of the factory-level needs outlined in the Difficult Challenges table would be the wider adoption of VM in the factory. Virtual metrology is defined by SEMI E133[284] standard as

> *"…the technology of prediction of post process metrology variables (either measurable or nonmeasurable) using process and wafer state information that could include upstream metrology and/or sensor data."*

The prediction of post process metrology variables using metrology and process information would help reduce cycle time, increase product quality, and reduce scrap. The introduction and familiarity of VM techniques such as smart sampling would help ensure that only the needed data is acquired. The next section is the Executive Summary of a white paper[47] on VM developed by the IRDS Factory Integration and Metrology Focus Teams in 2017. Although the landscape of virtual metrology is continually evolving, the key recommendations still hold true.

5.12.1. VM NEEDS

A white paper has provided an overview of virtual metrology (VM) and examined some of the issues preventing wider adoption of VM and offers some possible solutions [285]. . The key adoption issues identified in this white paper primarily came from a survey of advanced process control (APC) users, implementers, and managers, conducted by the International Roadmap for Devices and Systems (IRDS) Factory Integration focus team, to help understand the current state of VM adoption.

The main factors preventing wider adoption of VM include confidence in models, customer data quality, lack of process knowledge and correlation with metrology, model maintenance, cost, and intellectual property (IP) security. Possible solutions include the development of a standardized prediction quality metric, improved data communications and data quality for model building and model maintenance, better training data, correlation with real metrology when possible, and improved interaction between yield and VM, which will allow VM to leverage some of the metrology data that yield depends on. The whitepaper also describes some current and potential applications of VM.

The main recommendations from white paper makes include:

- *Standards are needed to evaluate customer data quality*. A set of criteria on the minimum level (type and completeness) of data required for VM models would be helpful. Although the wide range of current and possible applications preclude exact specifications, guidelines on how to select an initial data set would be helpful.

- *Standards or guidelines are needed on how to evaluate model quality and how to communicate model quality via a model quality metric*. Issues involving model quality are some of the key factors limiting VM model development and adoption. A model quality metric (or a number of possible metrics) will not only increase confidence in models but also provide governance for use and enhance model portability and reuse. A platform to host, maintain, and manage models would also be useful.

- *Where applicable, industry roadmaps should identify processes that could benefit from specific VM applications.* A wide range of processes could benefit from VM if there is a wider understanding of how VM should be applied and what benefits could be achieved. The development community and industry roadmap developers should highlight applications beyond the current ones that could benefit from VM. Use cases that clearly illustrate different applications should also be highlighted.

- *Solutions for VM model robustness and maintenance should be identified* Challenges with maintaining models in the face of process dynamics and context shifts should be identified along with potential solutions and a roadmap for implementation. The relationship between the model robustness and maintenance requirements for specific VM application types should be identified.

5.13. Outside System Connectivity

This section describes some of the key metrology issues identified by the Outside System Connectivity IFT. This is the first time OSC metrology issues are covered in the metrology roadmap, and the goal is to only highlight the key challenges. Future versions of the roadmap will provide potential solutions and capabilities.

5.13.1. Optical Interconnects: Heterogeneous Monolithic Integration

Optical Interconnects are a way to communicate information within and between chips using optical signals rather than wires. Part of the requirements for interconnect in general include high bandwidth, latency, and low power. Optical interconnects *"...promise ultra-high bandwidth, low latency, and great energy efficiency to alleviate the inter-rack, intra-rack, intra-board, and intra-chip communication bottlenecks in multiprocessor systems.*"[286] To meet the requirements of optical interconnects, heterogeneous monolithic integration with silicon components is required. Specific metrology issues involved with heterogeneous monolithic integration with silicon include:

Bonding InP to SOI (Quality of the bond)

Grating characteristics

Structures to couple radiation into waveguides

Grating structures to couple radiation into detector

GeSi (*Ge rich Silicon Germanium*) detector efficiency

5.13.2. Optical Interconnects: Optical Measurements

In addition to heterogeneous integration issues, optical interconnects need metrology to measure the optical characteristics of the signal. Preferably the metrology should be "*Minimally invasive*" so it could be used without disrupting the overall system. For optical interconnects to work, hundreds of optical signals would need to work in close proximity without crosstalk and interference. This requires *Precise wavelength measurement methods* to accurately characterize the wavelengths. Methods to test the *coupling efficiency* of the optical signal are also needed.

5.13.3. RF Device Fabrication

Radio frequency (RF) technologies as a means of outside system connectivity represent an expanding area for a wide range of systems. These include mobile communication and computing devices, and a host of wireless-enabled components and systems. As such, the production of RF devices is expected to increase exponentially. Specific metrology issues associated with RF device fabrication include:

Reducing contact resistance: correlating nanostructure to contact resistivity

- Group IV contacts
- III-V contacts

Heterogeneous monolithic integration of III-Vs on silicon

Measurement of complex layers for bipolar/CMOS

5.13.4. Characterization of Focusing Antenna Arrays (phased array antennas)

The proliferation of wireless devices means that there are more antennas in use today than at any other time in history. The quality of the signal depends to a large extent on the power and range of the antennas. In many applications, the antenna is directional. The metrology issues include the need to be able to *characterize broadcast direction and power during development*, and *reliability measure the reproducible direction and power*. This applies to both short and long-range antennas.

6. Potential Solutions

Potential solutions for some of the difficult challenges listed in Table MET-1 are highlighted throughout the chapter. Figures MET-2, MET-3, and MET-6 show potential solutions for Lithography Metrology, FEP Metrology, and Interconnect Metrology respectively for the "7 nm", "5 nm"," 3 nm", and "1.5 nm" node technologies. Most of the technologies shown extend through multiple years, this only means that they will be able to measure at least one parameter within the listed years. Figure MET-1 (in Section 5.3) shows a breakdown of the instrument capabilities based on feature size and applications. Only transmission small angle X-ray scattering (T-SAXS) is deemed capable

of measuring all the applications with feature size below 5 nm, however, more development needs to be done to adapt it for use in the factory.

Apart from instrument capabilities, enhancements to current instruments could help their adaptation to new technologies. Sections 6.1 to 6.4 list some improvements that cut across different technologies that would greatly improve the use of the instruments listed in Figure MET-1. These fall under two broad categories, 1) Combining different measurement technologies in ways that improve the usefulness of their results—3D metrology, hybrid metrology, and data analytics, and 2) Increased instrument range and resolution—improved instrument resolution, improved X-ray metrology and plasmonic assisted optical focusing.

6.1. Improved Instrument Resolution

Each technique shown in Figure MET-1 could benefit from an increase in resolution. Better resolution for current technologies such as CD-SEM, CD-AFM, and optical CD could help extend their application to smaller nodes or new device structures. Examples include, but are not limited to:

Introduction of aberration-corrected low energy SEM column

Utilization of high-energy SEM

Enhanced CD-AFM tip technology

High-speed AFM with multiple tips

Reduced spot size and uniform intensity for optical instruments.

Use of multi-column and multi-beam electron beam instruments for defect inspection

Increased use of data fusion or image stitching to increase range.

6.2. X-ray Metrology for Critical Dimensions and Films Metrology

As shown earlier in Figure MET- 1, CD-SAXS is the only technique that is currently viewed as having the capability to measure features less than 5 nm for applications such as 3D FinFET, Nanowire, and 2D/3D DSA. A limitation of SAXS is the lack of high-brightness sources for use in both laboratory and factory environments. As such, the availability of high-brightness sources would greatly improve the possibility of SAXS being available for sub-5 nm devices.

Specific examples include, but are not limited to:

An X-ray source with >100X brightness of conventional rotating anode sources can enable new techniques such as CD-SAXS and X-ray tomography, especially for logic applications.

Improved throughput and increased utilization of already-mainstream X-ray metrology solutions such as HR-XRD, XRF, TXRF, XRR, and XPS, among others.

Inelastic background quantitative analysis for addressing inter-diffusion phenomena at very deeply buried interfaces (<100 nm), development of automated, in-line compatible software solutions.

6.3. 3D Metrology

The examples shown in this section refer to enhancements that would help instruments acquire 3D information. These include:

Non-raster capabilities for scanning instruments—Currently, most scanning instruments acquire data in a raster or bi-directional manner that aligns with the instruments' orthogonal axes. This is inefficient as it leads to collecting excessive information that is not used in the analysis. A non-raster data acquisition strategy based on feature contours or a priori information would save time and allow the user to collect only the needed information. This would also allow the extraction of information from non-orthogonal axes.

Multihead/column for scanning instruments—The use of multiple instrument heads or columns has been proposed for metrology instruments. In addition to being able to acquire more data, each head could extract a different type of information (dimensional, material, etc.).

Hybrid Metrology—Increased use of a combination of instruments (hybrid or complementary metrology) to achieve the desired resolution, speed, or low levels of uncertainty needed to characterize different aspects of a feature.

6.4. Data Analytics

See the section on Emerging and Disruptive Technologies.

6.5. Sub Wavelength Imaging Techniques

See the section on Emerging and Disruptive Technologies.

7. Cross Teams

Within the IRDS, the Metrology IFT works with the More Moore, Lithography, Factory Integration, Emerging Research Materials, and Environmental, Safety, Health and Sustainability, and Outside System Connectivity IFTs. These IFTs help identify key issues in their area that could be addressed in the Metrology chapter.

7.1. More Moore IFT

More Moore refers to the continued shrinking of horizontal and vertical physical feature sizes to reduce cost and improve performance. (*See the More Moore chapter for additional information.)* As such, the Metrology IFT depends on the More Moore IFT for direction on projected device structures, sizes, channel materials, patterning technology, and a host of other manufacturing-related parameters. These are the support technologies outlined in the Overall Roadmap Technology Characteristics (ORTC), and other items as determined by both groups, including but not limited to FEP and Interconnect-related metrics. Some examples include information on starting materials, multilayer films, and three-dimensional control of interconnect features.

7.2. Lithography IFT

The Lithography IFT provides information on lithographic options that enable future semiconductor nodes. These include specific lithography and patterning targets and dimensions for a wide variety of device parameters, such as critical dimensions, overlay, line roughness, and sidewall angle, among others. The Metrology IFT uses this information to outline the measurement capabilities and needed uncertainty levels required to quantify the target dimensions. The Metrology IFT also provides information on new technologies that could be used for future device structures. *See the Lithography chapter for additional information.*

7.3. Factory Integration IFT

Part of the scope of the Factory Integration roadmap is to identify ways to identify ways to improve manufacturing productivity in the factory. This includes ways to fully integrate metrology systems "into the factory to facilitate run-to-run process control, wafer tracking to support traceability, yield analysis, and other off-line analysis." *See the Factory Integration chapter for additional information.* As such, the Factory Integration and the Metrology roadmap teams have a vested interest in exploring and identifying ways that process and metrology information could be used to improve the manufacturing process. One area where the two groups have collaborated closely is VM. The two have worked together to develop a white paper that examines some of the issues preventing wider adoption of VM and offers some possible solutions.

7.4. Environmental, Safety, HEALTH, and Sustainability (ESH/S) IFT

The ESH/S IFT provides information to the Metrology IFT on areas where the capabilities, measurement protocols, and sample handling techniques developed for metrology use could be applied to ESH/S. These include methodologies, instrumentation, and analytical techniques for emerging nanomaterials and their compounds that could be applied to effluent monitoring or contamination monitoring. *See the ESH/S chapter for additional information.*

7.5. Outside System Connectivity (OSC) IFT

Part of the scope of OSC is to identify "devices for signal conditioning, transmission devices, coupling and receiver devices and circuits for Cu wiring, wireless RF & Analog and Mixed Signal (AMS), including antennas, and photonic interconnects." *See the OSC chapter for additional information.* These include optical and RF components where precise measurement of certain parameters is important. These include Measure complex layers for bipolar/CMOS for RF; "Minimally invasive" metrology, Precise wavelength measurement methods, and Testing coupling efficiency for optical interconnects.

8. EMERGING/DISRUPTIVE CONCEPTS AND TECHNOLOGIES

8.1. ADVANCED DATA ANALYTICS

Advanced data analytics is used here to refer to a collection of methods such as big data handling, data analytics, modeling, and simulation that could make a fundamental difference in the way metrology is performed in the factory. Techniques such as digital twining, smart sampling, deep learning, artificial intelligence, and measurement modeling and simulation could be applied to most areas of metrology. Inference and correlation with other aspects of semiconductor manufacturing, coupled with additional process information, could fundamentally change what is measured, when, and how much. The advent of newer and better algorithms, relatively inexpensive data storage, faster data transfer rates, and methods to evaluate large data sets creates an opportunity for integrated adaptation by metrology. Note that the idea of extracting more information from metrology and process data is not new, and some of these techniques have been used extensively in metrology and process control in one form or another. The potentially disruptive aspect of current data analytics methods is the autonomous or semi-autonomous evaluation of data using more sophisticated versions of some of the techniques mentioned above to learn patterns, obtain key insights, and make decisions[287]. Process parameters and complex structures that cannot be measured directly or non-destructively would particularly benefit from such insights. Research and development in metrology-specific applications are currently underway[288-300]. Figure MET8 shows an In-lab. versus In-fab view of applications of machine learning in semiconductor metrology and the areas of overlap between the two. This information is based on analysis of papers presented at five IC Metrology related conferences from 2019 to early 2022. AI and ML related IC metrology applications fall under the broad categories shown below in Figure MET8, with some overlap. We will provide a more in-depth analysis of the applications, uses, limitations, and outlook for this application in a later roadmap.

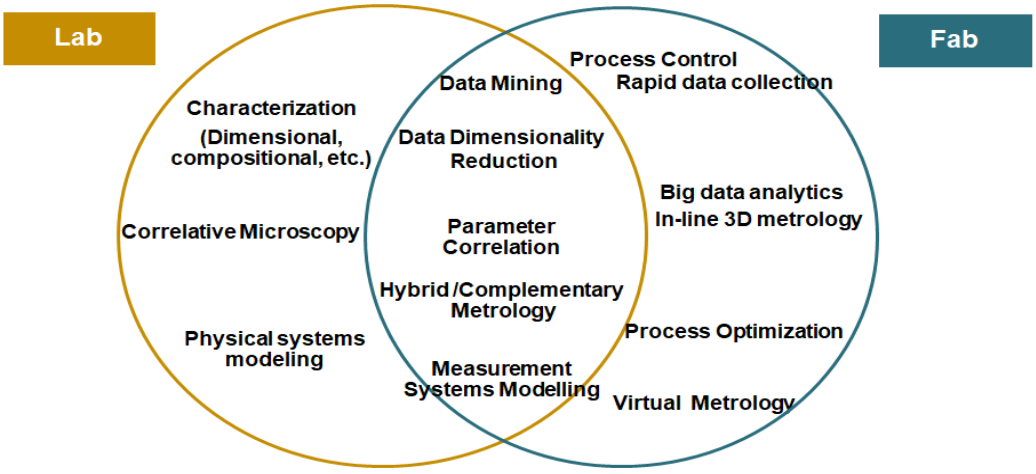

Figure MET8 Lab and Fab based applications of machine learning in semiconductor metrology (as of early 2022)

8.2. SUB-WAVELENGTH IMAGING TECHNIQUES

Subwavelength imaging techniques with the capability of detecting chemical and physical properties would address some of the measurement needs highlighted above. These could be for measuring optical properties and losses in small local regions including hard-to-reach regions of new device structures. Plasmonic-assisted optical focusing [301]

mentioned above, is one such technique. It can focus radiation to sub-wavelength size and could be used for materials identification where the resolution specifications are suitable.

Another technique is high-resolution imaging, similar to those used in biological applications[302], where different aspects of the sample are sensitive to different chemical markers, and wavelengths. Although present techniques would need to be modified for semiconductor applications (thick samples), the overall approach, *localizing and activating different aspects of the sample*, is something that should be explored for IC metrology development.

8.3. X-RAY TECHNIQUES

As highlighted in the Potential Solutions section, the use of X-ray metrology for critical dimensions and films[55] is one of the potential solutions for a host of metrology challenges listed in Table MET- 1. This is due to the resolution of the X-ray, and the range of possible applications. However, a high brightness source with >100X brightness of conventional rotating anode sources would be required This would significantly extend the use of X-ray techniques including CD-SAXS in semiconductor manufacturing. Large-scale X-ray tomographic ptychography could provide full-chip information[303-305] that could be combined with data from other techniques to provide CD, Overlay, films, and defect results for a wide range of logic and memory applications.

9. CONCLUSIONS AND RECOMMENDATIONS

As the industry continues to evolve, so do the manufacturing techniques, device structures, starting materials, and metrology requirements. In evaluating the metrology needs, key observations highlighted throughout the chapter are summarized below.

For 3D structures, the shape, number, and location of parameters needed to characterize logic and memory device structures pose a greater challenge than size alone. Sub-20 nm features are difficult to measure, however, device structure complexity and the use of new materials further complicate a challenging environment.

The large number of parameters needed to fully characterize complex logic and memory structures means that no single instrument has the capability, resolution, or low levels of uncertainty required to provide the needed information. As such, the use of hybrid or complementary metrologies, where multiple instruments are used to evaluate a set of parameters based on their capabilities, would increase. The question of which instrument combinations, analysis, and modeling techniques to use for specific measurements is still a subject of intense research. However, preliminary results are encouraging[280]. Investments in developing platforms with multiple technologies would be helpful. At least, having tools available that enable the combination and comparison of data from multiple technologies would be a good starting point.

A good number of the current metrology techniques with some enhancements can be extended to future nodes. These include enhancements that improve resolution or 3D measurement capabilities. In some cases, a different version of the technology may have the needed resolution but has not been applied to IC manufacturing, or the underlying technology has the needed resolution but not the range. In other cases, a promising technique may have been demonstrated in the lab, but not in the factory. In both cases, new research and development will be required if enhancements (such as high brightness sources for CD-SAXS and tomography for logic applications) are to make the transition from R&D to commercial products.

Data analytics, modeling, and simulation are poised to fundamentally change the way metrology is performed in the factory. Although similar statements have been made numerous times over the last 15 years, the promise of advanced data analytics (in all its variants) has not been realized. Due to the development of new algorithms for AI, deep learning, increased computing power, and awareness of the benefits, advanced data analytics will play a much larger role in IC metrology going forward. This will range from algorithms for specific image and data analysis, inference from large volumes of data, and seamless correlation with data from multiple techniques and other process control modules. Techniques such as VM, combined or hybrid metrology at their core already use a fair amount of data analytics. Knowledge gained from advanced data analytics will provide insight into the key information we need from the process, which will in turn guide when, where, and how much data is acquired.

Finally, a healthy industry infrastructure is required if suppliers are to provide cost-effective metrology and advanced data analytics tools, sensors, controllers, and reference materials. Metrology development requires that instrument vendors start tool development years in advance, when the lithography options may not be clear. Many metrology suppliers are small companies that find the cost of providing new tools for leading-edge activities prohibitive. Initial sales of metrology tools are to tool and process developers. Sustained, high-volume sales of the same metrology

equipment to chip manufacturers do not occur until several years later. The present infrastructure cannot support this delayed return on investment. Funding that meets the investment requirements of the supplier community is needed to take new technology from proof of concept to prototype systems and finally to volume sales. Recent public investments in the semiconductor industry by from different regions of the world could provide this support.

10. REFERENCES

[1] M. A. Breton, D. Schmidt, A. Greene, J. Frougier, and N. Felix, "Review of nanosheet metrology opportunities for technology readiness," *Journal of Micro/Nanopatterning, Materials, and Metrology,* vol. 21, no. 2, p. 021206, 2022.

[2] L. Van den hove, "The endless progression of Moore's law (Conference Presentation)," in *Proc. SPIE*, vol. 12053: SPIE, 2022.

[3] N. G. Orji *et al.*, "Metrology for the next generation of semiconductor devices," *Nature Electronics,* vol. 1, no. 10, pp. 532-547, 2018/10/01 2018, doi: 10.1038/s41928-018-0150-9.

[4] A. Masafumi *et al.*, "Metrology and inspection required for next generation lithography," *Japanese Journal of Applied Physics,* vol. 56, no. 6S1, p. 06GA01, 2017. [Online]. Available: http://stacks.iop.org/1347-4065/56/i=6S1/a=06GA01.

[5] B. Bunday, N. Orji, and J. Allgair, "High volume manufacturing metrology needs at and beyond the 5 nm node," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2584555. [Online]. Available: https://doi.org/10.1117/12.2584555

[6] B. D. Bunday, A. Bello, E. Solecky, and A. Vaid, "7/5nm logic manufacturing capabilities and requirements of metrology," in *Proc. SPIE*, 2018, vol. 10585, p. 105850I.

[7] "TSMC N2 NANOSHEET: The New Frontier in Advanced Logic Technology." TSMC. https://n2.tsmc.com/english/dedicatedFoundry/technology/N2.htm (accessed September, 11th, 2023).

[8] J.-A. Carballo, W.-T. J. Chan, P. A. Gargini, A. B. Kahng, and S. Nath, "ITRS 2.0: Toward a re-framing of the Semiconductor Technology Roadmap," in *2014 IEEE 32nd International Conference on Computer Design (ICCD)*, 2014/10 2014: IEEE, doi: 10.1109/iccd.2014.6974673. [Online]. Available: http://dx.doi.org/10.1109/iccd.2014.6974673

[9] S. Salahuddin, K. Ni, and S. Datta, "The era of hyper-scaling in electronics," *Nature Electronics,* vol. 1, pp. 442–450, 2018/09/01 2018, doi: https://doi.org/10.1038/s41928-018-0117-x.

[10] C. H. Naylor *et al.*, "2D Materials in the BEOL," in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 11-16 June 2023 2023, pp. 1-2, doi: 10.23919/VLSITechnologyandCir57934.2023.10185307.

[11] B. M. Barnes, R. M. Silver, S. Schmucker, H. Zhou, M.-A. Henn, and M. Y. Sohn, "Extensibility of optics-based metrology for sub-5nm technology (Conference Presentation)," in *Proc. SPIE*, 2018, vol. 10585.

[12] P. D. Bisschop, "Stochastic printing failures in extreme ultraviolet lithography," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 17, no. 4, pp. 1-23, 2018. [Online]. Available: https://doi.org/10.1117/1.JMM.17.4.041011.

[13] L. Wu, "The next generation of gate-all-around transistors," *Nature Electronics,* vol. 6, no. 7, pp. 469-469, 2023/07/01 2023, doi: 10.1038/s41928-023-01006-x.

[14] A. Veloso *et al.*, "Nanowire & nanosheet FETs for ultra-scaled, high-density logic and memory applications," *Solid-State Electronics,* p. 107736, 2019/11/26/ 2019, doi: https://doi.org/10.1016/j.sse.2019.107736.

[15] M. C. Lemme, D. Akinwande, C. Huyghebaert, and C. Stampfer, "2D materials for future heterogeneous electronics," *Nature Communications,* vol. 13, no. 1, p. 1392, 2022/03/16 2022, doi: 10.1038/s41467-022-29001-4.

[16] S. Das *et al.*, "Transistors based on two-dimensional materials for future integrated circuits," *Nature Electronics,* vol. 4, no. 11, pp. 786-799, 2021/11/01 2021, doi: 10.1038/s41928-021-00670-1.

[17] L. Tong *et al.*, "2D materials–based homogeneous transistor-memory architecture for neuromorphic hardware," *Science,* vol. 373, no. 6561, pp. 1353-1358, 2021, doi: doi:10.1126/science.abg3161.

[18] U. Celano, Electrical Atomic Force Microscopy for Nanoelectronics. Springer, 2019.

[19] F. Hui and M. Lanza, "Scanning probe microscopy for advanced nanoelectronics," *Nature Electronics,* vol. 2, no. 6, pp. 221-229, 2019/06/01 2019, doi: 10.1038/s41928-019-0264-8.

[20] S. Reboh *et al.*, "Imaging, Modeling and Engineering of Strain in Gate-All-Around Nanosheet Transistors," in *IEDM*, 2019.

[21] C. E. Murray *et al.*, "Mapping of the mechanical response in Si/SiGe nanosheet device geometries," *Communications Engineering,* vol. 1, no. 1, p. 11, 2022/06/10 2022, doi: 10.1038/s44172-022-00011-w.

[22] B. Bunday, T. A. Germer, V. Vartanian, A. Cordes, A. Cepler, and C. Settens, "Gaps Analysis for CD Metrology Beyond the 22 nm Node," (in English), *Proc Spie,* vol. 8681, 2013, doi: Unsp 86813b 10.1117/12.2012472.

[23] J. A. Liddle and G. M. Gallatin, "Lithography, metrology and nanomanufacturing," *Nanoscale,* 10.1039/C1NR10046G vol. 3, no. 7, pp. 2679-2688, 2011, doi: 10.1039/C1NR10046G.

[24] D. Akinwande *et al.*, "Graphene and two-dimensional materials for silicon technology," *Nature,* vol. 573, no. 7775, pp. 507-518, 2019/09/01 2019, doi: 10.1038/s41586-019-1573-9.

[25] L. Liu *et al.*, "Transferred van der Waals metal electrodes for sub-1-nm MoS2 vertical transistors," *Nature Electronics,* vol. 4, no. 5, pp. 342-347, 2021/05/01 2021, doi: 10.1038/s41928-021-00566-0.

[26] P.-C. Shen *et al.*, "Healing of donor defect states in monolayer molybdenum disulfide using oxygen-incorporated chemical vapour deposition," *Nature Electronics,* vol. 5, no. 1, pp. 28-36, 2022/01/01 2022, doi: 10.1038/s41928-021-00685-8.

[27] C. Y. Andrew, T. Srimani, C. Lau, B. Benton, M. Nelson, and M. M. Shulaker, "Foundry Integration of Carbon Nanotube FETs with 320 nm Contacted Gate Pitch using New Lift-off-free Process," *IEEE Electron Device Letters,* 2022.

[28] M. D. Bishop *et al.*, "Fabrication of carbon nanotube field-effect transistors in commercial silicon manufacturing facilities," *Nature Electronics,* vol. 3, no. 8, pp. 492-501, 2020/08/01 2020, doi: 10.1038/s41928-020-0419-7.

[29] G. Hills *et al.*, "Modern microprocessor built from complementary carbon nanotube transistors," *Nature,* vol. 572, no. 7771, pp. 595-602, 2019/08/01 2019, doi: 10.1038/s41586-019-1493-8.

[30] D. E. Nikonov and I. A. Young, "Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits,* vol. 1, pp. 3-11, 2015, doi: 10.1109/JXCDC.2015.2418033.

[31] I. Young and D. E. Nikonov, "Materials and Devices for Beyond CMOS Computing: Prospects and Best Bets " *Frontiers of Characterization and Metrology for Nanoelectronics,* p. 21, 2019.

[32] S. Manipatruni, D. E. Nikonov, and I. A. Young, "Beyond CMOS computing with spin and polarization," *Nature Physics,* vol. 14, no. 4, pp. 338-343, 2018/04/01 2018, doi: 10.1038/s41567-018-0101-4.

[33] G. Iannaccone, F. Bonaccorso, L. Colombo, and G. Fiori, "Quantum engineering of transistors based on 2D materials heterostructures," *Nature Nanotechnology,* vol. 13, no. 3, pp. 183-191, 2018/03/01 2018, doi: 10.1038/s41565-018-0082-6.

[34] S. Pi *et al.*, "Memristor crossbar arrays with 6-nm half-pitch and 2-nm critical dimension," *Nature Nanotechnology,* vol. 14, no. 1, pp. 35-39, 2019/01/01 2019, doi: 10.1038/s41565-018-0302-0.

[35] F. Arute *et al.*, "Quantum supremacy using a programmable superconducting processor," *Nature,* vol. 574, no. 7779, pp. 505-510, 2019/10/01 2019, doi: 10.1038/s41586-019-1666-5.

[36] G. Freychet *et al.*, "Using critical-dimension grazing-incidence small angle x-ray scattering to study line edge roughness (Conference Presentation)," in *Proc. SPIE*, 2019, vol. 10959: International Society for Optics and Photonics, p. 109590R.

[37] J. Wyrick *et al.*, "Atom-by-Atom Fabrication of Single and Few Dopant Quantum Devices," (in English), *Adv Funct Mater,* p. 1903475, Aug 14 2019, doi: ARTN 1903475 10.1002/adfm.201903475.

[38] R. Wagner, B. Schleich, B. Haefner, A. Kuhnle, S. Wartzack, and G. Lanza, "Challenges and Potentials of Digital Twins and Industry 4.0 in Product Design and Production for High Performance Products," *Procedia CIRP,* vol. 84, pp. 88-93, 2019/01/01/ 2019, doi: https://doi.org/10.1016/j.procir.2019.04.219.

[39] J. A. Liddle, B. D. Hoskins, A. E. Vladár, and J. S. Villarrubia, "Research Update: Electron beam-based metrology after CMOS," *APL Materials,* vol. 6, no. 7, p. 070701, 2018, doi: 10.1063/1.5038249.

[40] D. Giacobello, M. G. Christensen, M. N. Murthi, S. H. Jensen, and M. Moonen, "Retrieving Sparse Patterns Using a Compressed Sensing Framework: Applications to Speech Coding Based on Sparse Linear Prediction," *IEEE Signal Processing Letters,* vol. 17, no. 1, pp. 103-106, 2010, doi: 10.1109/LSP.2009.2034560.

[41] Y. Bi, X. S. Hu, Y. Jin, M. Niemier, K. Shamsi, and X. Z. Yin, "Enhancing Hardware Security with Emerging Transistor Technologies," *2016 International Great Lakes Symposium on VLSI (GLSVLSI),* pp. 305-310, 2016, doi: 10.1145/2902961.2903041.

[42] A. Chen, X. S. Hu, Y. Jin, M. Niemier, and X. Z. Yin, "Using Emerging Technologies for Hardware Security Beyond PUFs," *Proceedings of the 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE),* pp. 1544-1549, 2016.

[43] *SEMI E187 - Specification for Cybersecurity of Fab Equipment*, SEMI, 2022. [Online]. Available: https://store-us.semi.org/products/e18700-semi-e187-specification-for-cybersecurity-of-fab-equipment

[44] H. Jiang *et al.*, "A provable key destruction scheme based on memristive crossbar arrays," *Nature Electronics,* vol. 1, no. 10, pp. 548-554, 2018/10/01 2018, doi: 10.1038/s41928-018-0146-5.
[45] H. Nili *et al.*, "Hardware-intrinsic security primitives enabled by analogue state and nonlinear conductance variations in integrated memristors," *Nature Electronics,* vol. 1, no. 3, pp. 197-202, 2018/03/01 2018, doi: 10.1038/s41928-018-0039-7.
[46] C. Mack, "Uncertainty in roughness measurements: putting error bars on line-edge roughness," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 16, no. 1, p. 010501, 2017. [Online]. Available: https://doi.org/10.1117/1.JMM.16.1.010501.
[47] H. Fukuda *et al.*, "Measurement of pattern roughness and local size variation using CD-SEM," *J. of Micro/Nanolithography, MEMS, and MOEMS,* vol. 17, no. 4, p. 9, 2018.
[48] NIST, "Strategic Opportunities for U.S. Semiconductor Manufacturing," NIST, Gaithersburg, MD, 2022.
[49] NIST, "Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry: Summary of Request for Information Responses," in "Special Publications," NIST, Gaithersburg, MD, 2022.
[50] "Virtual Metrology White Paper - INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS (IRDS) 2017 Edition " IEEE, 2018.
[51] M. Breton *et al.*, "Nanosheet metrology opportunities for technology readiness," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2583636. [Online]. Available: https://doi.org/10.1117/12.2583636
[52] D. Schmidt *et al.*, "In-line Raman spectroscopy for stacked nanosheet device manufacturing," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2582181. [Online]. Available: https://doi.org/10.1117/12.2582181
[53] C. Jun, "The challenges of in-fab metrology: the needs for innovative solutions," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2588734. [Online]. Available: https://doi.org/10.1117/12.2588734
[54] B. Bunday, "HVM metrology challenges towards the 5nm node," in *Proc. SPIE*, 2016, vol. 9778: International Society for Optics and Photonics, p. 97780E.
[55] B. Bunday, E. Solecky, A. Vaid, A. F. Bello, and X. Dai, "Metrology capabilities and needs for 7nm and 5nm logic nodes," in *Proc. SPIE*, 2017/03/28 2017, vol. 101450G SPIE, doi: 10.1117/12.2260870. [Online]. Available: http://dx.doi.org/10.1117/12.2260870
[56] G. F. Lorusso *et al.*, "Electron beam metrology for advanced technology nodes," *Japanese Journal of Applied Physics,* vol. 58, no. SD, p. SD0801, 2019.
[57] J. Severi *et al.*, "Chemically amplified resist CDSEM metrology exploration for high NA EUV lithography," *Journal of Micro/Nanopatterning, Materials, and Metrology,* vol. 21, no. 2, p. 021207, 2022. [Online]. Available: https://doi.org/10.1117/1.JMM.21.2.021207.
[58] B. Bunday *et al.*, "Time-dependent electron-beam-induced photoresist shrinkage effects," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 11, no. 2, pp. 023007-1, 2012/06/05 2012, doi: 10.1117/1.jmm.11.2.023007.
[59] A. E. Vladár *et al.*, "10nm three-dimensional CD-SEM metrology," in *Proc. SPIE*, 2014/04/14 2014: SPIE, doi: 10.1117/12.2045977. [Online]. Available: http://dx.doi.org/10.1117/12.2045977
[60] A. Vladár, "Model-Based Scanning Electron Microscopy Critical-Dimension Metrology for 3D Nanostructures," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 3-30.
[61] J. S. Villarrubia *et al.*, "Scanning electron microscope measurement of width and shape of 10nm patterned lines using a JMONSEL-modeled library," *Ultramicroscopy,* vol. 154, pp. 15-28, 2015/07/01/ 2015, doi: https://doi.org/10.1016/j.ultramic.2015.01.004.
[62] B. Bunday, A. Cepler, A. Cordes, and A. Arceo, "CD-SEM metrology for sub-10nm width features," in *Proc. SPIE*, 2014/04/02 2014: SPIE, doi: 10.1117/12.2047099. [Online]. Available: http://dx.doi.org/10.1117/12.2047099
[63] C. Valade, J. Hazart, S. Bérard-Bergery, E. Sungauer, M. Besacier, and C. Gourgon, "Tilted beam scanning electron microscopy, 3-D metrology for microelectronics industry," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 18, no. 3, pp. 1-13, 2019. [Online]. Available: https://doi.org/10.1117/1.JMM.18.3.034001.
[64] K. Crosby, A. L. Eberle, and D. Zeidler, "Multi-beam SEM Technology for High Throughput Imaging," *MRS Advances,* vol. 1, no. 26, pp. 1915-1920, 2016, doi: 10.1557/adv.2016.363.

[65] M. Malloy *et al.*, "Massively parallel E-beam inspection: enabling next-generation patterned defect inspection for wafer and mask manufacturing," in *Alternative Lithographic Technologies VII*, 2015, doi: 10.1117/12.2175535. [Online]. Available: http://dx.doi.org/10.1117/12.2175535

[66] O. D. Patterson *et al.*, "Advancement in Massively Parallel Electron Beam Inspection Technology for 7nm and Below Process Development and Manufacturing," in *Frontiers of Characterization and Metrology for Nanoelectronics*, 2019: NIST.

[67] M. De Goede, E. Johlin, B. Sciacca, F. Boughorbel, and E. C. Garnett, "3D multi-energy deconvolution electron microscopy," *Nanoscale,* vol. 9, no. 2, pp. 684-689, 2017.

[68] A. Kenslea *et al.*, "CD-TEM: Characterizing impact of TEM sample preparation on CD metrology," in *2018 29th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)*, April 30 2018-May 3 2018 2018, pp. 324-327, doi: 10.1109/ASMC.2018.8373170.

[69] J. S. Clarke, M. B. Schmidt, and N. G. Orji, "Photoresist cross-sectioning with negligible damage using a dual-beam FIB-SEM: A high throughput method for profile imaging," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 25, no. 6, p. 2526, 2007, doi: 10.1116/1.2804516.

[70] M.-A. Henn, H. Zhou, and B. M. Barnes, "Data-driven approaches to optical patterned defect detection," *OSA Continuum,* vol. 2, no. 9, pp. 2683-2693, 2019/09/15 2019, doi: 10.1364/OSAC.2.002683.

[71] R. Attota *et al.*, "TSOM method for semiconductor metrology," in *Proc. SPIE*, 2011/03/17 2011: SPIE, doi: 10.1117/12.881620. [Online]. Available: http://dx.doi.org/10.1117/12.881620

[72] S. Bernard, R. A. Miller, V. Pepper, J. Braggin, and F. F. C. Duval, "Impact of using filtration on global and local uniformity of spin on glue materials," in *Micromachining and Microfabrication Process Technology XVI*, 2011/02/10 2011: SPIE, doi: 10.1117/12.878757. [Online]. Available: http://dx.doi.org/10.1117/12.878757

[73] J. Qin, R. M. Silver, B. M. Barnes, H. Zhou, R. G. Dixson, and M.-A. Henn, "Deep subwavelength nanometric image reconstruction using Fourier domain optical normalization," *Light: Science & Applications,* vol. 5, p. e16038, 2016/02/26 2016, doi: 10.1038/lsa.2016.38.

[74] T. F. Crimmins, "Defect metrology challenges at the 11-nm node and beyond," in *Proc. SPIE*, 2010/03/11 2010: SPIE, doi: 10.1117/12.846623. [Online]. Available: http://dx.doi.org/10.1117/12.846623

[75] A. D. Humphris, B. Zhao, D. Bastard, and B. Bunday, "Probe microscopy for metrology of next generation devices," in *Proc. SPIE*, 2016, vol. 9778: International Society for Optics and Photonics, p. 97782L.

[76] A. D. L. Humphris, F. L., M. Tedaldi, D. Ockwell, and J. Goulden, "A Novel High Throughput Probe Microscope: for measuring 3D High Aspect Ratio Structures, Designed for In-Line, Integrated or Standalone Operation," in *Proc. SPIE*, 2020, vol. 11325.

[77] B. M. Barnes *et al.*, "Three-dimensional deep sub-wavelength defect detection using $\lambda = 193$ nm optical microscopy," *Optics Express,* vol. 21, no. 22, p. 26219, 2013/10/25 2013, doi: 10.1364/oe.21.026219.

[78] B. M. Barnes, H. Zhou, M. A. Henn, M. Y. Sohn, and R. M. Silver, "Optimizing image-based patterned defect inspection through FDTD simulations at multiple ultraviolet wavelengths," in *Modeling Aspects in Optical Metrology VI*, 2017, vol. 10330, pp. 103300W-1-15, doi: Unsp 103300w 10.1117/12.2271149.

[79] B. M. Barnes, H. Zhou, M. A. Henn, M. Y. Sohn, and R. M. Silver, "Assessing the wavelength extensibility of optical patterned defect inspection," *Proc Spie,* vol. 10145, 2017, doi: Unsp 1014516 10.1117/12.2262191.

[80] B. M. Barnes, M.-A. Henn, M. Y. Sohn, H. Zhou, and R. M. Silver, "Assessing Form-Dependent Optical Scattering at Vacuum- and Extreme-Ultraviolet Wavelengths of Nanostructures with Two-Dimensional Periodicity," *Physical Review Applied,* vol. 11, no. 6, p. 064056, 06/24/ 2019, doi: 10.1103/PhysRevApplied.11.064056.

[81] A. Arceo, B. Bunday, V. Vartanian, and R. Attota, "Patterned defect and CD metrology by TSOM beyond the 22-nm node," in *Proc. SPIE*, 2012/03/29 2012: SPIE, doi: 10.1117/12.917236. [Online]. Available: http://dx.doi.org/10.1117/12.917236

[82] J. H. Lee, S. Na, J. Jeong, and R. Buengener, Comparative near infrared through-focus scanning optical microscopy for 3D memory subsurface defect detection and classification (SPIE Advanced Lithography). SPIE, 2021.

[83] P. De Bisschop and E. Hendrickx, "Stochastic printing failures in EUV lithography," in *Proc. SPIE*, 2019, vol. 10957: International Society for Optics and Photonics, p. 109570E.

[84] M. Saib *et al.*, "Scatterometry and AFM measurement combination for area selective deposition process characterization," in *Proc. SPIE*, 2019, vol. 10959: International Society for Optics and Photonics, p. 109591N.

[85] M. Sanchez, G. Wallraff, N. Megiddo, and W. Hinsberg, "An analysis of EUV resist stochastic printing failures," in *Proc. SPIE*, 2019, vol. 11147: SPIE. [Online]. Available: https://doi.org/10.1117/12.2537632. [Online]. Available: https://doi.org/10.1117/12.2537632

[86] Y. Abramovitz *et al.*, "EPE budget analysis and margin co-optimization on the multiple critical on-device features in a single image for yield enhancement," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2585369. [Online]. Available: https://doi.org/10.1117/12.2585369

[87] S. Smith *et al.*, "Comparison of Measurement Techniques for Linewidth Metrology on Advanced Photomasks," *IEEE Transactions on Semiconductor Manufacturing,* vol. 22, no. 1, pp. 72-79, 2009, doi: 10.1109/tsm.2008.2010733.

[88] B. Bunday, C. Montgomery, W. Montgomery, and A. Cepler, "Photoresist shrinkage effects in 16 nm node extreme ultraviolet (EUV) photoresist targets," in *Proc. SPIE*, 2013/04/10 2013: SPIE, doi: 10.1117/12.2012470. [Online]. Available: http://dx.doi.org/10.1117/12.2012470

[89] B. D. Bunday *et al.*, "Value-Added Metrology," *IEEE Transactions on Semiconductor Manufacturing,* vol. 20, no. 3, pp. 266-277, 2007, doi: 10.1109/TSM.2007.901851.

[90] J. Bals and M. Epple, "Deep learning for automated size and shape analysis of nanoparticles in scanning electron microscopy," *RSC Advances,* 10.1039/D2RA07812K vol. 13, no. 5, pp. 2795-2802, 2023, doi: 10.1039/D2RA07812K.

[91] B. Le Gratiet *et al.*, "Contour based metrology: getting more from a SEM image," in *Proc. SPIE*, 2019, vol. 10959: International Society for Optics and Photonics, p. 109591M.

[92] J. S. Villarrubia, R. G. Dixson, and A. E. Vladar, "Proximity-associated errors in contour metrology," in *Proc. SPIE*, 2010, vol. 7638, doi: 10.1117/12.848406. [Online]. Available: http://dx.doi.org/10.1117/12.848406

[93] N. G. Orji, R. G. Dixson, B. P. Ng, A. E. Vladár, and M. T. Postek, "Contour metrology using critical dimension atomic force microscopy," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 15, no. 4, p. 044006, 2016, doi: 10.1117/1.jmm.15.4.044006.

[94] A. Cordes, B. Bunday, and J. Nadeau, "Profile Variation Impact on FIB Cross-Section Metrology," in *Proc. SPIE*, 2012, vol. 8324, doi: 10.1117/12.917321. [Online]. Available: http://dx.doi.org/10.1117/12.917321

[95] S. Knight *et al.*, "Advanced metrology needs for nanoelectronics lithography," *Comptes Rendus Physique,* vol. 7, no. 8, pp. 931-941, 2006/10 2006, doi: 10.1016/j.crhy.2006.10.004.

[96] T. Zhou *et al.*, "An effective method of contour extraction for SEM image based on DCNN," in *2020 International Workshop on Advanced Patterning Solutions (IWAPS)*, 5-6 Nov. 2020 2020, pp. 1-4, doi: 10.1109/IWAPS51164.2020.9286798.

[97] J. Li, O. Kritsun, P. Dasari, C. Volkman, T. Wallow, and J. Hu, "Evaluating scatterometry 3D capabilities for EUV," in *Proc. SPIE*, 2013/04/10 2013: SPIE, doi: 10.1117/12.2011675. [Online]. Available: http://dx.doi.org/10.1117/12.2011675

[98] A.-L. Charley *et al.*, "Scatterometry for gate all around (GAA) technology enablement (Conference Presentation)," in *Proc. SPIE*, 2018, vol. 10585.

[99] A. C. Diebold, A. Antonelli, and N. Keller, "Perspective: Optical measurement of feature dimensions and shapes by scatterometry," (in English), *Apl Materials,* vol. 6, no. 5, May 2018, doi: Artn 058201 10.1063/1.5018310.

[100] M. Ghafoori *et al.*, "Broadband scatterometry at extreme ultraviolet wavelengths for nanograting characterization," in *Metrology, Inspection, and Process Control for Semiconductor Manufacturing XXXV*, 2021, vol. 11611: SPIE, pp. 602-614.

[101] A. F. Herrero, M. Pflüger, J. Puls, F. Scholze, and V. Soltwisch, "Uncertainties in the reconstruction of nanostructures in EUV scatterometry and grazing incidence small-angle X-ray scattering," *Optics Express,* vol. 29, no. 22, pp. 35580-35591, 2021.

[102] A. Fernández Herrero, F. Scholze, G. Dai, and V. Soltwisch, "Analysis of Line-Edge Roughness Using EUV Scatterometry," *Nanomanufacturing and Metrology,* pp. 1-10, 2022.

[103] D. Schmidt et al., Vertical travelling scatterometry for metrology on fully integrated devices (SPIE Advanced Lithography + Patterning). SPIE, 2022.

[104] N. G. Orji, A. Martinez, R. G. Dixson, and J. Allgair, "Progress on implementation of a CD-AFM-based reference measurement system," in *Proc. SPIE*, 2006, vol. 6152, doi: Artn 61520o 10.1117/12.653287. [Online]. Available: https://doi.org/10.1117/12.653287

[105] H. Danish, A. Khurshid, S. Jianmin, and X. Hui, "Advances in the atomic force microscopy for critical dimension metrology," *Measurement Science and Technology,* vol. 28, no. 1, p. 012001, 2017. [Online]. Available: http://stacks.iop.org/0957-0233/28/i=1/a=012001.

[106] D. Kong *et al.*, "Machine learning and hybrid metrology using scatterometry and LE-XRF to detect voids in copper lines," in *Proc. SPIE*, 2019, vol. 10959: International Society for Optics and Photonics, p. 109590A.
[107] S. Wolfing, "AI and Machine Learning for Advanced Semiconductor Metrology and Process Control," in *Frontiers of Characterization and Metrology for Nanoelectronics*, 2019: NIST.
[108] P. Leray, S. Halder, D. Cerbu, Roelwuyts, and W. Verachtert, "Machine Learning Application For Metrology And Process Control," in *Frontiers of Characterization and Metrology for Nanoelectronics*, 2019: NIST.
[109] S. Dey, A. Diebold, N. Keller, and M. Korde, "Muller matrix spectroscopic ellipsometry based scatterometry simulations of Si and Si/SixGe1-x/Si/SixGe1-x/Si fins for sub-7nm node gate-all-around transistor metrology (Conference Presentation)," in *Proc. SPIE*, 2018, vol. 10585: SPIE.
[110] S. O'Mullane, N. Keller, and A. C. Diebold, "Modeling ellipsometric measurement of three-dimensional structures with rigorous coupled wave analysis and finite element method simulations," 2016, vol. 15: SPIE, p. 8.
[111] D. J. Dixit *et al.*, "Sensitivity analysis and line edge roughness determination of 28-nm pitch silicon fins using Mueller matrix spectroscopic ellipsometry-based optical critical dimension metrology," 2015, vol. 14: SPIE, p. 13.
[112] M. Korde et al., Scatterometry of nanowire/ nanosheet FETs for advanced technology nodes (SPIE Advanced Lithography). SPIE, 2021.
[113] S. C. C. Hsu *et al.*, "Scatterometry or imaging overlay: a comparative study," in *Proc. SPIE*, 2015/03/19 2015: SPIE, doi: 10.1117/12.2085950. [Online]. Available: http://dx.doi.org/10.1117/12.2085950
[114] A. J. den Boef, "Optical wafer metrology sensors for process-robust CD and overlay control in semiconductor device manufacturing," *Surf Topogr-Metrol,* vol. 4, no. 2, Jun 2016, doi: 10.1088/2051-672x/4/2/023001.
[115] S. O'Mullane, D. Dixit, and A. Diebold, "Advancements in Ellipsometric and Scatterometric Analysis," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 65-108.
[116] D. J. Dixit *et al.*, "Metrology for block copolymer directed self-assembly structures using Mueller matrix-based scatterometry," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 14, no. 2, p. 021102, 2015/04/10 2015, doi: 10.1117/1.jmm.14.2.021102.
[117] D. Dixit *et al.*, "Optical critical dimension metrology for directed self-assembly assisted contact hole shrink," 2016, vol. 15: SPIE, p. 15.
[118] D. Dixit *et al.*, "Advanced applications of scatterometry based optical metrology," in *Proc. SPIE*, 2017.
[119] D. Dixit *et al.*, "Nonconventional applications of Mueller matrix-based scatterometry for advanced technology nodes," *J. of Micro/Nanolithography, MEMS, and MOEMS,* vol. 17, no. 3, p. 10, 2018.
[120] M. Korde, S. Kal, C. Pereira, N. Keller, A. Mosden, and A. C. Diebold, "Optical characterization of multi-NST nanowire test structures using Mueller matrix spectroscopic ellipsometry (MMSE) based scatterometry for sub 5nm nodes," in *Proc. SPIE*, 2019, vol. 10959: International Society for Optics and Photonics, p. 109590X.
[121] N. F. Zhang, R. M. Silver, H. Zhou, and B. M. Barnes, "Improving optical measurement uncertainty with combined multitool metrology using a Bayesian approach," *Applied Optics,* vol. 51, no. 25, p. 6196, 2012/08/30 2012, doi: 10.1364/ao.51.006196.
[122] D. Kong *et al.*, "In-line characterization of non-selective SiGe nodule defects with scatterometry enabled by machine learning (Conference Presentation)," in *Proc. SPIE*, 2018, vol. 10585: SPIE.
[123] B. M. Barnes, R. M. Silver, S. Schmucker, H. Zhou, M.-A. Henn, and M. Y. Sohn, "Extensibility of optics-based metrology for sub-5nm technology (Conference Presentation)," in *SPIE Advanced Lithography*, 2018, vol. 10585.
[124] B. Barnes and M.-A. Henn, "Improving data-driven OCD uncertainties from Gaussian process regression," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2584821. [Online]. Available: https://doi.org/10.1117/12.2584821
[125] R. L. Jones *et al.*, "Small angle x-ray scattering for sub-100 nm pattern characterization," *Applied Physics Letters,* vol. 83, no. 19, pp. 4059-4061, 2003/11/10 2003, doi: 10.1063/1.1622793.
[126] D. F. Sunday, E. Ashley, L. Wan, K. C. Patel, R. Ruiz, and R. J. Kline, "Template-polymer commensurability and directed self-assembly block copolymer lithography," *Journal of Polymer Science Part B: Polymer Physics,* vol. 53, no. 8, pp. 595-603, 2015/02/05 2015, doi: 10.1002/polb.23675.

[127] D. Sunday and R. Kline, "X-Ray Metrology for Semiconductor Fabrication," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 31-64.
[128] K. Sasaki, T. Hashimoto, Y. Kuo, H. Tsukada, and H. Tanizaki, "Measurability analysis of the HAR structure in 3D memory by T-SAXS simulation," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2582070. [Online]. Available: https://doi.org/10.1117/12.2582070
[129] D. F. Sunday, S. List, J. S. Chawla, and R. J. Kline, "Determining the shape and periodicity of nanostructures using small-angle X-ray scattering," *Journal of Applied Crystallography,* vol. 48, no. 5, pp. 1355-1363, 2015/08/08 2015, doi: 10.1107/s1600576715013369.
[130] R. J. Kline, D. F. Sunday, D. Windover, and B. D. Bunday, "X-ray scattering critical dimensional metrology using a compact x-ray source for next generation semiconductor devices," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 16, no. 1, p. 014001, 2017/02/08 2017, doi: 10.1117/1.jmm.16.1.014001.
[131] M. Bech *et al.*, "Hard X-ray phase-contrast imaging with the Compact Light Source based on inverse Compton X-rays," *Journal of Synchrotron Radiation,* vol. 16, no. 1, pp. 43-47, 2008/11/27 2008, doi: 10.1107/s090904950803464x.
[132] W. S. Graves, W. Brown, F. X. Kaertner, and D. E. Moncton, "MIT inverse Compton source concept," Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, vol. 608, no. 1, pp. S103-S105, 2009/09 2009, doi: 10.1016/j.nima.2009.05.042.
[133] J. M. J. Madey, E. B. Szarmes, M. R. Hadmack, B. T. Jacobson, J. M. D. Kowalczyk, and P. Niknejadi, "Optimized cavity-enhanced x-ray sources for x-ray microscopy," in *X-Ray Nanoimaging: Instruments and Methods*, 2013/09/26 2013: SPIE, doi: 10.1117/12.2027193. [Online]. Available: http://dx.doi.org/10.1117/12.2027193
[134] N. D. Powers *et al.*, "Quasi-monoenergetic and tunable X-rays from a laser-driven Compton light source," *Nature Photonics,* vol. 8, no. 1, pp. 28-31, 2013/11/24 2013, doi: 10.1038/nphoton.2013.314.
[135] M. Fan, R. Ranjit, A. Thurber, and D. Engelhard, *High resolution profiles of 3D NAND pillars using x-ray scattering metrology* (SPIE Advanced Lithography). SPIE, 2021.
[136] M. Wormington et al., X-ray critical dimension metrology solution for high aspect ratio semiconductor structures (SPIE Advanced Lithography). SPIE, 2021.
[137] M. Pfluger, V. Soltwisch, J. Probst, F. Scholze, and M. Krumrey, "Grazing-incidence small-angle X-ray scattering (GISAXS) on small periodic targets using large beams," *IUCrJ,* vol. 4, no. 4, pp. 431-438, 2017, doi: doi:10.1107/S2052252517006297.
[138] M. Pflüger, R. J. Kline, A. F. Herrero, M. Hammerschmidt, V. Soltwisch, and M. Krumrey, "Extracting dimensional parameters of gratings produced with self-aligned multiple patterning using grazing-incidence small-angle x-ray scattering," *J. of Micro/Nanolithography, MEMS, and MOEMS,* vol. 19, no. 1, p. 014001, 2020. [Online]. Available: https://doi.org/10.1117/1.JMM.19.1.014001.
[139] G. Freychet *et al.*, "Estimation of Line Cross Sections Using Critical-Dimension Grazing-Incidence Small-Angle X-Ray Scattering," *Physical Review Applied,* vol. 12, no. 4, p. 044026, 10/11/ 2019, doi: 10.1103/PhysRevApplied.12.044026.
[140] T. Hofmann, E. Dobisz, and B. M. Ocko, "Grazing incident small angle x-ray scattering: A metrology to probe nanopatterned surfaces," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 27, no. 6, p. 3238, 2009, doi: 10.1116/1.3253608.
[141] Y. Ishibashi, T. Koike, Y. Yamazaki, Y. Ito, Y. Okazaki, and K. Omote, "Characterization of cross sectional profile of nanostructure line grating using small angle x-ray scattering," in *Proc. SPIE*, 2010/03/11 2010: SPIE, doi: 10.1117/12.848193. [Online]. Available: http://dx.doi.org/10.1117/12.848193
[142] S.-J. Cho *et al.*, "Three-dimensional imaging of undercut and sidewall structures by atomic force microscopy," *Review of Scientific Instruments,* vol. 82, no. 2, p. 023707, 2011, doi: 10.1063/1.3553199.
[143] Test Method for Evaluation of Line-Edge Roughness and Linewidth Roughness, SEMI P47-0307 (Reapproved 0513), SEMI, Milpitas, CA, 2013.
[144] B. D. Bunday and C. A. Mack, "Influence of metrology error in measurement of line edge roughness power spectral density," in *Proc. SPIE*, 2014/04/14 2014: SPIE, doi: 10.1117/12.2047100. [Online]. Available: http://dx.doi.org/10.1117/12.2047100
[145] B. D. Bunday *et al.*, "Determination of optimal parameters for CD-SEM measurement of line edge roughness," *Proc Spie,* vol. 5375, pp. 515-533, 2004, doi: 10.1117/12.535926.
[146] G. F. Lorusso *et al.*, "Need for LWR metrology standardization:the imec roughness protocol," (in English), *J Micro-Nanolith Mem,* vol. 17, no. 4, Oct 2018, doi: 10.1117/1.Jmm.17.4.041009.

[147] C. A. Mack, "Analytical expression for impact of linewidth roughness on critical dimension uniformity," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 13, no. 2, p. 020501, 2014.
[148] S. Levi *et al.*, "Lines roughness holistic metrology sensitivity study supported by EUV mask designed with induced roughness (Conference Presentation)," in *Proc. SPIE*, 2018, vol. 10585.
[149] C. A. Mack and B. Bunday, "CD-SEM algorithm optimization for line roughness metrology (Conference Presentation)," in *Proc. SPIE*, 2018, vol. 10585.
[150] H. Kawada, T. Kawasaki, J. Kakuta, T. Kondo, and M. Ikota, "How to measure a-few-nanometer-small LER occurring in EUV lithography processed feature," in *Proc. SPIE*, 2018, vol. 10585, p. 4.
[151] A. Liang *et al.*, "Unbiased roughness measurements: the key to better etch performance," in *Proc. SPIE*, 2018, vol. 10585, p. 9.
[152] K. Takamasu, S. Takahashi, H. Kawada, and M. Ikota, "Linewidth roughness of advanced semiconductor features using focused ion beam and planar-transmission electron microscope as reference metrology," *J. of Micro/Nanolithography, MEMS, and MOEMS,* vol. 17, no. 4, p. 7, 2018.
[153] J. Reche, M. Besacier, P. Gergaud, Y. Blancquaert, G. Freychet, and T. Labbaye, "Programmed line width roughness metrology by multitechniques approach," *J. of Micro/Nanolithography, MEMS, and MOEMS,* vol. 17, no. 4, p. 10, 2018.
[154] C. A. Mack, "Reducing roughness in extreme ultraviolet lithography," *J. of Micro/Nanolithography, MEMS, and MOEMS,* vol. 17, no. 4, p. 8, 2018.
[155] C. A. Mack and G. F. Lorusso, "Determining the ultimate resolution of scanning electron microscope-based unbiased roughness measurements. I. Simulating noise," *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena,* vol. 37, no. 6, p. 062903, 2019.
[156] M. Abaidi *et al.*, "Determining the validity domain of roughness measurements as a function of CD-SEM acquisition conditions," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2584040. [Online]. Available: https://doi.org/10.1117/12.2584040
[157] Y. Bian *et al.*, "Effects of lithography process conditions on unbiased line roughness by PSD analysis," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2583545. [Online]. Available: https://doi.org/10.1117/12.2583545
[158] G. Papavieros, V. Constantoudis, and E. Gogolides, Pixelization effect in SEM images: investigating the effect of the selected pixel size on LER measurement (SPIE Advanced Lithography). SPIE, 2021.
[159] B. Bunday *et al.*, "Impact of sampling on uncertainty: semiconductor dimensional metrology applications," in *Proc. SPIE*, 2008/03/14 2008: SPIE, doi: 10.1117/12.772993. [Online]. Available: http://dx.doi.org/10.1117/12.772993
[160] A. Vaid *et al.*, "Hybrid metrology: from the lab into the fab," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 13, no. 4, p. 041410, 2014/11/06 2014, doi: 10.1117/1.jmm.13.4.041410.
[161] R. Dixson and N. G. Orji, "Comparison and uncertainties of standards for critical dimension atomic force microscope tip width calibration," *Proc Spie,* vol. 6518, 2007, doi: 10.1117/12.714032.
[162] N. G. Orji *et al.*, "Transmission electron microscope calibration methods for critical dimension standards," *J Micro-Nanolith Mem,* vol. 15, no. 4, 2016, doi: Artn 044002 10.1117/1.Jmm.15.4.044002.
[163] G. Witvoet, J. Peters, S. Kuiper, S. Keyvani, and R. Willekers, "First results from the Large Dynamic Range Atomic Force Microscope for overlay metrology," in *Proc. SPIE*, 2019, vol. 10959: International Society for Optics and Photonics, p. 109592E.
[164] K. Bhattacharyya, "Tough road ahead for device overlay and edge placement error," in *Proc. SPIE*, 2019, vol. 10959: International Society for Optics and Photonics, p. 1095902.
[165] A. Cherala *et al.*, "Topography and flatness induced overlay distortion correction using resist drop pattern compensation in nanoimprint lithography systems," in *Proc. SPIE*, 2019, vol. 10958: International Society for Optics and Photonics, p. 109580C.
[166] A. H. Gabor and N. M. Felix, "Overlay error statistics for multiple-exposure patterning," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 18, no. 2, p. 021202, 2019.
[167] R. Gronheid *et al.*, "Overlay error investigation for metal containing resist," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 18, no. 4, p. 044001, 2019.
[168] O. Inoue and K. Hasumi, "Review of scanning electron microscope-based overlay measurement beyond 3-nm node device," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 18, no. 2, p. 021206, 2019.

[169] H. Lee *et al.*, "Improved accuracy and robustness for advanced DRAM with tunable multi-wavelength imaging and scatterometry overlay metrology," in *Proc. SPIE*, 2019, vol. 10959: International Society for Optics and Photonics, p. 109591E.
[170] H.-G. Lee *et al.*, "Measuring after etch overlay and characterizing tilt fingerprints in multi-tier 3D-NAND structures," in *Proc. SPIE*, 2019, vol. 10959: International Society for Optics and Photonics, p. 1095907.
[171] O. Morimoto *et al.*, "Patterning, mask life, throughput and overlay improvements for high volume semiconductor manufacturing using nanoimprint lithography," in *Proc. SPIE*, 2019, vol. 11148: International Society for Optics and Photonics, p. 111480M.
[172] D. Schmidt, R. Cornell, M. Kling, A. Gabor, and C. Ausschnitt, "Characterization of EUV image fading induced by overlay corrections using pattern shift response metrology," in *Proc. SPIE*, 2019, vol. 11147: International Society for Optics and Photonics, p. 1114713.
[173] Y. Sufrin, P. Leray, E. Canga, A. Cohen, V. Dmitriev, and K. Gorhad, "Enhanced wafer overlay residuals control: deep sub-nanometer at sub-millimeter lateral resolution," in *Proc. SPIE*, 2019, vol. 11177: International Society for Optics and Photonics, p. 111770J.
[174] R. van Haren *et al.*, "The impact of the reticle and wafer alignment mark placement accuracy on the intra-field mask-to-mask overlay," in *Proc. SPIE*, 2019, vol. 11178: International Society for Optics and Photonics, p. 111780R.
[175] R. van Haren *et al.*, "Wafer alignment mark placement accuracy impact on the layer-to-layer overlay performance," in *Proc. SPIE*, 2019, vol. 11148: International Society for Optics and Photonics, p. 1114811.
[176] O. Inoue, "Review of scanning electron microscope-based overlay measurement," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2585880. [Online]. Available: https://doi.org/10.1117/12.2585880
[177] S. Katz, Y. Grauer, R. Yohanan, X. Liu, D. Negri, and A. Golotsvan, "Accuracy enhancement in imaging based overlay metrology by optimizing measurement conditions per layer," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2583615. [Online]. Available: https://doi.org/10.1117/12.2583615
[178] Y.-L. Liu *et al.*, "Imaging-based overlay metrology optimized by HV-SEM in 3D-NAND process," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2583609. [Online]. Available: https://doi.org/10.1117/12.2583609
[179] L. Tu *et al.*, "A novel method of overlay variation study for 3D NAND channel hole," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2583760. [Online]. Available: https://doi.org/10.1117/12.2583760
[180] P. Zhang *et al.*, "An accurate and robust after-develop overlay measurement solution using YieldStar multi-wavelength optical metrology accompanied by a precise application strategy," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2583737. [Online]. Available: https://doi.org/10.1117/12.2583737
[181] Guide to the expression of uncertainty in measurement — Part 6: Developing and using measurement models, JCGM GUM-6:2020, W. G. o. t. J. C. f. G. i. M. J. W. 1). 2020.
[182] H.-G. Lee *et al.*, "Virtual overlay metrology for fault detection supported with integrated metrology and machine learning," in *Proc. SPIE*, 2015, vol. 9424: SPIE, p. 6.
[183] K. Bhattacharyya and A. d. Boef, "Holistic Metrology Approaches For Improved Device Overlay And Edge Placement Error," in *Frontiers of Characterization and Metrology for Nanoelectronics*, 2019: NIST.
[184] P. R. Chidambaram, C. Bowen, S. Chakravarthi, C. Machala, and R. Wise, "Fundamentals of silicon material properties for successful exploitation of strain engineering in modern CMOS manufacturing," *IEEE Transactions on Electron Devices,* vol. 53, no. 5, pp. 944-964, 2006, doi: 10.1109/TED.2006.872912.
[185] *International technology roadmap for semiconductors*, 2011 ed. San Jose, Calif.: Semiconductor Industry Association, 2011.
[186] T. Nuytten *et al.*, "Raman Stress Measurements at the Nanoscale," *ECS Transactions,* vol. 86, no. 7, pp. 311-320, 2018.
[187] M. Kuhn *et al.*, "Transistor Strain Measurement Techniques and Their Applications," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 207-376.
[188] D. Schmidt *et al.*, "In-line Raman spectroscopy for gate-all-around nanosheet device manufacturing," *Journal of Micro/Nanopatterning, Materials, and Metrology,* vol. 21, no. 2, p. 021203, 2022. [Online]. Available: https://doi.org/10.1117/1.JMM.21.2.021203.

[189] W. Vandervorst *et al.*, "Dopant, composition and carrier profiling for 3D structures," *Materials Science in Semiconductor Processing,* vol. 62, pp. 31-48, 2017/05/01/ 2017, doi: https://doi.org/10.1016/j.mssp.2016.10.029.
[190] P. Eyben, R. Ritzenthale, U. Celano, T. Chiarella, and A. Veloso, "3D-carrier Profiling and Parasitic Resistance Analysis in Vertically Stacked Gate-All-Around Si Nanowire CMOS Transistors," in *IEDM*, 2019.
[191] A. Schulze *et al.*, "Quantitative three-dimensional carrier mapping in nanowire-based transistors using scanning spreading resistance microscopy," *Ultramicroscopy,* vol. 125, pp. 18-23, 2013/02 2013, doi: 10.1016/j.ultramic.2012.10.008.
[192] A. Schulze, P. Eyben, T. Hantschel, and W. Vandervorst, "Scanning Spreading Resistance Microscopy (SSRM): High-Resolution 2D and 3D Carrier Mapping of Semiconductor Nanostructures," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 377-445.
[193] T. Kelly and K. Henry, "Atom Probe Tomography of Semiconductor Nanostructures," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 711-756.
[194] P. Parikh *et al.*, "Three-dimensional nanoscale mapping of state-of-the-art field-effect transistors (FinFETs)," *Microscopy and Microanalysis,* vol. 23, no. 5, pp. 916-925, 2017.
[195] K. Nikawa, "Introduction to Panel Discussion: Dopant Visualization," in *NANO Testing Symposium* 2015, pp. 275-280
[196] A. Schulze *et al.*, "Mapping Conductance and Carrier Distributions in Confined Three-Dimensional Transistor Structures," in *Electrical Atomic Force Microscopy for Nanoelectronics*: Springer, 2019, pp. 71-106.
[197] Y. Cho, "High resolution characterizations of fine structure of semiconductor device and material using scanning nonlinear dielectric microscopy," *Japanese Journal of Applied Physics,* vol. 56, no. 10, p. 100101, 2017.
[198] W. Zhou, M. Varela, J.-C. Idrobo, S. Pantelides, and S. Pennycook, "Electron Energy Loss Spectroscopy of Semiconductor Nanostructures and Oxides," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds.: Pan Stanford, 2017, pp. 663-709.
[199] R. Dias and D. Goyal, "Methodology and Challenges in Characterization of 3D Package Interconnection Materials and Processes," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 1089-1119.
[200] I. DeWolf, "3D Interconnect Characterization Using Raman Spectroscopy," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 1121-1146.
[201] W. Yun *et al.*, "Advances in 3D Interconnect Characterization Techniques for Fault Isolation and Defect Imaging," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 1147-1272.
[202] S. Borel, M. Assous, S. Moreau, and R. Velard, "Recent Progress in the Development of High-Density TSV for 3-Layers CMOS Image Sensors," in *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*, 30 May-2 June 2023 2023, pp. 1156-1163, doi: 10.1109/ECTC51909.2023.00198.
[203] K. J. Chui *et al.*, "A 2-tier Embedded 3D Capacitor with High Aspect Ratio TSV," in *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, 3-30 June 2020 2020, pp. 611-616, doi: 10.1109/ECTC32862.2020.00101.
[204] A. Jourdain *et al.*, "Extreme Wafer Thinning and nano-TSV processing for 3D Heterogeneous Integration," in *2020 IEEE 70th Electronic Components and Technology Conference (ECTC)*, 3-30 June 2020 2020, pp. 42-48, doi: 10.1109/ECTC32862.2020.00020.
[205] C. Okoro *et al.*, "X-ray micro-beam diffraction determination of full stress tensors in Cu TSVs," in *2013 IEEE 63rd Electronic Components and Technology Conference*, 28-31 May 2013 2013, pp. 648-652, doi: 10.1109/ECTC.2013.6575642.
[206] SEMI MS5-1107 Test Method for Wafer Bond Strength Measurements using Micro-Chevron Test Structures SEMI MS5-1107, SEMI, Milpitas, CA, 2013.
[207] L. Colonel *et al.*, "Double cantilever beam bonding energy measurement using confocal IR microscopy," *Journal of Applied Physics,* vol. 132, no. 21, 2022, doi: 10.1063/5.0114668.
[208] Y. Qu, J. Hao, and R. Peng, "Machine-learning models for analyzing TSOM images of nanostructures," *Optics Express,* vol. 27, no. 23, pp. 33978-33998, 2019/11/11 2019, doi: 10.1364/OE.27.033978.

[209] S.-w. Park, G. Park, Y. Kim, J. H. Cho, J. Lee, and H. Kim, "Through-focus scanning optical microscopy with the Fourier modal method," *Optics Express,* vol. 26, no. 9, pp. 11649-11657, 2018/04/30 2018, doi: 10.1364/OE.26.011649.

[210] R. K. Attota, H. Kang, K. Scott, R. Allen, A. E. Vladar, and B. Bunday, "Nondestructive shape process monitoring of three-dimensional, high-aspect-ratio targets using through-focus scanning optical microscopy," *Measurement Science and Technology,* vol. 29, no. 12, p. 125007, 2018/11/05 2018, doi: 10.1088/1361-6501/aae4c2.

[211] R. Attota, "Through-focus or volumetric type of optical imaging methods: a review," *Journal of Biomedical Optics,* vol. 23, no. 7, pp. 19100-19114 2018.

[212] R. Attota and R. Silver, "Nanometrology using a through-focus scanning optical microscopy method," (in English), *Meas Sci Technol,* vol. 22, no. 2, Feb 2011, doi: Artn 024002 10.1088/0957-0233/22/2/024002.

[213] R. Attota and R. G. Dixson, "Resolving three-dimensional shape of sub-50 nm wide lines with nanometer-scale sensitivity using conventional optical microscopes," (in English), *Applied Physics Letters,* vol. 105, no. 4, Jul 28 2014, doi: Artn 043101 10.1063/1.4891676.

[214] J. Marro, C. Okoro, Y. Obeng, and K. Richardson, "Defect and microstructural evolution in thermally cycled Cu through-silicon vias," *Microelectronics Reliability,* vol. 54, no. 11, pp. 2586-2593, 2014/11/01/ 2014, doi: https://doi.org/10.1016/j.microrel.2014.05.007.

[215] W. Fuliang and W. Feng, "Rapidly Void Detection in TSVs With 2-D X-Ray Imaging and Artificial Neural Networks," *IEEE Transactions on Semiconductor Manufacturing,* vol. 27, no. 2, pp. 246-251, 2014/05 2014, doi: 10.1109/tsm.2014.2309591.

[216] H. Xin, S. Vishnubhotla, and R. Lin, "3D Electron Tomography for Nanostructures," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 637-662.

[217] D. Priyadarshini et al., "Advanced single precursor based pSiCOH k = 2.4 for ULSI interconnects," Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena, vol. 35, no. 2, p. 021201, 2017/03 2017, doi: 10.1116/1.4974317.

[218] C. E. Sunday, K. R. Montgomery, P. K. Amoah, and Y. S. Obeng, "Broadband Dielectric Spectroscopic Characterization of Thermal Stability of Low-k Dielectric Thin Films for Micro- and Nanoelectronic Applications," *ECS Journal of Solid State Science and Technology,* vol. 6, no. 9, pp. N155-N162, 2017, doi: 10.1149/2.0141709jss.

[219] J. Weiss, J. Ganesh, A. Darbal, J. Zhang, D. Xu, and E. Rauch, "Microstructure Characterization of Nanoscale Materials and Interconnects," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 447-492.

[220] Y. Zhou and H. Li, "Characterization of the Chemistry and Mechanical Properties of Interconnect Materials and Interfaces: Impact on Interconnect Reliability," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 493-539.

[221] R. C. Hedden, H.-J. Lee, C. L. Soles, and B. J. Bauer, "Characterization of Pore Structure in a Nanoporous Low-Dielectric-Constant Thin Film by Neutron Porosimetry and X-ray Porosimetry," *Langmuir,* vol. 20, no. 16, pp. 6658-6667, 2004/08/01 2004, doi: 10.1021/la036334u.

[222] H.-J. Lee *et al.*, "Structural characterization of porous low-k thin films prepared by different techniques using x-ray porosimetry," *Journal of Applied Physics,* vol. 95, no. 5, pp. 2355-2359, 2004, doi: 10.1063/1.1641955.

[223] N. Orji and R. Dixson, "3D-AFM Measurements for Semiconductor Structures and Devices," in *Metrology and Diagnostic Techniques for Nanoelectronics*, Z. Ma and D. G. Seiler Eds. New York: Pan Stanford, 2017, pp. 109-152.

[224] D. F. Sunday *et al.*, "Characterizing the Interface Scaling of High χ Block Copolymers near the Order–Disorder Transition," *Macromolecules,* vol. 51, no. 1, pp. 173-180, 2018/01/09 2018, doi: 10.1021/acs.macromol.7b01982.

[225] D. F. Sunday *et al.*, "Quantifying the Interface Energy of Block Copolymer Top Coats," *ACS Macro Letters,* vol. 5, no. 12, pp. 1306-1311, 2016/12/20 2016, doi: 10.1021/acsmacrolett.6b00684.

[226] T. F. Kelly, M. K. Miller, K. Rajan, and S. P. Ringer, "Atomic-Scale Tomography: A 2020 Vision," *Microscopy and Microanalysis,* vol. 19, no. 03, pp. 652-664, 2013/05/13 2013, doi: 10.1017/s1431927613000494.

[227] J. C. Meyer, C. Kisielowski, R. Erni, M. D. Rossell, M. F. Crommie, and A. Zettl, "Direct Imaging of Lattice Atoms and Topological Defects in Graphene Membranes," *Nano Letters,* vol. 8, no. 11, pp. 3582-3586, 2008/11/12 2008, doi: 10.1021/nl801386m.

[228] J. H. Warner, M. H. Rümmeli, T. Gemming, B. Büchner, and G. A. D. Briggs, "Direct Imaging of Rotational Stacking Faults in Few Layer Graphene," *Nano Letters,* vol. 9, no. 1, pp. 102-106, 2009/01/14 2009, doi: 10.1021/nl8025949.

[229] V. A. Ukraintsev, N. G. Orji, T. V. Vorburger, R. G. Dixson, J. Fu, and R. M. Silver, "Distributed force probe bending model of critical dimension atomic force microscopy bias," *J Micro-Nanolith Mem,* vol. 12, no. 2, 2013, doi: Artn 023009 10.1117/1.Jmm.12.2.023009.

[230] J. Choi *et al.*, "Evaluation of carbon nanotube probes in critical dimension atomic force microscopes," *J Micro-Nanolith Mem,* vol. 15, no. 3, 2016, doi: 10.1117/1.Jmm.15.3.034005.

[231] S. Mayo, P. Miller, D. Gao, and J. Sheffield-Parker, "Software image alignment for X-ray microtomography with submicrometre resolution using a SEM-based X-ray microscope," *Journal of Microscopy,* vol. 228, no. 3, pp. 257-263, 2007/12 2007, doi: 10.1111/j.1365-2818.2007.01857.x.

[232] N. G. Orji *et al.*, "Tip characterization method using multi-feature characterizer for CD-AFM," *Ultramicroscopy,* vol. 162, pp. 25-34, 2016, doi: 10.1016/j.ultramic.2015.12.003.

[233] G. Dahlen, M. Osborn, N. Okulan, W. Foreman, A. Chand, and J. Foucher, "Tip characterization and surface reconstruction of complex structures with critical dimension atomic force microscopy," (in English), *J Vac Sci Technol B,* vol. 23, no. 6, pp. 2297-2303, Nov-Dec 2005, doi: 10.1116/1.2101601.

[234] S. Babin *et al.*, "1.5nm fabrication of test patterns for characterization of metrological systems," in *Proc. SPIE*, 2017: SPIE, doi: 10.1117/12.2257624.

[235] R. Dixson *et al.*, "Multilaboratory comparison of traceable atomic force microscope measurements of a 70-nm grating pitch standard," (in English), *J Micro-Nanolith Mem,* vol. 10, no. 1, Jan-Mar 2011, doi: 10.1117/1.3549914.

[236] L. Yang, C. D. Spataru, S. G. Louie, and M. Y. Chou, "Enhanced electron-hole interaction and optical absorption in a silicon nanowire," *Physical Review B,* vol. 75, no. 20, 2007/05/23 2007, doi: 10.1103/physrevb.75.201304.

[237] J. Chen, "Large On-Off Ratios and Negative Differential Resistance in a Molecular Electronic Device," *Science,* vol. 286, no. 5444, pp. 1550-1552, 1999/11/19 1999, doi: 10.1126/science.286.5444.1550.

[238] C. P. Collier, "A [2]Catenane-Based Solid State Electronically Reconfigurable Switch," *Science,* vol. 289, no. 5482, pp. 1172-1175, 2000/08/18 2000, doi: 10.1126/science.289.5482.1172.

[239] C. A. Richter, D. R. Stewart, D. A. A. Ohlberg, and R. S. Williams, "Electrical characterization of Al/AlOx/molecule/Ti/Al devices," *Applied Physics A,* vol. 80, no. 6, pp. 1355-1362, 2005/03 2005, doi: 10.1007/s00339-004-3169-x.

[240] S.-M. Koo, A. Fujiwara, J.-P. Han, E. M. Vogel, C. A. Richter, and J. E. Bonevich, "High Inversion Current in Silicon Nanowire Field Effect Transistors," *Nano Letters,* vol. 4, no. 11, pp. 2197-2201, 2004/11 2004, doi: 10.1021/nl0486517.

[241] J. Fang, W. G. Vandenberghe, and M. V. Fischetti, "Microscopic dielectric permittivities of graphene nanoribbons and graphene," *Physical Review B,* vol. 94, no. 4, 2016/07/28 2016, doi: 10.1103/physrevb.94.045318.

[242] F. Kremer and A. Schönhals, *Broadband dielectric spectroscopy*. Berlin ; New York: Springer, 2003, pp. xxi, 729 p.

[243] S. Deleonibus, "Nanoelectronics and Diversification in the 3D technologies era," in *IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC)*, 2012/12 2012: IEEE, doi: 10.1109/edssc.2012.6482878. [Online]. Available: http://dx.doi.org/10.1109/edssc.2012.6482878

[244] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Transactions on Electron Devices,* vol. 59, no. 7, pp. 1813-1828, 2012/07 2012, doi: 10.1109/ted.2012.2193129.

[245] V. Delaye *et al.*, "In-line transmission electron microscopy for micro and nanotechnologies research and development," *Microelectronic Engineering,* vol. 85, no. 5-6, pp. 1157-1161, 2008/05 2008, doi: 10.1016/j.mee.2008.01.092.

[246] M. Strauss and M. Williamson, "Automated transmission electron microscopy for defect review and metrology of Si devices," in *ASMC 2013 SEMI Advanced Semiconductor Manufacturing Conference*, 2013/05 2013: IEEE, doi: 10.1109/asmc.2013.6552761. [Online]. Available: http://dx.doi.org/10.1109/asmc.2013.6552761

[247] P. van der Heide, I. Mathotkin, W. Vandervorst, and C. Fleischmann, "APT Tip Shape Modifications During Analysis, Its Implications, and the Potential to Measure Tip Shapes in Real Time via Soft-X-Ray Ptychography," *Microscopy and Microanalysis,* vol. 25, no. S2, pp. 2504-2505, 2019, doi: 10.1017/S1431927619013254.

[248] L. J. Allen, A. J. D'Alfonso, S. D. Findlay, J. M. LeBeau, N. R. Lugg, and S. Stemmer, "Elemental mapping in scanning transmission electron microscopy," *Journal of Physics: Conference Series,* vol. 241, p. 012061, 2010/07/01 2010, doi: 10.1088/1742-6596/241/1/012061.
[249] A. Genc *et al.*, "XEDS STEM tomography for 3D chemical characterization of nanoscale particles," *Ultramicroscopy,* vol. 131, pp. 24-32, 2013/08 2013, doi: 10.1016/j.ultramic.2013.03.023.
[250] C. Song *et al.*, "Nanoscale Imaging of Buried Structures with Elemental Specificity Using Resonant X-Ray Diffraction Microscopy," *Physical Review Letters,* vol. 100, no. 2, 2008/01/18 2008, doi: 10.1103/physrevlett.100.025504.
[251] Y. Takahashi, A. Suzuki, S. Furutaku, K. Yamauchi, Y. Kohmura, and T. Ishikawa, "Bragg x-ray ptychography of a silicon crystal: Visualization of the dislocation strain field and the production of a vortex beam," *Physical Review B,* vol. 87, no. 12, p. 121201, 2013.
[252] A. Béché, J. L. Rouvière, J. P. Barnes, and D. Cooper, "Dark field electron holography for strain measurement," *Ultramicroscopy,* vol. 111, no. 3, pp. 227-238, 2011/02 2011, doi: 10.1016/j.ultramic.2010.11.030.
[253] D. Cooper, C. Le Royer, A. Béché, and J.-L. Rouvière, "Strain mapping for the silicon-on-insulator generation of semiconductor devices by high-angle annular dark field scanning electron transmission microscopy," *Applied Physics Letters,* vol. 100, no. 23, p. 233121, 2012/06/04 2012, doi: 10.1063/1.4723572.
[254] M. P. Vigouroux *et al.*, "Strain mapping at the nanoscale using precession electron diffraction in transmission electron microscope with off axis camera," *Applied Physics Letters,* vol. 105, no. 19, p. 191906, 2014/11/10 2014, doi: 10.1063/1.4901435.
[255] J.-L. Rouviere, A. Béché, Y. Martin, T. Denneulin, and D. Cooper, "Improved strain precision with high spatial resolution using nanobeam precession electron diffraction," *Applied Physics Letters,* vol. 103, no. 24, p. 241913, 2013/12/09 2013, doi: 10.1063/1.4829154.
[256] D. Cooper, N. Bernier, and J.-L. Rouvière, "Combining 2 nm Spatial Resolution and 0.02% Precision for Deformation Mapping of Semiconductor Specimens in a Transmission Electron Microscope by Precession Electron Diffraction," *Nano Letters,* vol. 15, no. 8, pp. 5289-5294, 2015/07/30 2015, doi: 10.1021/acs.nanolett.5b01614.
[257] C. Mahr *et al.*, "Theoretical study of precision and accuracy of strain analysis by nano-beam electron diffraction," *Ultramicroscopy,* vol. 158, pp. 38-48, 2015/11 2015, doi: 10.1016/j.ultramic.2015.06.011.
[258] J. Mody *et al.*, "3D-Carrier Profiling in FinFETs using Scanning Spreading Resistance Microscopy," *2011 IEEE International Electron Devices Meeting (IEDM),* 2011.
[259] U. Celano *et al.*, "Three-Dimensional Observation of the Conductive Filament in Nanoscaled Resistive Memory Devices," *Nano Letters,* vol. 14, no. 5, pp. 2401-2406, 2014/04/10 2014, doi: 10.1021/nl500049g.
[260] U. Celano *et al.*, "Progressive vs. abrupt reset behavior in conductive bridging devices: A C-AFM tomography study," in *2014 IEEE International Electron Devices Meeting*, 2014/12 2014: IEEE, doi: 10.1109/iedm.2014.7047048. [Online]. Available: http://dx.doi.org/10.1109/iedm.2014.7047048
[261] U. Celano *et al.*, "Non-filamentary (VMCO) memory: A two-and three-dimensional study on switching and failure modes," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2-6 Dec. 2017 2017, pp. 39.1.1-39.1.4, doi: 10.1109/IEDM.2017.8268519.
[262] A. Schulze, R. Cao, P. Eyben, T. Hantschel, and W. Vandervorst, "Outwitting the series resistance in scanning spreading resistance microscopy," *Ultramicroscopy,* vol. 161, pp. 59-65, 2016/02 2016, doi: 10.1016/j.ultramic.2015.10.029.
[263] P. Bleuet *et al.*, "Specifications for Hard Condensed Matter Specimens for Three-Dimensional High-Resolution Tomographies," *Microscopy and Microanalysis,* vol. 19, no. 03, pp. 726-739, 2013/04/10 2013, doi: 10.1017/s1431927613000330.
[264] G. Martínez-Criado *et al.*, "Status of the hard X-ray microprobe beamline ID22 of the European Synchrotron Radiation Facility," *Journal of Synchrotron Radiation,* vol. 19, no. 1, pp. 10-18, 2011/11/15 2011, doi: 10.1107/s090904951104249x.
[265] G. Haberfehlner *et al.*, "Four-dimensional spectral low-loss energy-filtered transmission electron tomography of silicon nanowire-based capacitors," *Applied Physics Letters,* vol. 101, no. 6, p. 063108, 2012/08/06 2012, doi: 10.1063/1.4742932.
[266] P. A. Midgley and R. E. Dunin-Borkowski, "Electron tomography and holography in materials science," *Nature Materials,* vol. 8, no. 4, pp. 271-280, 2009/04 2009, doi: 10.1038/nmat2406.

[267] H. L. Xin and D. A. Muller, "Aberration-corrected ADF-STEM depth sectioning and prospects for reliable 3D imaging in S/TEM," *Journal of Electron Microscopy,* vol. 58, no. 3, pp. 157-165, 2009/01/22 2009, doi: 10.1093/jmicro/dfn029.
[268] S. Bals, S. Van Aert, and G. Van Tendeloo, "High resolution electron tomography," *Current Opinion in Solid State and Materials Science,* vol. 17, no. 3, pp. 107-114, 2013/06 2013, doi: 10.1016/j.cossms.2013.03.001.
[269] M. Cantoni, G. Knott, and C. Hébert, "FIB-SEM Nanotomography in Materials and Life Science at EPFL," *Microscopy and Microanalysis,* vol. 16, no. S2, pp. 226-227, 2010/07 2010, doi: 10.1017/s1431927610059623.
[270] G. D. West and R. C. Thomson, "Combined EBSD/EDS tomography in a dual-beam FIB/FEG-SEM," *Journal of Microscopy,* vol. 233, no. 3, pp. 442-450, 2009/03 2009, doi: 10.1111/j.1365-2818.2009.03138.x.
[271] U. Celano *et al.*, "Individual Device Analysis Using Hybrid TEM-Scalpel SSRM Metrology," in *Frontiers of Characterization and Metrology for Nanoelectronics*, E. M. Secula and D. G. Seiler Eds., 2017.
[272] B. Gault *et al.*, "Design of a femtosecond laser assisted tomographic atom probe," *Review of Scientific Instruments,* vol. 77, no. 4, p. 043705, 2006/04 2006, doi: 10.1063/1.2194089.
[273] R. Pandey *et al.*, "Tunnel Junction Abruptness, Source Random Dopant Fluctuation and PBTI Induced Variability Analysis of GaAs0.4Sb0.6/In0.65Ga0.35As Heterojunction Tunnel FETs," in *IEEE International Electron Devices Meeting (IEDM)*, 2015.
[274] T. F. Kelly, "Atom-Probe Tomography," in *Springer Handbook of Microscopy*, P. W. Hawkes and J. C. H. Spence Eds. Cham: Springer International Publishing, 2019.
[275] F. A. Stevie, L. Sedlacek, P. Babor, J. Jiruse, E. Principe, and K. Klosova, "FIB-SIMS quantification using TOF-SIMS with Ar and Xe plasma sources," *Surface and Interface Analysis,* vol. 46, no. S1, pp. 285-287, 2014/03/21 2014, doi: 10.1002/sia.5483.
[276] I. Holfelder *et al.*, "Complementary methodologies for thin film characterization in one tool – a novel instrument for 450 mm wafers," *Journal of Analytical Atomic Spectrometry,* vol. 28, no. 4, p. 549, 2013, doi: 10.1039/c3ja30324a.
[277] D. Le Cunff *et al.*, "Combining metrology techniques for in-line control of thin SiGe:B layers," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 13, no. 4, p. 041402, 2014/09/15 2014, doi: 10.1117/1.jmm.13.4.041402.
[278] N. G. Orji, "Progress on implementation of a reference measurement system based on a critical-dimension atomic force microscope," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 6, no. 2, p. 023002, 2007/04/01 2007, doi: 10.1117/1.2728742.
[279] N. G. Orji, "Measurement traceability and quality assurance in a nanomanufacturing environment," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 10, no. 1, p. 013006, 2011/01/01 2011, doi: 10.1117/1.3549736.
[280] A. Vaid and E. Solecky, "Special Section Guest Editorial: Holistic/Hybrid Metrology," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 13, no. 4, p. 041401, 2014/12/19 2014, doi: 10.1117/1.jmm.13.4.041401.
[281] A. Grenier *et al.*, "Three dimensional imaging and analysis of a single nano-device at the ultimate scale using correlative microscopy techniques," *Applied Physics Letters,* vol. 106, no. 21, p. 213102, 2015/05/25 2015, doi: 10.1063/1.4921352.
[282] R. Dixson, N. Orji, I. Misumi, and G. Dai, "Spatial dimensions in atomic force microscopy: Instruments, effects, and measurements," *Ultramicroscopy,* vol. 194, pp. 199-214, Aug 15 2018, doi: 10.1016/j.ultramic.2018.08.011.
[283] M.-A. Henn, B. M. Barnes, N. F. Zhang, H. Zhou, and R. M. Silver, "The effect of systematic errors on the hybridization of optical critical dimension measurements," in *Modeling Aspects in Optical Metrology V*, 2015/06/21 2015: SPIE, doi: 10.1117/12.2189928. [Online]. Available: http://dx.doi.org/10.1117/12.2189928
[284] SEMI E133-1014 -SEMI Standard Specification for Automated Process Control Systems Interface, SEMI E133-101, SEMI, Milpitas, CA, 2014.
[285] N. G. Orji, Y. S. Obeng, C. Beitia, S. Mashiro, and J. R. Moyne, "Virtual Metrology White Paper - INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS(IRDS)," 2018.
[286] P. Yang *et al.*, "Inter/intra-chip optical interconnection network: opportunities, challenges, and implementations," in *2016 Tenth IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, Aug. 31 2016-Sept. 2 2016 2016, pp. 1-8, doi: 10.1109/NOCS.2016.7579343.

[287] K. A. Brown, S. Brittman, N. Maccaferri, D. Jariwala, and U. Celano, "Machine Learning in Nanoscience: Big Data at Small Scales," *Nano Letters,* 2019/12/05 2019, doi: 10.1021/acs.nanolett.9b04090.
[288] P. Timoney *et al.*, "Implementation of machine learning for high-volume manufacturing metrology challenges (Conference Presentation)," in *SPIE Advanced Lithography*, 2018, vol. 10585, p. 8.
[289] N. Rana and C. Chien, "Deep machine learning based Image classification in hard disk drive manufacturing (Conference Presentation)," in *Proc. SPIE*, 2018, vol. 10585.
[290] J. Foucher, J. Baderot, S. Martinez, A. Dervilllé, and G. Bernard, "Cognitive learning: a machine learning approach for automatic process characterization from design," in *Proc. SPIE*, 2018, vol. 10585, p. 6.
[291] N. Rana, Y. Zhang, T. Kagalwala, and T. Bailey, "Leveraging advanced data analytics, machine learning, and metrology models to enable critical dimension metrology solutions for advanced integrated circuit nodes," *Journal of Micro/Nanolithography, MEMS, and MOEMS,* vol. 13, no. 4, p. 041415, 2014/12/29 2014, doi: 10.1117/1.jmm.13.4.041415.
[292] N. Rana, Y. L. Zhang, D. Wall, B. Dirahoui, and T. Bailey, "Machine Learning and Predictive Data Analytics Enabling Metrology and Process Control in IC Fabrication," *Proc Spie,* vol. 9424, 2015, doi: 10.1117/12.2087406.
[293] E. Solecky *et al.*, "New Techniques in Large Scale Metrology Toolset Data Mining to Accelerate Integrated Chip Technology Development and Increase Manufacturing Efficiencies," in *Proc. SPIE*, 2014, vol. 9050, doi: 10.1117/12.2046274. [Online]. Available: http://dx.doi.org/10.1117/12.2046274
[294] P. Ebersbach, A. M. Urbanowicz, D. Likhachev, C. Hartig, and M. Shifrin, "Context-based virtual metrology," in *Proc. SPIE*, 2018, vol. 10585, p. 13.
[295] W. Sun, Y. Goto, T. Yamamoto, and K. Hitomi, "Evaluation of deep learning model for 3D profiling of HAR features using high-voltage CD-SEM," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2592052. [Online]. Available: https://doi.org/10.1117/12.2592052
[296] A. Zandiatashbar *et al.*, "Introducing machine learning-based application for writer main pole CD metrology by dual beam FIB/SEM," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2583746. [Online]. Available: https://doi.org/10.1117/12.2583746
[297] T. jo *et al.*, "Machine learning aided process control: critical dimension uniformity control of etching process in 1z nm DRAM," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2583473. [Online]. Available: https://doi.org/10.1117/12.2583473
[298] T. Kondo *et al.*, "Massive metrology and inspection solution for EUV by area inspection SEM with machine learning technology," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2583691. [Online]. Available: https://doi.org/10.1117/12.2583691
[299] B. Dey *et al.*, "SEM image denoising with unsupervised machine learning for better defect inspection and metrology," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2584803. [Online]. Available: https://doi.org/10.1117/12.2584803
[300] M. Chastan, A. Lam, and F. Iutzeler, "Unsupervised density based machine learning for abnormal leveling signatures detection," in *Proc. SPIE*, 2021, vol. 11611: SPIE. [Online]. Available: https://doi.org/10.1117/12.2581468. [Online]. Available: https://doi.org/10.1117/12.2581468
[301] S. Vedantam, H. Lee, J. Tang, J. Conway, M. Staffaroni, and E. Yablonovitch, "A Plasmonic Dimple Lens for Nanoscale Focusing of Light," *Nano Letters,* vol. 9, no. 10, pp. 3447-3452, Oct 2009, doi: 10.1021/nl9016368.
[302] W. R. Legant *et al.*, "High-density three-dimensional localization microscopy across large volumes," *Nat Methods,* vol. 13, no. 4, pp. 359-365, Apr 2016, doi: 10.1038/Nmeth.3797.
[303] M. Holler *et al.*, "High-resolution non-destructive three-dimensional imaging of integrated circuits," *Nature,* vol. 543, no. 7645, pp. 402-+, Mar 16 2017, doi: 10.1038/nature21698.
[304] M. Holler *et al.*, "Three-dimensional imaging of integrated circuits with macro- to nanoscale zoom," *Nature Electronics,* vol. 2, no. 10, pp. 464-470, 2019/10/01 2019, doi: 10.1038/s41928-019-0309-z.
[305] R. J. Kline, "Multiscale 3D X-ray imaging," *Nature Electronics,* vol. 2, no. 10, pp. 435-436, 2019/10/01 2019, doi: 10.1038/s41928-019-0320-4.

11. ACRONYMS

Acronym/ Abbreviation	*Definition*
3D NAND	three dimensional NAND memory (flash memory)
AFM	atomic force microscope, atomic force microscopy
AI	artificial intelligence
APC	advanced process control
APT	atom probe tomography
ARC	antireflective coating
ARPES	angle-resolved photoemission spectroscopy
As	arsenic
BDS	broadband dielectric spectroscopy
B	boron
BWP	bonded wafer pairs
CBED	convergent beam electron diffraction
CCD	charge coupled device
CD	critical dimension
CD-AFM	critical dimension-atomic force microscopy
CD-SAXS	critical dimension-small angle X-ray scattering
CD-SEM	critical dimension-scanning electron microscopy
CGS	coherent gradient sensing
CIM	computer integrated manufacturing
CMOS	complementary metal-oxide semiconductor
CMP	chemical mechanical polishing or chemical mechanical planarization
CRM	certified reference materials
CVS	cyclic voltammetric stripping
D2D	die to die
D2W	die to wafer
DBM	design-based metrology
DFM	design for manufacturing, design for manufacture, design for manufacturability
DLTS	deep level transient spectroscopy
DRAM	dynamic random access memory
DSA	directed self assembly
DWBA	distorted wave Born approximation
EBSEM	electron beam scanning electron microscopy
EBSD	electron backscatter diffraction
ECT	electro-capacitive tomography
EDS	energy dispersive X-ray spectroscopy, energy-dispersive spectroscopy, electron-dispersive spectroscopy; energy dispersive spectrometers
EELS	electron energy loss spectroscopy
ELS	energy loss spectroscopy
EPD	etch pit density
EPE	edge placement error
E-SEM	environmental-scanning electron microscopy
EUV	extreme ultra violet
EUVL	extreme ultra violet lithography
EUV AIMS	EUV aerial image measurements systems, aerial image microscope
EXAFS	extended X-ray absorption fine structure
FDSOI	fully depleted silicon-on-insulator
FE-AES	field emission auger electron spectroscopy
FEP	front end processes

FFT-SSRM	fast Fourier transform-scanning spreading resistance microscopy
FIB	focused ion beam
FinFET	fin structure field effect transistor
FMP	fleet matching precision
GAA	gate all around
GDS	graphic database system
GeSi	Ge rich silicon germanium
GI-SAXS	grazing incidence small angle X-ray scattering
HAADF	high angle annular dark field
HAR	high aspect ratio
HeIM	helium ion microscopy
HIM	helium ion microscopy
HVM	high volume manufacturing
HV-SEM	high voltage scanning electron microscopy
IC	integrated circuit
ICP-MS	ion coupled plasma mass spectrometry
IoT	Internet of Things
IP	intellectual property
IR	infrared
IRDS	International Roadmap for Devices and Systems
LER	line edge roughness
LGAA	lateral gate all around
LLBSE-SEM	low-loss backscattered electrons SEM
LWR	line width roughness, line width reduction
MBIR	model-based infrared
MEF	mask error factor, mask error factors, mask error fault
MFM	multiple feature measurement, mass flow meter
MOS	metal-oxide semiconductor; metal-oxide-silicon
NBD	nanobeam diffraction
NBED	nanobeam electron diffraction
NIST	National Institute of Standards and Technology
NMI	National Metrology Institutions
NMOS	negative channel metal-oxide semiconductor
N-PED or NPED	NBED in precession mode
NTRM	NIST traceable reference materials
OCD	optical critical dimension
OPC	optical proximity correction
OSC	outside systems connectivity
P	phosphorus
P/T	precision to tolerance
PMOR	photo modulated optical reflectance
PMOS	positive channel metal-oxide semiconductor
PSM	phase shift mask
RCWA	rigorous coupled wave analysis
RF	radio frequency
RMS	reference measurement system, root mean square;
SANS	small angle neutron scattering
SAM	scanning acoustic microscopy, scanning auger microscopy, scanning acoustical microscopy, self-assembled monolayer
SAXS	small angle X-ray scattering
SEM	scanning electron microscopy or scanning electron microscope
SIMS	secondary ion mass spectroscopy
SOI	silicon on insulator
SPM	scanning probe microscopy, scanning probe microscope

SPV	surface photovoltage
SRM	standard reference materials
SDD	silicon drift detectors
SSi	strained silicon
SSOI	strained silicon on insulator
SSRM	scanning spreading resistance microscopy
STEM	scanning transmission electron microscope/microscopy
STI	shallow trench isolation
TCAD	technology computer-aided design
TEM	transmission electron microscopy or transmission electron microscope
TEM/EDS	transmission electron microscopy energy-dispersive X ray spectroscopy
TERS	tip enhanced Raman scattering
TFET	tunnel field-effect transistor
TMU	total measurement uncertainty
TOF	time-of-flight
T-SAXS	transmission small angle X-ray scattering
TSOM	through-focus scanning optical microscopy
TSVs	through silicon vias
TTV	total thickness variation
TuT	tools under test
TXRF	total reflectance X-ray fluorescence, total reflection x-ray fluorescence
VGAA	vertical gate all around
VLSI	very large scale integration
VM	virtual metrology
VPD-ICPMS	vapor phase decomposition-inductively-coupled plasma mass spectrometry
W2W	wafer to wafer
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
XRF	X-ray fluorescence
XRR	X-ray reflectivity