



INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

INTERNATIONAL
ROADMAP
FOR
DEVICES AND SYSTEMS™

2020 EDITION

MORE THAN MOORE
WHITE PAPER

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MORE THAN MOORE

1. INTRODUCTION

Since its inception in 1998, the objective of the International Technology Roadmap for Semiconductors (ITRS) has been to identify the technical challenges that had to be addressed in order to ensure that microelectronics would be able to remain a driver for innovation in a wide range of applications. This has resulted in an industrial/academic agenda for pre-competitive research, which is continuously being updated to take into account new trends.

Over the years, the scope of the ITRS was enlarged to include not only the CMOS-based digital domain for memory and microprocessor devices (driven by miniaturization, as described by Moore's Law), but also heterogeneous integration of multi-functional analog and mixed-signal technologies for smart system applications (More than Moore). At the same time, the perspective of the roadmap shifted from being mostly technology driven to being increasingly determined by application requirements. In line with this, the ITRS changed into the International Roadmap for Devices and Systems (IRDS™).

The roadmapping effort has given rise to new insights in innovation methodology and strategy. This is in particular the case for More than Moore, which requires a highly multidisciplinary R&D environment. It has become clear that progress in highly complex technology fields can only be achieved by cooperation along the complete innovation chain, which implies that multiple fields of expertise can be combined for the development of generic technology modules, which can be made available on open technology platforms. This trend is clearly demonstrated in the present developments in, e.g., the automotive industry and the medical domain.

The objective of the present More than Moore white paper is to provide an overview of a number of technology/application areas that are representative for the More than Moore domain in the sense that they require multifunctional heterogeneous system solutions, rather than miniaturization of devices only. These are:

- Smart sensors,
- Smart energy,
- Energy harvesting and
- Wearable and flexible electronics.

The content of this chapter has been generated by the IRDS International Focus Team (IFT) on More than Moore, as listed in the acknowledgments section. Extensive use has been made of the NEREID NanoElectronics Roadmap for Europe.¹

1.1. HISTORY

The concept of “More than Moore” was introduced in the 2005 edition of the ITRS.² It followed from the observation that many functional requirements, such as power consumption, wireless communication, passive components, sensing and actuating, and biological functions did not scale with Moore's Law, as these would require non-CMOS-based technologies. It was anticipated that the integration of CMOS-based system on chip (SOC) and non-CMOS based system in package (SiP) technologies within a single package would become increasingly important. It was realized that “More Moore” and More than Moore” were not to be viewed as alternative technologies in competition with each other, but rather as complementary technology options that could be combined to create new high value systems. This was depicted in a diagram (Figure MtM-1) that has served as a “conversation piece” ever since.

A particular challenge that More than Moore posed to the roadmapping process was to be driven by application needs, rather than technology requirements. Consequently, a methodology had to be developed to guide the roadmapping effort

¹ NEREID NanoElectronics Roadmap for Europe (2018), <https://www.nereid-h2020.eu/roadmap>.

² International Technology Roadmap for Semiconductors 2005 Edition, Semiconductor Industry Association, Executive Summary.

2 Introduction

for More than Moore. This was the subject of a first More than Moore white paper that was published by the ITRS in 2010.³

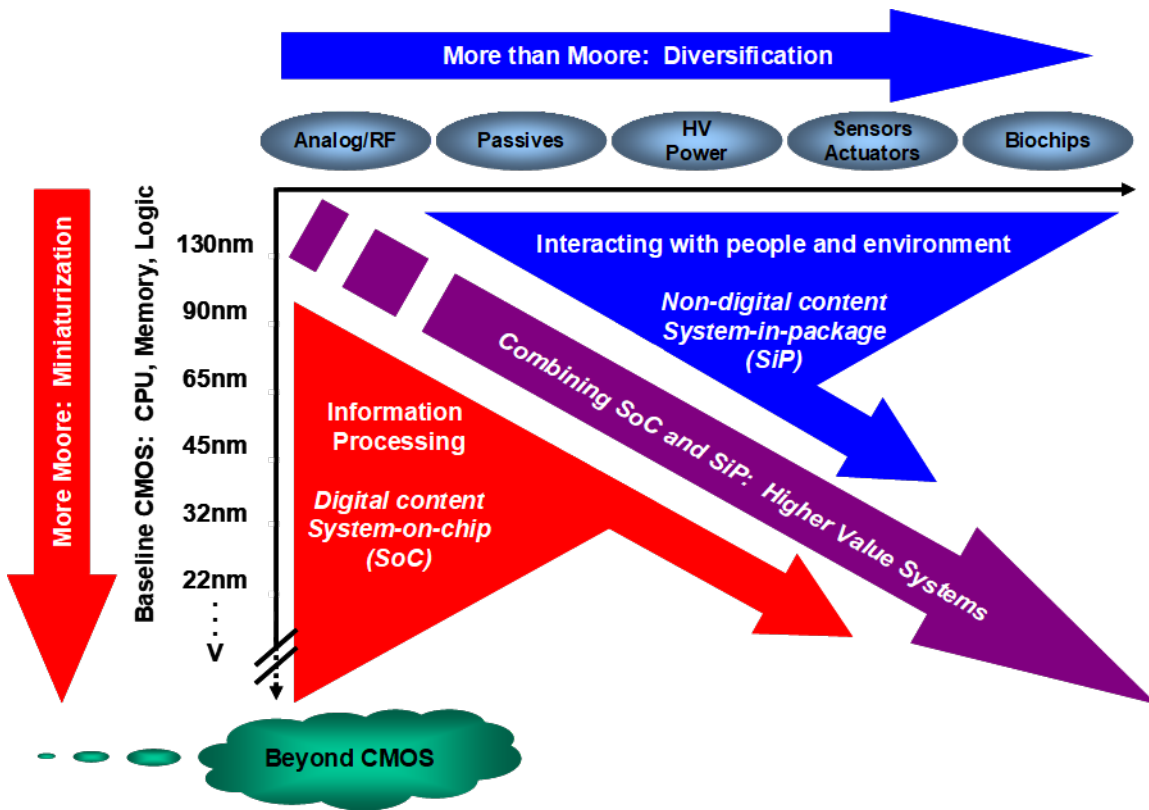


Figure MtM-1 Moore's Law and more

During the last decade, multifunctional devices and system-of-systems have become the building blocks and backbone of virtually every application field imaginable, from the internet of everything to artificial intelligence (AI). With it, the complexity of designing and creating (both in terms of hardware and software) these MtM-based building blocks has increased tremendously. Various strategic research agendas have been published with the objective to identify the societal needs and to guide the R&D programs of industries, institutes and universities.⁴

One of the major challenges for More than Moore today is the creation of technology platforms (both hardware and software) that will make available generic technologies that will serve as building blocks for the development of a wide range of applications. The objective of this document is to map the technology requirements in the areas of smart sensors, smart energy, energy harvesting and flexible/wearable electronics, and how these can be addressed by More than Moore-type solutions.

1.2. DEFINITION OF MORE THAN MOORE

The definitions given here are derived from the original More than Moore white paper (2010) and the ITRS (2009).

Moore's Law

An historical observation by Gordon Moore is that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) \times instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, Moore's Law has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 40 years.

³ W. Arden, M. Brillouët, P. Cogež, M. Graef, B. Huizing, R. Mahnkopf, "More-than-Moore" White Paper, SIA/ITRS (2010).

⁴ e.g., ECS Strategic Research Agenda 2020, AENEAS, <https://aeneas-office.org/strategy/documents/>.

More Moore: Scaling

“More Moore” refers to the continued shrinking of physical feature sizes of the *digital* functionalities (logic and memory storage) in order to improve *density* (cost per function reduction) and *performance* (speed, power).

Due to physical constraints that limit *geometrical scaling* if atomic dimensions are approached, the concept of *equivalent scaling* was introduced.

- *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling*, which occurs in conjunction with, and also enables, continued geometrical scaling, refers to 3-dimensional (3D) device structure (“design factor”) improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

“More than Moore”: Functional diversification

“More than Moore” refers to the incorporation into devices of functionalities that do not necessarily scale according to Moore's Law, but provide additional value in different ways. The More-than-Moore approach allows for the *non-digital* functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into the package (SiP) or onto the chip (SoC).

In addition, the increasingly intimate integration of complex embedded software into SoCs and SiPs means that software might also need to become a fabric under consideration that directly affects performance scaling. The objective of More-than-Moore is to extend the use of the silicon-based technology developed in the microelectronics industry to provide new, non-digital functionalities. It often leverages the scaling capabilities derived from the More Moore developments to incorporate digital and non-digital functionality into compact systems and, eventually, system-of-systems.

2. SMART SENSORS

2.1. INTRODUCTION

Global smart sensor technology is widely used in healthcare, automotive, environment, agriculture and energy applications. The technology-market developments⁵ moved from the Moore’s Law age from the 80s to 2010 to the More than Moore age from 2010 to 2030 and expected to move to a Beyond Moore age beyond 2030. The role of edge-of-the cloud devices and the generation of big data are expected to drive the creation of new ecosystems and include 11% of the world economy by 2030. The European smart sensor roadmap is broad, complex and diversified and leading to sustainable, ICT-enabled strategies. The smart sensor market is expected to grow from USD 18.58 Billion in 2015 to USD 57.77 Billion by 2022, at a compound annual growth rate (CAGR) of 18.1% between 2016 and 2022. In terms of unit shipments, the global smart sensor market is estimated to grow at a double-digit growth rate between 2016 and 2022. European countries are the main contributors to healthcare sector after the US and will lead the automotive in the coming 5-10 years. The nascent field of Smart AG-Tech (the digitization of the Agri-Food industry) is an accelerating emerging sector with a forecasted global CAGR of 16.2% up to 2023 with North America/Canada having the largest share of the market followed closely by the Europe. In all these sectors, the technology is moving from simple sensing to smart sensing with integration of multiple functions, cloud applications, self-powered systems and portable and/or disposable devices.

2.1.1. SMART SENSOR SYSTEMS

Around 29 billion connected devices are forecast by 2022, of which around 18 billion will be related to IoT. Smart system Deep-Tech and high levels of miniaturization and systems integration are the paradigms that are enabling the IoT. Connectivity is driving changes in many disciplines. Trends in smart sensor development will open the door to new offerings and business models, widening the value chain and increasing competitiveness and economic return. It is not the sensor “alone” but the result of the combination of sensors with IoT, AI and cloud-based solutions that will bear new opportunities. Smart sensor systems designed for smart mobility, autonomous driving, smart energy, medicine, and agriculture (amongst others) are becoming ubiquitous and interconnected and are key in driving the technological innovations of today. Large volume ultra-scalable manufacturing process, within the semiconductor industry, are essential to enable cost-effective devices required to increase market penetration and ultimately consumer take-up. The convergence between cyber-physical worlds will enable application specific stakeholder decision support tools and drive

⁵ *Sensors for Wearable Electronics & Mobile Healthcare 2015 Report by Yole Development*

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digitalization into new (non-traditional) sectors, thereby promoting increased societal benefits and sustainability. However, it is the application pull rather than technology push that will inform system design.

2.2. SCOPE

Targeting smart sensor system technologies with low fabrication cost, high efficiency and without toxic/rare materials is the main challenge. Adding flexibility and/or transparency is also an increasing demand for compatibility with wearables applications. Another challenge is the ability to develop systems that enable environmentally benign deployments in the environment.

For the semiconductor companies, the interest is also to develop new sensor devices compatible with silicon technologies. The diverse range of sensor applications and deployment conditions precludes a “one size fits all approach”. Low-cost native CMOS-based physical sensor interface platforms provide an attractive way to combine a subset of mutually compatible sensor functions (humidity/gas/VOC/etc.) with a microcontroller into a self-contained smart multi-sensor chip (e.g., an electronic nose). Other, more demanding sensor modalities require specific sensors, systems and packaging approaches. While very large markets exist for the automotive and Med-Tech sectors (in their widest sense), smaller emerging markets in sustainable Agri-Food and environmental applications may be of more interest to smaller OEM SME companies. The scope of this document is to provide an overview of mid to far horizon challenges that will need to be addressed in the coming years.

2.3. STAKEHOLDERS

At present the smart sensor user community of academic researchers and technologists struggle to develop industry-relevant solutions as there is a lack of focus on system-level assessment and optimization of their innovations. Similarly, there is a lack of cross-disciplinary interactions between stakeholders. New initiatives are required to address this and enable user communities to develop technology roadmaps, and promote workshops and networking events. The communities need to capture not just the developers and manufacturers of materials and devices but also the system integrators, users/stakeholders, social scientists, hardware, software and ICT protocol architects creating the ecosystem that needs these technologies. These need to be underpinned by technology offering such as those outlined in this document but introduced in a “solving the grand challenges” activity to address the sustainable development goals as set by the United Nations. This will enable the accelerated development of sustainable smart sensor solutions that are fit for purpose, specific to different deployment environments/scenarios, and are connected end-to-end. Increasing the stakeholder network, not only in terms of critical mass but also in diversity, particularly by including social scientists, will yield many new synergies, particularly in engraining the mindset of thinking about adoption at the very early conceptual stages in designing IoT systems. This will extend beyond electronics to ICT and MEMS, software, industrial design and data analytics spanning a broad variety of end applications such as Medtech, smart cities, Agri-tech, environmental monitoring and Industry 4.0.

2.4. TECHNOLOGY STATUS, REQUIREMENTS AND POTENTIAL SOLUTIONS

A key challenge in the development of smart sensor systems is that a “one size fits all” approach is not possible due to the myriad of different deployment scenarios ranging from controlled sterile environments (e.g., Medtech) to harsh and aggressive environments (e.g., Automotive, Agri-tech). Consequently, new or existing sensing paradigms must be developed or modified to render them fit-for-purpose to address their specific problem statements; bearing in mind that not all sensor types or approaches will be suitable for each deployment type.

Concept 1—Motion Sensors

The automotive market leads the development of MEMS devices. Motion sensors are widely used in automotive, consumer electronics, aerospace and defense, healthcare, and industrial applications. The motion sensor market is projected to be 2.6 billion by 2023. Similarly, accelerometer and gyroscope have become an integral part of all the consumer electronic devices and that market is expected to reach \$5 billion by 2022⁶. However, the growth of the motion sensor market is restrained by low accuracy and the average price of MEMS is limited to <\$1, which results in very low margins. The development on medical, automotive and industrial sensor is crucial now and shows the potential to lucrative opportunities.

⁶ *Accelerometer & Gyroscope Market (...) and Industry Vertical (Consumer Electronics, Automotive, Aerospace & Defence, Industrial, and Healthcare)-Global Opportunity Analysis and Industry Forecast, 2014-2022, (www.alliedmarketresearch.com)*

Concept 2—Pressure Sensors

The pressure sensor market is dominated by automotive and medical applications and will grow fast in the short term (3-5 years). The pressure sensors monitor and control the pressure of gases and liquids, and other pressures like vacuum, gauge and absolute. As a key component in automotive emission control sensor, the pressure sensors are helping to reduce emission and fuel consumption and the air pollution. Moreover, they play a crucial role in the passenger safety system. The smart phones and wearables consumer industry has shrinking margins and it is necessary to limit the cost of manufacturing and increase the efficiency of the process to limit market regression. Some measures could be shared costs, improved processes, or new devices with added value.

Concept 3—Advanced Drive Assistance Systems

Advanced Drive Assistance Systems (ADAS)—integrating image devices, radar sensors, laser and ultrasonic sensors— attract a keen interest from technology providers to help ensure road safety. The development of ADAS will be compliant to government regulations along with enhancing the user experience. Mounted image devices, including cameras, infrared detectors, and light detection and ranging (LiDAR), could offer a 180-degree view of path and night vision for drivers, and may be integrated to central monitoring systems to allow automated response. Image sensors are classified into charge-coupled device (CCD) and complementary metal-oxide semiconductor (CMOS), which could also be used in medical imaging for 3D scanning, 3D rendering, image reconstruction or 3D modeling gesture recognition. CCD will be fully replaced by CMOS in both the short and long term. Infrared detectors are used in defense systems, medical, and automotive applications such as night vision and pedestrian and/or animal detection. The current infrared detectors with affordable prices are based on the temperature variations of objects, which has an inaccuracy issue because of dusty environment and high humidity. LiDAR technology forms the environmental image by scanning the laser and computing the distance with the reflection. However, though the LiDAR is micro-size, low-cost and silicon based, and is suitable for all kinds of new applications including autonomous driving, the cost is still higher than other technologies such as radars due to the large number of components required. Furthermore, the image sensors can be connected to mobile applications and have the potential for the visualization of accurate test diagnosis. 3D imaging healthcare application is expected to dominate the global market share by 2022. The development of image sensors is growing fast and key technology almost updates every other year, and will help to miniaturize the devices with higher resolution mapping and more reasonable price. Long/mid-range radar sensors could help to prevent crashes by monitoring the environment around the vehicle (360 °sensing) and is less affected by weather and pollutions. The market is driven by development in the ADAS technology and the increasing awareness on safety and a comfort driving system. Apart from the technology and packaging, integration with electronic control unit and data management are also crucial and required by the market.

Concept 4—Environmental Sensors

Pollutants such as CO₂, NO_x and SO_x are mainly generated from vehicles, industries, and power plants diesel generators. On the other hand, the indoor/ outdoor air quality monitoring (PM10, NO₂, O₃, PM2.5, CO, SO₂) are crucial because of the influence on our health. Different platforms are widely investigated including metal oxide semiconductor (MOS), nanometal oxides, MEMS micro-hotplate MOS, polymer sensing, carbon materials, arrays of nano-capacitors⁷ for detection of micro-particles and others. The gas sensor market is dominated by the US, and followed by Europe, which is expected to grow over \$3 billion by 2027.⁸ The low-emission vehicles (hybrid or fully electrical) will reduce both pollution and the dependence on oil. Apart from the gas sensing, water quality monitoring using electrochemical sensors is developing fast as well. Investigation on novel materials, high-integration sensors and software development are leading the environmental sensing to an easy-operation and portable system.

Concept 5—Agri-food Sensors

Reducing the extent of future climate change by limiting the amount of greenhouse gases (GHG) being emitted and increasing the rate of carbon dioxide removal from the atmosphere is a significant global challenge. With the global population expected to reach ~10Bn by 2050 a key challenge is to produce food sustainably with increasing limited resources. Under the United Nations Framework Convention on Climate Change⁹, developed countries are expected to play a leading role in achieving major reductions in GHG emissions. The forestry, agriculture, and other land use sector is responsible for 24% of global CO₂ emission, thus to reduce impacts on climate change it is obvious there is a requirement

⁷ C. Laborde et al., *Real-time imaging of microparticles and living cells with CMOS nanocapacitor arrays*, *Nature Nanotechnology* v. 10, p. 791, 2015

⁸ *Environmental gas sensors 2017-2027*, idTechEx, (<http://idtechex.com/research/reports/environmental-gas-sensors-2017-2020-000-500.asp>)

⁹ https://en.wikipedia.org/wiki/United_Nations_Framework_Convention_on_Climate_Change

6 Smart Sensors

to develop robust and achievable mitigation strategies that can lower emissions within this sector. This will require investment in new digital technologies as smart monitoring strategies to ensure that production systems deliver sustainability while maximizing economic, societal and environmental benefits from this sector.

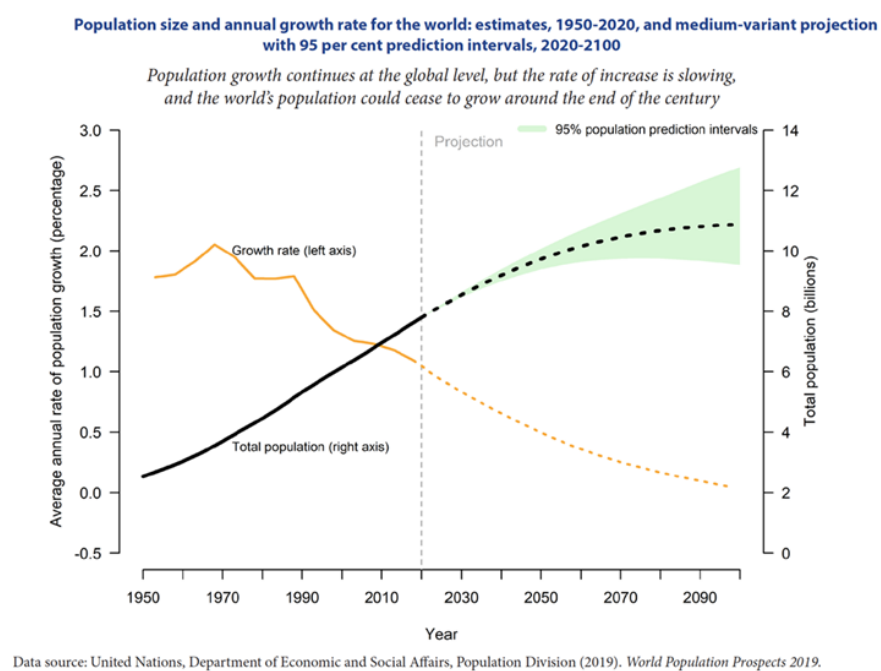


Figure MtM-2 Predicted global population growth.

Source—United Nations

For the past twenty years, the Agri-food industry has been transforming from a supply driven market approach to one driven by the consumer. Global trends and policy changes along with concerns over food safety, security, supply chain management, and energy requirements are leading market demands for competitively priced food products, produced at the desired quality and in a safe and sustainable manner. This challenge is set against the backdrop of climate change, scarce natural resources, adverse weather events, geopolitical instability and other societal demands for land including housing, transport infrastructure and recreation. Global demand for food, particularly protein, is increasing as urbanization and expansion of middle classes in developing countries (particular Asia and India) are driving growth in global demand. The abolition of the quota system is providing the catalyst for the expansion of supply and product development for the dairy industry in particular. Concurrently, societal expectations such as conservation of scarce natural resources, improved water and air quality along with retaining biodiversity must also be achieved simultaneously.

It is recognized that a significant increase in food production cannot be considered in isolation from its environmental impact, in particular regarding concerns associated with the depletion of natural resources and the potential impact on climate change. To address this, future food production systems must be focused on managing and sustaining our natural resources as they are on increasing production. Consequently, there is now a pressing need for the development of new advanced technologies based on emerging new materials and processes that will increase productivity while also permitting more efficient use of natural resources and minimizing waste within the production systems.

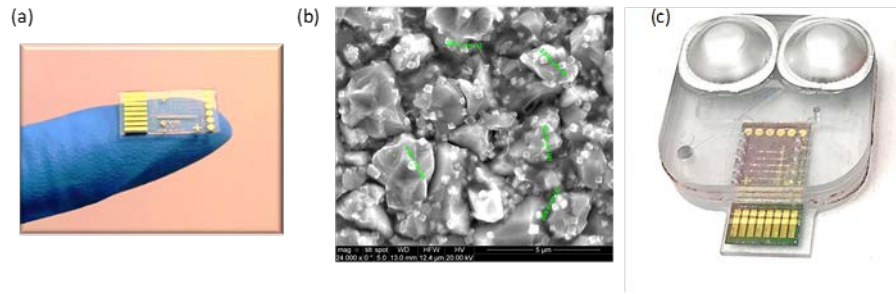


Figure MtM-3 Advanced nanosensor modified with nano-copper designed for monitoring of agricultural nitrate run off

The continued growth of the Agri-food sector must be based on sustainable intensification, a concept included in the conclusions of the October 2014 EU Council on the 2030 EU Climate and Energy Policy Framework.¹⁰ Producers must play a positive role in the protection of landscapes, waterway biodiversity and water quality while also increasing production. This will require that the investment in monitoring systems and science-based research programs must be undertaken to develop cutting-edge technologies that address current limitations in the production system. A key challenge with the current system is the difficulty of transforming scientific research into commercial returns. Improved knowledge transfer to all actors along the supply chain is required and the involvement of private enterprise with the required capacity to absorb new research and innovation will be critical to translate research outcomes and enable the rollout and uptake of new commercial technological products and processes.

As the demand for dairy, meat and fish protein products is forecast to increase substantially throughout the next decade as the emerging middle classes in developing countries seek to raise their dietary protein to starch ratio. This demand places tremendous stresses on the Agri-food industry to produce more food with increasing constraints on limited natural resources. This is cast against the significant global challenge that the industry greatly needs to reduce ammonia greenhouse emissions to reduce its impact on future climate change. It is clear that future viability and profitability at producer level will require adoption and application of new technologies and processes. Further benefits can be accrued such as mitigation against supply chain disruption arising from emerging disease or food safety risks and arresting biodiversity losses by continuing the improvement of water quality. Development of new technologies that reduce waste are vital in this regard and represent a robust mitigation strategy that can both reduce emissions and help to deliver a lower carbon future.

Concept 6—Sensors for Medical and Healthcare Applications

In the medical field, the main applications of sensors are the remote patient monitoring (not only disease monitoring, but also drug development and clinical operation), home healthcare and fitness/wellness monitoring. Depending on the application, the end users can be the healthcare providers and players (doctors, hospital personnel, pharmaceutical companies) but also patients themselves. The three main categories of the medical sensing devices are (i) wearable physiological signal monitoring devices, (ii) implantable sensors and (iii) sensors for molecular diagnosis. The technological solutions, requirements and challenges are strongly dependent on the application and on the category of the sensor. However, some common elements include safety/security requirements, miniaturization potential, manufacturability and cost, reliability and packaging, biocompatibility and bio-stability, multi-sensing capabilities.

The next sections describe the 3 categories cited previously with more specific details.

¹⁰ <https://www.consilium.europa.eu/en/policies/climate-change/2030-climate-and-energy-framework/>

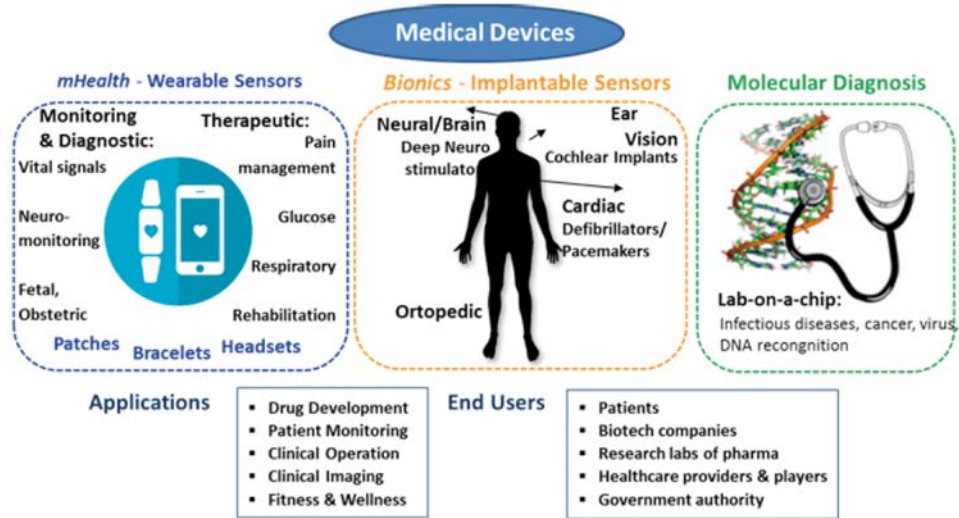


Figure MtM-4 Breakdown of medical devices by application and genera

Physiological Signal Monitoring

Wearable medical devices are widely applied to attach the human body from head to toe (glasses, bands or watches, hats, shoes or neck wear) to monitor changes in body signatures of various area and organs like oxygen, glucose, insulin level, heart diseases, blood pressure, brain activity, hydration, temperature, quantity and quality of sleep, calorie intake, etc. Software such as mobile based applications, data transmission, and/or alerting mechanism are integrated to the wearable medical devices and lead to more user-friendly scenarios. Physiological signals monitoring could help to enhance the healthy life-style, prevent cardiovascular accidents and improve the management of chronic/acute diseases. Moreover, physiological sensors are able to detect the pollution related health hazards and fill the gap of home monitoring and diagnostics. These technological solutions used involve temperature, pressure, ion and/or biomarkers sensors. Some specific challenges for the physiological signal monitoring concern detection with a good signal quality, free or artefacts, having high-autonomy and low-power designs, allowing personalized algorithms and real-time feedbacks; being non-invasive and allowing multiple parameters monitoring. The development of medical devices is very difficult because of the long-term development, high cost of clinical validations and difficult CE labelling / FDA approval process. Thereby, the period are in the range of 10 to 15 years and unaffordable for standards SMEs and spinoff companies. In addition, the security and privacy of patients are respected and prevention of hacking is crucial.

Implantable Sensors

Bionics, biomedical implants, are artificial addition to the body, which would mimic the function (vision, ear, orthopedic, cardiac, neural/brain) of the lost or non-functional natural organ. However, the high cost, corresponding medical treatment, and stringent approval processes are challenging and limit the market growth. Besides the challenges in terms of biocompatibility, bio stability, extremely high reliability, a key element for the implantable bio-sensors is the lifetime of the implants and their autonomy (energy harvesting systems, remote/wireless power transmission, wireless data communication and device control).

Realizing an all-electrical device for electrophysiology, a closely packed microelectrode array (MEA) capable of high-precision intracellular recording from a large network of cells has long been a major pursuit in bioengineering, neuro- and cardio-technology. Ionic currents across membranes are crucial in both excitable and non-excitable cells; their accurate measurement requires efficient coupling between cell membrane and measuring electrodes. A most ambitious goal pursued to date is to realize all-electrical electrophysiological imaging by CMOS-MEA, which should allow massively parallel recording of cellular networks. The combination of this technique with large-scale integration typical of microelectronics has not been attempted yet, due to the difficulty to combine the usual CMOS technology with the nanotechnology needed to grow small-sized nano-electrodes. Emerging nanomaterials such as the growth of silicon nanowires (SiNWs) directly on the surface of pre-existing devices, can greatly increase large arrays of extremely resolute pixels. Such integrated electrophysiology sensors, for example, has huge applications as patient based devices, such as the following examples: in vivo monitoring of cardiac fibrillation, neurons activity, and retina vision.

Concept 7—Molecular Diagnostics

Molecular diagnostics is the technique to analyze biological markers at the molecular level by detecting specific sequences in DNA or RNA. It also can diagnose various infectious diseases, cancer and check the risk of genetic predisposition for a disease, which will potentially reduce the cost, and simplify the diagnostic procedure. However, only simplest biological parameters such as C-reactive protein and procalcitonin could be detected, central laboratory analysis still required for complex and life-threatening infectious diseases. Electrochemical sensors also play an important role in molecular diagnostics. In order to detect different target, the sensors are coated by different functional groups such as antibody or DNA, and could be easily integrated with a portable device and would be suitable for wider usage scenario like on-field diagnostics. The continuous advancement of CMOS technology allows the fabrication of sensor arrays as for example the large matrixes of ion-sensitive-FET used for DNA sequencing (“ion-torrent” concept¹¹).

The smart sensors are developing fast in the recent decade and will be integrated with other technique compactly. Internet of things is not only a network of smart devices, but also including data collecting, data analyzing, system integration, software development and services. Moreover, energy supporting of the sensor, packaging, and eco-system design are challenging for developers and manufacturers. Some sensors like motion sensors, pressure sensors, are mature which may result to product into market in 3 years, while some others such as quantum air monitor sensor and rapid complex disease diagnostics are under functional investigation, and may take decades. Modeling plays and will play a key role in the smart sensor development as it does for CMOS technology. This requires a shift from TCAD tools solving the semiconductor equations toward multi-physics approaches describing light absorption, electro-mechanical interactions, electro-chemical processes, molecular binding just to name a few. These tools will help interpreting experimental results and give guideline to optimize the resolution, selectivity and time response of the sensors. Beside these “device-level” models above, compact models are needed when designing the electronic read-out. Due to the large variety of sensors, description languages as Verilog-A can be used to develop compact models for circuit simulation which can be updated and refined on short time scales. Significant effort should be devoted to the modeling of the AC and noise behavior.

MicroRNAs are evolutionarily conserved non-coding RNA in size of 20-22 nucleotides, synthesized through processing by both nuclear and cytosolic proteins and are important down regulators of gene expression via MicroRNAs cleavage or translational repression. The presence of microRNA in blood and the ability to measure their levels in a non-invasive way has opened new doors in the search for peripheral biomarkers for the diagnosis and prognosis of diseases such as brain ischemia. Since the recommended therapeutic window is very limited, biomarkers in particular for stroke have the potential to expedite diagnosis and institution of treatment. Moreover, in the last decade it has been evidenced that expression levels of MicroRNAs in blood are reproducible and indicative of several diseases. The backend of CMOS integrated circuits is covered by a top layer of silicon dioxide. This makes the surface particularly suitable for functionalization with biomolecules, including Peptide Nucleic Acids which can recognize the particular sequence of miRNA and fix to the surface fluorophore molecule. To this aim can be re-used silicon-based Optical Sensors are already key components for medical applications, specifically for diagnosis.

¹¹ B. Merriman, et al, “Progress in Ion Torrent semiconductor chip based sequencing,” *Electrophoresis*, vol. 33,no. 23, p. 3397, 2012.

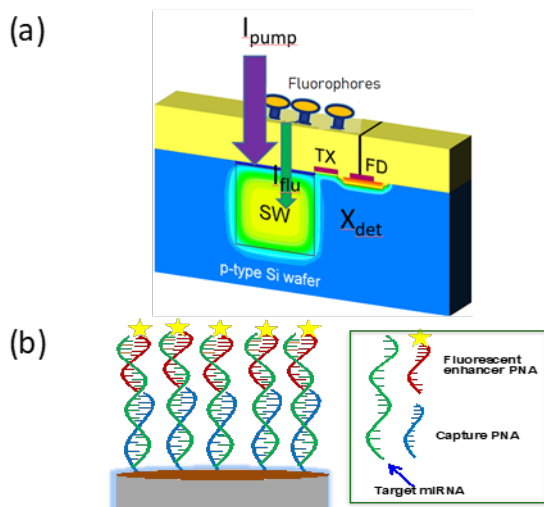


Figure MtM-5 A. Sketch of the filtering structure in a pinned photo diode. B. Schematic of the PNA-miRNA sandwich array used to detect the target miRNAs.

*Note—The violet curve in Figure MtM-5A depicts the absorption of the radiation of the short wavelength pump, while green curve indicates the photo-emitted radiation, which can reach the SW collection region.

Concept 8—Native CMOS-based physical sensor interfaces

A CMOS-pixelated capacitive sensor platform consists of a dense 2-D array of individually addressable micro-/nanocapacitor sense electrodes at the surface of a CMOS chip. The electrodes are connected to selection and read-out electronics underneath the electrode array, which allows making arrays with ten thousand or more electrodes. In addition, the chip might contain temperature sensors, and ADC, DSP, control and I/O electronics. Such an array sensor can be operated like a capacitive camera (no optical components like light sources, lenses, etc., are needed). The sense electrodes can be either exposed or covered by an insulating protection layer (e.g., the chip's scratch protection layer). Exposed electrodes can be made of gold or a gold-rich gold-copper alloy, to prevent them from corroding, or to form an surface for immobilizing e.g., biomolecules. Covered microelectrodes can be made of standard top-metal aluminum.

The platform serves as a generic massively parallel capacitive sensor interface that can be turned into a variety of physical and/or chemical multi-sensors by ink-jetting “sensing inks” on the array, with dielectric properties that change when exposed to humidity, gases, volatile organic compounds (VOCs), air pressure variations, infrared light, etc. Alternatively, mobile masses can be suspended above the array (within the reach of electric field lines emerging from the sense electrodes). When exposed to motion, the capacitive camera can measure linear translation, rotation and tilt of the masses, turning the chip into a 6-axis motion sensor. In principle, gas and motion sensing can be combined on the same array, turning the chip into a very versatile smart multi-sensor system, e.g., for edge-IoT applications. Gold or gold-copper electrodes can be functionalized with antibody, nanobody, aptamer or single-stranded DNA or PNA capture probes. This way, the platform chip can be turned into a variety of biosensors. Without functionalization, the capacitive camera can be used for spectroscopic detection of a variety of micro- or nanoparticles, e.g., living cells, viruses, etc.

Table MtM-1 Smart Sensors Difficult Challenges

Difficult Challenges 2019-2025	Summary of Issues
<i>MEMS (highest accuracy, stability, power consumption and miniaturization)</i>	3-axis accelerometers 3-axis gyroscopes IMU/iNEMO SiP inertial modules (accelerometer, gyroscope, magnetometer) Low accuracy
<i>Pressure sensors (automotive and medical applications)</i>	Medical applications (e.g., blood pressure, bladder examination) Pressure monitoring system (barometric air pressure)
<i>Advanced Drive Assistance Systems (image sensors, LiDAR, infrared sensors, and radar sensors)</i>	Improve sensitivity, with smaller pixel size ; flicker-free and HDR n-cabin near-IR global shutter; 3D cameras Improve resolution Long, short/medium range radar; silicon, silicon germanium
<i>Patient-based devices; hospital-based devices</i>	Blood glucose meter, cardio meter; activity monitor-actimetry Blood pressure meters monitor
<i>Implantable sensors</i>	Vision, ear, orthopedic, cardiac, neural/brain Critical to the final sensor performance Difficult, expensive and time consuming validation tests and certifications. A few centimeters implant depth The basic technology of low-temperature silicon nanowires growth on CMOS, to be used in many different electrophysiology meters directly at cellular level.
<i>Molecular diagnostics</i>	Infectious disease, cancer, other disorders medical diagnostics Functionalization of CMOS IC, optimization of image sensors as fluorescence detectors
Difficult Challenges 2025-2034	Summary of Issues
<i>MEMS (highest accuracy, stability, power consumption and miniaturization)</i>	IMU/iNEMO SiP inertial modules (accelerometer, gyroscope, magnetometer) High reliability and quality, low price, and ultra-low power consumption for portable application and implantable devices
<i>Pressure sensors (automotive and medical applications)</i>	Automotive application (pressure monitoring system—tire pressure monitor, air bag development) Tactile sensors for fall detection Packaging
<i>Advanced Drive Assistance Systems (image sensors, LiDAR, Infrared sensors, and radar sensors)</i>	New sensing layer to replace silicon; local computer vision; global shutter/ flicker-free/ HDR; secured data links; 3D cameras; photodetectors Reduce cost; data fusion with CMOS imaging sensor; microbolometers Higher integration into a small module, laser scanner, Long, short/ medium range radar; silicon, silicon germanium
<i>Environmental sensors</i>	Gas sensors (CO, SO ₂ , NO ₂ , O ₃) market introduction Particulate matter detection (PM2.5, PM10) market introduction Toxic, explosive, fire, or injurious gases (industrial, infrastructure), market introduction Polymer and carbon based sensing—R&D Quantum dots, nanotubes and nanowires—R&D Moisture absorbing material—humidity monitoring
<i>Agri-food sensors</i>	Gas sensors, (CO ₂ NH ₄ , N ₂ O, CO, CH ₄) market introduction Multiplexed water sensors (NO ₃ , NO ₂ , Do, pH, PO ₄ , K) market introduction Multiplexed soil nutrient sensor (C, N, P, K, pH, H ₂ O) market introduction Animal health DNA probe/target recognition, label free immunoassays, Molecular diagnostics Plan health DNA probe/target recognition, label free immunoassays, Molecular diagnostics Soil health, low cost sequencing for soil microbiome
<i>Patient-based devices; hospital-based devices; driver impairment monitoring</i>	Cardio meter, BP monitor, EEG monitoring for epilepsy for children, fitness monitor, energy expenditure monitor, stress monitor Vital signal monitoring, apnea and sleep monitor, pulse oximetry, congestive heart failure Drowsiness mitigation systems; driver inattention
<i>Implantable sensors</i>	Ear, orthopedic, neural/brain Packaging solutions, power solutions for >10 cm implantation depth available
<i>Molecular diagnostics</i>	Lab-on-chip DNA probe/target recognition Single particle or virus detection Biological markers analyzer m-RNA in blood

2.5. RECOMMENDATIONS

Key challenges remain to develop smart sensor systems that are fit-for-purpose for final deployments. To this end, sensor development, integration and packaging need to be driven by user-specified problem statements. Concerning the challenges outlined in Table MtM-1, improvement in different sensing approaches in terms of sensitivity, selectivity, repeatability, robustness, precision and accuracy are key requirements. Edge analytics and AI at the edge will be key, not only to reduce power consumption, but essential to achieve these requirements. Successful translation of emerging research devices and systems from the lab to real world deployments, i.e., increase the technology readiness levels will require investment in new and appropriate infrastructural test-beds and development of an early adopters/social scientist ecosystem. Test beds will permit innovation testing for verification and proof-of-concept studies outside of the laboratory to enable evaluation of the technology from institutional, stakeholder and learner perspectives. Customer adoption patterns are important to understanding how to market and position new product for adoption. Engaging with a social scientists/early adopter ecosystem, iteratively with the validation phase, will provide a clear understanding of what each type of adopter values leading to better business outcomes, including revenue growth and greater profit margins.

Concerning the challenges covered in this white paper, the use of nanotechnologies is foreseen to increase the performance of all the concepts in general. Flexible and low-cost approaches should be developed, where appropriate, and environmentally benign deployment paradigms such as “Deploy and Forget” or “Deploy and Dissolve” should be explored. Adoption of innovative power management circuits, energy storage and generation, will enhance the efficiency of deployments. While it is accepted that a “one size fits all” approach is not possible sensor fusion, judicious selection of materials coupled with the most suitable sensing modality and transductions mechanisms coupled with edge analytics will provide a route for future sensing challenges to be successfully addressed. Finally, investigation into disruptive sensing approaches and technologies, such as quantum sensors, must be undertaken to provide solutions to heretofore unanswered challenges/problem statements.

2.6. SUMMARY

Integrating new and existing sensor to electronic devices, communication and edge data analytics will be a key factor in enhancing deep technologies required for smart sensor networks and IoTs. Various different sensors transducers mechanisms are available that can be exploited, further developed and fused to provide orthogonal and robust sensing approaches that are required for the many diverse application areas described in this white paper. It is expected that research in non-CMOS nanotechnologies and emerging material science will drive increased functionality and increased specificity/sensitivity and robustness. The evolution of the materials, processing and disruptive technologies will enable a growing number of possible applications and products to be placed on the market, which were unfeasible up to now.

3. SMART ENERGY

3.1. INTRODUCTION

Smart energy devices have to incorporate the technological capabilities needed for generating, distributing and consuming electrical energy. Also, they enable replacing other energy sources like mechanical, hydraulic or combustion engines with electrical power. This section focuses on the definition of the roadmap for technologies, materials, integration methodologies and processes for the realization of more efficient power management devices. Roadmaps for smart power need to cover different sectors, as follows:

- New highly efficient power devices based on wide band-gap semiconductor materials, like GaN on silicon and later diamond on silicon or nanowire-based materials
- Integrated and smart power GaN device and system solutions
- New cost-efficient, Si based power devices to enable high efficiencies for mass-market applications
- Power management for very high voltage applications making use of new wide bandgap materials, is required for the main power supply in order to minimize or avoid fluctuations on the power line caused by e.g., solar panels and wind mills. In addition, developments such as artificial intelligence (AI) and battery management are important in this respect.
- Power management for very low-power applications, as required for IoT, including the development of power scavenging technology

- High-temperature capable packages employing new materials and 3D technologies with lifetimes fulfilling highest requirements and the integration capabilities

Power electronics is the technology associated with the efficient conversion, control and conditioning of electric energy from the source to the load. It is the enabling technology for the generation, distribution and efficient use of electrical energy. It is a cross-functional technology covering the very high gigawatt (GW) power (e.g., in energy transmission lines) down to the very low milliwatt (mW) power needed to operate a mobile phone.

Many market segments—such as domestic and office appliances, computer and communication, ventilation, air conditioning and lighting, factory automation and drives, traction, automotive and renewable energy—can potentially benefit from the application of power electronics technology. The ambitious goals of the European Union to reduce the energy consumption and CO₂ emissions can only be achieved by an extensive application and use of power electronics.

3.2. SCOPE

The Smart Energy devices roadmap will present the medium- and long-term targets for the two main wide bandgap semiconductors (WBS) SiC and GaN, as well as for the new promising WBS of Ga₂O₃, AlN, diamond. The aspects that will be covered within this roadmap are as follows: i) materials and processing issues (including device architectures), ii) applications, iii) technology and design challenges; and iv) figures of merit (FoM). In addition, important aspects of the roadmaps of corresponding silicon technologies will be presented.

3.3. TECHNOLOGY STATUS, REQUIREMENTS AND POTENTIAL SOLUTIONS

3.3.1. SILICON-BASED POWER DEVICES

Super-junction (SJ) devices

Silicon-based power devices are relatively advanced from the semiconductor technology point of view. The material, reliability, and properties of Si/SiO₂ are extensively researched and well understood. Moreover, production capacities of 12" wafer diameter are already in place or are planned by various companies. Altogether, this maturity combined with the low area-specific resistance unit cost of super-junction (SJ) technology enables the power-conversion market dominance of these devices in various application segments. The main figure of merit to improve is $R_{on} \times A \times \text{cost}$. This in turn can be optimized by further reducing the pitch of the SJ structure to achieve $R_{on} \times A$ values even below 5 Ωcm^2 (currently 10 Ωcm^2 is available on the market). Here, the main research paths are:

- 1) Exploring the limits of trench-based and multi-epi/multi-implant (ME/MI) based SJ technologies
- 2) Evaluation of alternative structuring concepts to trench or ME/MI
- 3) Reduction of the switching losses to close the performance gap between wide bandgap (WBG) and super-junction-based devices

It has to be noted that further die size shrinks (for a given R_{ON} value) pose similar challenges and have the same relevance as for GaN and WBG devices regarding novel packaging concepts, thermal management, and understanding electrical parasitics, etc.

Currently, in the voltage range of 500-1000 V SJ-based devices dominate the power conversion market. Devices are used in both, hard- and soft-switching topologies for various applications and market segments like adapters, PC power, server/telecom, lighting, solar, EV-charging, eMobility, etc. There are several well-known manufacturers competing in these market segments.

These major manufacturers are Infineon, STMicroelectronics, Vishay, ON semiconductor, Toshiba, Fuji and others. China is catching up with a multitude of smaller companies supported by government and funding programs. Moreover, Chinese foundry HHGrace offers a power discrete fabrication services for the voltages 400-700 V.

Field Plate Trench Power MOSFETs

In the voltage range from 15 V to 300 V Si Power MOSFETs were used since more than 40 years. The concept changed from vertical DMOS with planar gate to a vertical gate structure more than 20 years ago. Roughly 20 years ago the field plate trench technology was introduced with improved $R_{on} \times A$ for a given breakdown voltage. Here an additional electrode on source potential below the gate trench is integrated that is insulated by a thick field oxide layer. This field plate allows higher epi doping since it compensates charges from the drift region. Meanwhile a large number of manufacturers are using this concept—Infineon, ON semiconductor, STMicroelectronics, Vishay, Toshiba, Renesas, Nexperia, AOS, Hunteck, TI and others.

The $R_{on} \times A$ of this concept is continuously improved by a systematic shrink path of the cell pitch and the reduction of the silicon substrate thickness, which has a strong contribution to the $R_{on} \times A$ especially for the lower voltage classes. For both measures (pitch, substrate thickness) development activities are still ongoing and planned for the future. The smallest available pitch for a 25 V field plate trench MOSFET is 650 nm and the thinnest substrate is currently 40 μm .

Besides $R_{on} \times A$ improvement, a reduction of different figure of merits (FoMs) is beneficial. Typical application of the 25 V class is computing DCDC. For higher voltage classes (e.g., 100 V) typical applications are switch mode power supply, telecom, low-voltage drives, battery management and many more. The main driving forces are power density, efficiency, ease of use and cost and therefore different FoMs are important— $FoM_g = R_{on} \times Q_g$, $FoM_{gd} = R_{on} \times Q_{gd}$, $FoM_{oss} = R_{on} \times Q_{oss}$, $FoM_{qrr} = R_{on} \times Q_{rr}$

The Q_g and Q_{gd} reduction goes hand in hand with channel length reduction, which basically is enabled by better process controls, e.g., by CMP processes and high precision recess etches. Q_{oss} improvements can be achieved by better control of epi doping and trench depth. Q_{rr} can be improved by optimized cell design or lifetime killing techniques.

Besides transistor cell optimization, the trend of feature integration like current senses or integrated gate resistors is clearly visible. Also, system solutions with driver IC, high-side and low-side chip is getting traction. In parallel, new packages have been developed with lower electrical series resistance, lower inductances and better thermal connection.

Insulated Gate Bipolar Transistor (IGBT)

Further development steps on Si-based IGBT technology are possible and crucial for future business success in the respective markets, although this technology is mature and approaching their limits. The remaining improvement potential of Si-IGBT technology can be separated in four main categories, as follows:

1) *Advanced Transistor Cell Design*—The basic principle behind the design of advanced IGBT cell structures is to enhance the amount of charge carriers (holes and electrons) in the upper region of the device during the on state resulting in a low static on state voltage. This can be achieved by introducing sophisticated sub- μm mesa structures in between adjacent deep trenches. The challenge is to approach the theoretical limit of IGBT on state performance without jeopardizing switching behavior and dynamic losses. Development activities in this direction are currently running and will be driven in the future by leading IGBT suppliers. A further reduction of the on-state losses of about 1 V for a 1200 V device may become feasible. Furthermore, in combination with advanced gate driving schemes the trade-off between required short circuit capability and low forward voltage drop (low channel resistance) could be improved. This can be realized by current sensing and fast short circuit detection in intelligent power modules (IPMs) which is not yet a standard in the broad market of drive applications.

2) *Vertical Design*—In order to reduce static and dynamic losses a further reduction of device thickness is essential. The theoretical limits for silicon are not yet reached. For example, for a 1200 V device 110 μm to 115 μm are common and state of the art for high-performance IGBTs whereas 80 μm to 90 μm are enough for the voltage blocking. Today's restrictions for further thickness reduction are given by critical application requirements like switching softness, cosmic ray robustness and thermal short circuit capability, where other specific measures will help to overcome these limitations (e.g., low inductance modules, field stop/p-emitter optimization, increased Z_{th}).

3) *Reverse Conducting IGBTs*—The possibility of monolithic integration of IGBT and a freewheeling diode (FWD) in one device is demonstrated by several IGBT manufacturers. The so-called reverse conducting IGBT concept (RC-IGBT) enables a more efficient use of the given footprint in a power module and is therefore contributing to power density gain and cost reduction. The challenge is mainly to integrate very differently optimized features technologically (lifetime killing of diode, high p dose in IGBT cell) within one single die. Further device performance optimization is visible and full benefit of the concept is achievable by implementation of sophisticated gate driver concepts.

4) *Increased Power Density*—The fundamental development path of increasing power density is still valid and intact for IGBT technology. Further steps in Si-IGBT technology are visible and essential for future business success. Increasing power density is leading to higher operation temperature (T_{jop}) and higher T_{jmax} of the device due to visible limitations in loss reduction. As a consequence, improvement measures for chip interconnect and chip packages are essential to prepare the path to increased device operation temperature. In addition to measures of lowering R_{th} and improving thermal stability of package materials, a key roadmap target is therefore the improvement of power cycling capability in order to regain the desired product reliability. This leads to the necessity of the development of new chip metallization and interconnect schemes of highest power cycling capability. First development steps are done in the premium high-power segment like Infineon's XT technology with back side Ag sintering and power-Cu front side metallization or double-side

cooling/sintering assembly techniques for electric drive train application. Next steps have to follow to improve cost effectiveness and roll out to the general-purpose drive segment.

Smart Power BCD Technology Platform

Thanks to the availability of a wide variety of elementary devices (bipolar, CMOS, lateral DMOS, power and passive) that enable electronic functionalities, bipolar-CMOS-DMOS (BCD) products are present in almost all the current applications. During the last 30 years, the BCD platform evolution has followed with some delay the standard CMOS evolution. Clearly the very different applications covered by this flexible platform has been addressed with specific customization requiring dedicated device features for high voltage applications (600 V and above) or specific isolation capabilities addressed by fully dielectric isolated device built on silicon-on-insulator (SOI) substrates.

As for all the technologies in the More than Moore arena, the evolution of this platform is driven by the application requirements and evolution, as follows:

- *Digital Processing Capability increase*—System miniaturization for mobile applications together with some emerging applications in the automotive segment are pushing the migration to more dense technology nodes, enabling the possibility to integrate in the IC a larger amount of logic together with an meaningful amount of non-volatile memory for code and data storage. The integration cost must be carefully evaluated and it may be alleviated thanks to the availability novel memory solution and larger diameter wafer.
- *Power and High Voltage evolution*—The continuous need of increased electronic system power efficiency is requiring the integration of high-performance power devices in the BCD platform. Despite the lower level of power managed by a power IC (due to package thermal limitations) the key power device target performance level requirements are not far from power discrete both in terms of conduction loss ($R_{on} \times Area$) and in terms of switching loss ($R_{on} \times Qg$). Industrial applications (Industry 4.0) and automotive electrification are requiring higher voltage devices drivers (1200 V) and high voltage galvanic isolation capability that will require specific process solutions in mature BCD technology platforms.
- *Power Customization by Application*—Specific technology modules are often key differentiator factors enabling optimum solution for specific applications. Power metal metallization is for example very important to manage in an optimum way the interaction between the silicon die and the assembly in the specific package family.

Within this scenario it is very difficult to identify a single parameter or set of parameters for the description of the BCD technology evolution in the coming decade. Clearly the logic density capability, power device performance together with the demand for some new high-voltage device rating will be three key drivers for the evolution together with the function cost decrease.

Focusing on the high-voltage device performance, the 40 V rated power device is a key component in all BCD platforms addressing industrial and automotive markets. Key performance parameter ($R_{on} \times Area$) evolution is one of most important parameters for the STM BCD platform. Keeping a 20% reduction of that is a target for the new coming generation. The reduction rate, however, has decreased due to the difficulty of drift region scaling.

The roadmap of $R_{on} \times Area$ of the Power Lateral DMOS (LDMOS) for the BCD platform is the following:

Year of Production	2020	2025	2030	2035
40 V Rated Integrated Power LDMOS $R_{on} \times A$ ($m\Omega \cdot mm^2$) $BV_{off} > 50$ V	25	21	19	17

The vertical power MOS (VMOS) has a potential to keep 20% reduction by the optimization of device parameters and structure. The roadmap is the following:

Year of Production	2020	2025	2030	2035
40 V Rated Integrated Power Vertical POWER MOS $R_{on} \times A$ ($m\Omega \cdot mm^2$) $BV_{off} > 50$ V	7.0	5.6	4.5	3.5

3.3.2. GAN-DEVICES AND SUBSTRATES

GaN semiconductor devices provide competitive system advantage in terms of thermal performance, efficiency, weight and size. GaN is anticipated to be the next generation power semiconductor and thus different countries are indulged in developing widespread applications of GaN semiconductors. The wide bandgap semiconductor technology has matured rapidly over several years. In fact, gallium nitride high electron mobility transistors (GaN HEMTs) have been available as commercial off-the-shelf devices since 2005. Well-known GaN device manufacturers are Infineon, Panasonic, NXP, ON Semiconductor, STMicroelectronics, EPC, Texas Instruments, Transphorm, Navitas, GaNSystems, Nexperia, TSMC, Sumitomo, Exagan, Innoscience, and Power Integrations.

Substrate Diameter—Today, 6” to 8” wafer size, low vertical leakage current, current collapse free GaN-on-Si wafers are available on the open market. This remarkable achievement is a result of concentrated epi efforts during the past years that led to an ever-increasing understanding of the physical/technical properties of GaN-on-Si growth and corresponding improvements. Pricing for such material has come down significantly in the recent years. It is generally agreed that the magic cost target of 1.5 \$/cm² for epitaxial material, which is also the price point at which GaN technology becomes cost-competitive with Si-based components at the device-level, can be achieved within the next couple of years under the important assumption that the wafers can be produced in volume. A next logical evolution would be to make the transition to 300 mm wafer diameters (as demonstrated for RF power GaN-Devices by Intel), but it is as yet an open question whether this makes sense from an economical perspective.

Voltage Rating—Standard products of GaN-on-Si typically feature an epilayer thickness of 4 μm to 6 μm, yielding a voltage handling capability of 650 V, including derating for temperature and lack of avalanche capability. Recent literature reports on boosted voltage rating of epi-wafers to values beyond 1200 V at room temperature by improvements in epitaxial recipes as well as increased layer thickness. However, due to the high intrinsic strain in GaN-on-Si layer stacks as well as the drive towards the adoption of semi standard substrate thicknesses, there is a fundamental limit to the maximal thickness (and breakdown voltage) that can be achieved. One possible way to increase the voltage rating of GaN-on-Si devices is the removal and replacement of the substrate, although questions concerning manufacturability and reliability of such an approach remain. On the other hand, for higher breakdown voltages the chip area utilization and the fact that large electric fields have to be handled on top of the active device becomes more and more problematic. True vertical GaN devices where the off-state voltage is block over an n-doped vertical drift region become increasingly important.

Lateral device architecture—Usually lateral devices embed a pGaN gate architecture or use a cascode topology to achieve n-Off behavior. Recently studies have shown the potential of MOS gate on GaN with oxide such as Al₂O₃ or SiO₂ to achieve a stable n-Off behavior. This novel gate architecture is expected to increase the reliability of the overall transistor by the reduction of the gate leakage. Nevertheless this technology requires a highly stable and well-engineered oxide/GaN interface as well as a high quality oxide with limited trapping to ensure a stable V_{th} of the transistor during operation. Local substrate removal, introduced by Imec and CNRS Lille, also are a valuable solution to increase the lateral breakdown beyond 2 kV.

Transport properties—The hetero-structures are typically based on AlGaN barrier material and have a sheet resistance of around 400 Ω/sq (which directly influences the device’s on-state resistance). Future developments will make the sheet resistance to be reduced to values below 200 Ω/sq. by adopting highly polarized AlN barriers or by using lattice matched InAlN barriers. Recent work at Fraunhofer also demonstrated that heterostructures based on alloys of scandium (AlScN/GaN) can benefit of a strong increase of the polarization, leading to much higher 2DEG density in GaN HEMTs. On the other hand, an increased 2DEG density will increase the device capacitance, which is undesirable for switching.

Vertical Devices—Besides lateral devices, also vertical devices are being investigated. They hold the promise of higher attainable power densities as well as avalanche capability. Although the structure does not have the advantage of electron transport along the two-dimensional electron gas (2DEG), the high channel mobility of the MOS channel provides a better R_{on} × A than other WBSs in the breakdown voltage range from 600 V to 1.5 kV. The vertical current flow makes this type of device more sensitive to (vertical) threading dislocations. Therefore, this technology requires a high-quality GaN substrate and innovative and optimized growth technology on it. The quality of GaN substrates for these applications is also improving. Although not yet in practical use, manufacturing process technologies such as low doping epitaxial growth, Mg ion implantation, and low damage etching have been advanced. However, the major problem of reducing wafer cost still remains. In MOS-based devices, the choice of the insulator and the processes to control the trapped charges are still debated issues. Many device concepts are currently competing against each other, in this connection vertical FinFETs should be mentioned. They do not need any p-type doped epitaxial layer and rely on electron accumulation at the gate insulator /semiconductor interface. Due to the absence of a p-type doping they do not show any

reverse recovery effects and therefore outperform most of the other vertical device concepts. There are some literature reports about the development of GaN superjunction devices with superior performance. However, the practical implementation is to date troubled by issues, e.g., to perform the trench regrowth of p-type GaN.

Development of GaN substrates—Upgrading the quality of GaN substrates has been a major challenge for vertical GaN power devices. Mainstream of the fabrication method of GaN substrates is thick GaN growth on sapphire using high-speed HVPE method, which has adequate buffer layer to remove GaN from sapphire. Though the method is conventional, the quality of the GaN substrate is drastically improved recently. The dislocation density was reduced by one order magnitude from middle 10^6 cm^{-2} to middle 10^5 cm^{-2} . Moreover, to reduce the dislocation density, combinations of ammonothermal method or sodium flux method with HVPE method are being developed. With this method, the dislocation density can be reduced by one or two orders of magnitude compared with conventional high-quality GaN substrates. The developed wafer size is also expanding from 2" to 6". However, as main market of the GaN substrate at present time is optical devices (LEDs and lasers), needs for large size substrates is still small. When large devices such as power devices become mainstream, the substrate costs will become lower. However, the breakthroughs for drastically cost down are still required, which are, for example, slice technologies of bulk GaN and wafer bonding to backing plates.

On-chip integration—A further path to cost reduction for GaN technology is to include several components on a single chip, allowing to save component, packaging and design costs for creating a full system. Beyond merely costs advantages, a monolithic integration will also enable the main potential of GaN to be tapped, which is a high commutation speed, leading to an increased switching frequency for the power circuit. Discrete Si power components can be quite readily integrated in a power circuit; however, GaN components can deliver high power at a fast switching frequency. These properties lead to a stringent requirement on the design of circuit and interconnect parasitic. Integrating, for example, two switches on a single die can also significantly reduce interconnect parasitic, offering further system-level performance benefits.

3.3.3. SiC-DEVICES AND SUBSTRATES

Compared to the standard bulk silicon, SiC has superior properties for the application in power electronics, i.e., higher breakdown voltage, lower losses as well as the capability for high frequency switching and high temperature operation. These performance data are related to important material properties, e.g., wider energy bandgap, electric breakdown field, and thermal conductivity. The current maximum SiC wafer size in production is 150 mm.

SiC is on the verge of market penetration for very high current values (50 A and above) and high voltages over 1700 V with the potential to allow for voltages far above 10 kV. In this respect it is the most advanced material. Next to improving device parameters and extending device limits the appropriate integration of such advanced devices in new module architectures is of utmost importance to exploit all benefits. The present state of the market is as follows:

- SiC device manufacturer—Infineon, Wolfspeed, Mitsubishi, STMicroelectronics, ABB, Bosch, ON Semiconductors, ROHM etc.
- Packaging—All SiC device manufacturers, Semikron, Vincotech, Danfoss, etc.
- For devices up to 2000 V, the position of Europe is quite good and comparable to that of Japan. But, there are huge publicly funded projects in China and the USA to catch up, with Japan and USA poised to take over the lead for voltage classes higher than 2000 V.

China, Japan and the USA have started funding key development projects for future devices. Power semiconductors are the key components of any power electronics circuit. An ambitious funded project in Europe targets to demonstrate the complete chain for 200 mm SiC technology (with the development of an industrial pilot line) within the next 5 years. Recently, SiC devices with breakdown voltages of 10 kV and higher have been developed for high voltage (HV) applications. This voltage rating noticeably surpasses that of commercial Si devices, such as 6.5 kV IGBTs. The breakdown voltage rating of this new device generation has not yet reached its limit. Latest SiC HV power semiconductors—for example, MOSFETs, IGBTs, diodes and GTOs—have been presented in order to offer innovative opportunities. Its properties make SiC the ideal material for high current ratings (50 A and higher) for high voltages.

In the long term, large area cubic 3C-SiC is a promising material for 600-900 V devices, but strong efforts in heteroepitaxy technology are needed to reduce the density of killer defects (stacking faults, anti-phase-boundaries, etc.).

Due to its wide bandgap SiC is highly suitable for applications at higher temperatures. Currently a wide variety of sensors for sensing at high temperatures are available. However, most of these do not have a high signal/noise ratio. SiC amplifier circuits will cope with this issue. In addition, for high-temperature applications, stable multilayer metallization is required.

3.3.4. ALTERNATIVE WIDE BANDGAP SEMICONDUCTORS

Besides GaN, a number of other wide-bandgap materials exist. The most cited is diamond, which is considered to be the “ultimate material”. However, technological obstacles (lack of efficient n-type doping, conductive surface channels and difficulties to make ohmic contacts) have for a long time blocked the demonstration of performant devices. Unless spectacular progress is made on these issues, no real-world implementations are foreseen and as such, diamond is not included in the roadmap. Besides SiC (for which a separate part of the roadmap is dedicated), we identify two major candidate materials—AlN and Ga₂O₃.

AlN native substrate—is probably the most interesting wide bandgap material, because it combines high thermal conductivity with a very large bandgap of 6.2 eV, higher than that of diamond. As a thin film it can be easily combined with GaN-based materials to form heterojunctions (such as HEMTs). Currently few AlN bulk substrate suppliers exist (Hexatech, Crystal-N) and the substrates are 2” in diameter or below. However, the potential of AlN based electronic devices for both power switching and mm-wave applications is very high so that AlN crystal growers are more and more facing the demand towards larger diameter AlN substrates.

Gallium oxide—The latest prospect in wide bandgap materials is Ga₂O₃. As it can be grown from the melt, it is potentially a low-cost material. It can be doped (with some difficulties) to make vertical devices and can be combined with Al₂O₃ as a gate dielectric. Recently, a number of publications reported on promising device characteristics. Ga₂O₃ is a material system that allows processing devices with improved breakdown voltage compared to SiC and even GaN. The main advantage stems from the fact that the material can be grown from the melt and can thus be produced at very low cost compared to GaN and SiC. However, the main disadvantage of this material is the very low thermal conductivity, which is a really undesirable property for power devices. Moreover, the absence of a p-type doping in Ga₂O₃ is a serious concern, which can be partially mitigated by the integration with p-type oxides. Up to now most of the developed Ga₂O₃ devices rely on lateral device concepts. However, Ga₂O₃ can only demonstrate its unique advantages at very high voltages in the range between 1000 V and perhaps 5000 V. Therefore, vertical high-voltage Ga₂O₃ power switching architectures may be the better choice. In fact accumulation type FinFET technologies are being developed. This concept does not need any p-type doping, is highly scalable and therefore allows for extremely high-power density devices. In contrast to 2DEG based GaN devices Ga₂O₃ devices show a far lower thermal dependence of the electron transport properties, which may make it possible to run them at higher baseplate temperatures. This property in combination with novel heat removal techniques may help to alleviate the disadvantage of the principally low thermal conductivity. Further research will have to demonstrate if devices can be fabricated that can solve this issue.

Diamond is considered by many the ultimate material for fabricating power components. It has the highest breakdown strength of any known material, combined with an extremely high thermal conductivity. However, due to the wide bandgap it is also challenging to find a suitable dopant for diamond. Apart from this the growth of the material is also quite challenging. Initial demonstrator transistors are available in diamond, but much work will be needed to improve performance towards practical performance and demonstrate the capabilities of the material system.

Table MtM-2 Smart Energy Difficult Challenges

Difficult Challenges 2019-2025	Potential solutions
<p><i>GaN-on-Si substrates, large diameter (8”), low defectivity and low cost.</i></p>	<p>New generation of MOCVD reactors allow to scale to 200 mm and 300 mm Move from multi-wafer to single wafer reactor concept for 300 mm for better control on temperature profile across the wafer, bow and warp Improve substrate quality by growing on non-Si substrates (e.g., poly-AlN) and (potentially) liftoff</p> <p>Strain engineering</p> <ul style="list-style-type: none"> • Growth and processing of wafers thicker than SEMI standard (Si fab compatibility to be solved) • Optimized nucleation, layer-sequence, and growth processes • Growth on CTE matched substrates (e.g., GaN-on-Si/AlN) • Alternative approaches: GaN-on-SiC → Quanfine® (inexpensive semi-insulating SiC substrates required). DENSO® (GaN epi-growth on 4 degree off-axis 4H-SiC without buffer layers by tri-halide vapor phase epitaxy) • GaN-on-Sapphire <p>Low defectivity</p> <ul style="list-style-type: none"> • Clean Si substrates • Optimized epi growth (crystal quality, dislocations) • Epi tool automation • Improved reactor cleaning processes

	<ul style="list-style-type: none"> Improved epi wafer cleaning processes Better defect detection tools. Binning capability pits vs. particles Enabling CL as defect (dislocation) detection tool for production monitoring In-line detection and monitoring of Si, C, Mg doping <p>Low cost</p> <ul style="list-style-type: none"> Increased epi growth speed Improved break-down behavior (more V/μm buffer thickness) Shortened reactor cleaning processes (e.g., in-situ cleaning) Epi tool automation Improved tool up-times and reduction of maintenance intervals Less monitoring effort due to increased process stability Eventually GaN-on-Si in 300 mm (beyond 2025)
<i>GaN Devices—Low leakage, reliability, avalanche capability</i>	<p>Low buffer leakage through improved substrate quality Reduction in gate leakage by Schottky gate engineering or by adopting an alternative regrowth of the gate after recess Better reliability by improved UID and barrier quality (less defects, better doping control). Improve hot carrier injection by improving quantum well</p> <p>Low leakage</p> <ul style="list-style-type: none"> Reduced dislocation density in GaN epi pGaN devices—gate module engineering, Schottky type vs. ohmic gate contact <p>Reliability, incl. dynamic properties</p> <ul style="list-style-type: none"> Electric field management Reduced dislocation and defect density Optimized buffer trapping Improved passivation processes and materials (e.g., atomic layer deposition) Improved GaN purity (in particular in unintentionally doped GaN channel) Engineering of hole injection for trapped charge compensation Resistivity balance in layer stack TCAD model for buffer & device leakage, trapping, detrapping For p-GaN gate module—Leakage balance between Schottky diode and pn diode
<i>GaN MIS-Gate structures</i>	<p>Achieve a stable gate architecture with limited trapping effects and low leakage jointly to a n-Off behavior by reconstructing the etched GaN surface and choosing the adequate insulator Reduce Dit at the dielectric interface Insulator charge control by post-annealing and/or plasma and in-situ doping Might require regrowth of, e.g., in-situ SiN or AlN and subsequent ALD</p> <ul style="list-style-type: none"> Atomic layer etching for gate recess etching, atomic layer deposition for gate dielectric Possibly fundamental limitation due to separation of 2DEG channel and trapping interface by barrier hindering rapid charge exchange during switching Invention/development of appropriate gate dielectric required, which prevents positive charge incorporation during positive gate biasing
<i>Regrown ohmic contacts</i>	<p>Today ohmic contact resistance is $\sim 0.1 \Omega\cdot\text{mm}$ with a standard Ti/Al metal stack, which is sufficient for power devices Silicon doping for n ohmic contacts High temperature ion implantation techniques in combination with high temperature pulse activation need to be investigated</p>
<i>On-Chip Integration</i>	<p>pMOS device that is compatible with the standard HEMT process flow Creation of a 2DHG based devices. Some studies showing the potentiality of AlN/GaN Barrier to create such a channel</p>
<i>GaN modules</i>	<p>Parallellization of several GaN die in a module Co-integration of the driver (and controller ?) Simulation approach to optimize parasitic inductance (“digital twin”) Monolithic GaN driver integration wherever necessary and of advantage. This needs to be aligned with the hybrid GaN die integration capabilities.</p>
<i>High power switching of GaN devices with high reliability</i>	<p>Epi without trapping effects to decrease hot electrons tapping during Hard Switching operation which limits the SSOA of commercially available devices</p>

<i>GaN Multi MHz operation @ 100 W and more</i>	Decrease as much as possible the internal parasitic capacitance as well as the dynamic R_{on} of the transistors operated in a multi-MHZ switching mode
<i>Channel conduction in 4H-SiC trench-MOSFETs</i>	Alternative approaches to standard nitridation (e.g., post-oxidation processes and implants)
<i>Ohmic contacts on p-type 4H-SiC for body-diode and bipolar devices</i>	Alternative solutions (Ti- or Al-based) to the standard nickel silicide
<i>4H-SiC devices on 8-inches substrates</i>	Development of equipment able to guarantee processes uniformity (high-temperature annealing, implantation, oxidation).
<i>Development of cubic polytype (3C-SiC) for 600-900 V devices</i>	Compliant substrates to reduce the defect density of 3C-SiC on Si substrates
Difficult Challenges 2025-2034	Potential solutions
<i>Move to 300 mm</i>	Single wafer MOCVD reactor
<i>GaN automotive qualification</i>	Guarantee low ppb levels Need good epitaxy
<i>GaN Smart power</i>	Requires all elements from monolithic GaN. Cost reduction of GaN wafers to take benefit of an all-GaN technology. However, a well-adapted combination between Si logic devices and GaN power switching devices should be feasible as well. This approach allows combining the advantages of both worlds.
<i>Development of device process on 3C-SiC</i>	Adapting the main processes used for 4H-SiC devices, special challenge in implanted dopant activation.
<i>III-Nitrides growth on arbitrary substrates</i>	Use of 2D materials with hexagonal structure (graphene, MoS ₂ or h-BN) as compliant interlayer for quasi-van der Waals growth of III-N.
<i>Improved thermal management of GaN power HEMTs</i>	Use of high thermal conductivity graphene structures as heat sinks for localized heat dissipation in high power GaN HEMTs.
<i>Monolithic integration HS/LS</i>	Potential solutions for resolving cross-talk and back-gating effects (electrical isolation of HS/LS and backside): - Junction isolation; - GaN-on-SOI; - GaN-on-other insulating substrates.
<i>On-Chip Integration</i>	<ul style="list-style-type: none"> • Homogeneous integration of driver, control, and protection functions by using GaN process design kit • Realization of device library based on pure GaN technology • Realization of true p channel devices with acceptable mobility • Heterogeneous integration of silicon and GaN technology • Chip bonding or wafer bonding as conceivable options
<i>Revolutionary shrink path</i>	<ul style="list-style-type: none"> • Three-dimensional gate structures • FIN-FET devices • Nano-structured gates (e.g., Tri-Gates) • Multi-channel devices
<i>Vertical devices</i>	Development of large area (150mm) GaN bulk substrates with high conductivity (e.g., 0.02 \square cm) at a reasonable price (e.g., 1500\$)
<i>GaN superjunction devices</i>	Simulations show that the specific on-resistance of vertical superjunction devices are 10x and 1000x lower than 2H-GaN 1D limit with breakdown voltage 1kV and 10kV, respectively (Ref—Xiang Zhou et al, Compound Semiconductor week 2019)

3.4. RECOMMENDATIONS

3.4.1. SJ

Due to its market dominance it is of utmost importance to continuously invest in the research and development of Si-based super-junction devices in order to grow/preserve strong presence of European companies in the 500-1000 V power-conversion markets. In addition to the continuous reduction of the $R_{on} \times A \times \text{cost}$, in order to reduce variable product costs, further growth of fully automated large scale 300 mm wafer production is necessary for cost reduction via economy of scale. Finally, R&D synergies that are related to chip shrink require further focus since these topics are also relevant for WBGs (i.e., novel packaging concepts, heat management, etc.).

3.4.2. FIELD PLATE TRENCH MOSFETs:

In the last years more competitors developed power MOSFETs with the advantageous field plate trench MOSFET concept in 12" fabs. The technology leadership is currently shared within different manufacturers all over the world. With further design and process optimizations this silicon technology can be further improved that can again lead to single technology leaderships. For 15 V and 25 V, a roadmap towards monolithic integrated features can further reduce power losses in computing DCDC applications.

In the medium voltage range of 40 V-300 V, the Si technology is partly competitive to GaN devices due to the cost position and the fact that the chip shrink is limited for various applications due to the thermal requirements.

For high performance applications it is expected that GaN increases market share in future for the medium voltage market.

3.4.3. IGBT

In the next decade further strengthening of the development of Si-IGBT technology is crucial. Due to the fact that wide bandgap semiconductors will take over only parts of the market, a very long coexistence of Si-based technologies with wide bandgap is foreseeable over a long timeframe of at least two decades.

Fully automatized large-scale 300 mm wafer production of Si-IGBT power technologies is still be a key lever for cost reduction and competitiveness to Japan and Asia, especially the upcoming China. Further R&D efforts in this direction are recommended. From a technical point of view a strong focus has to be put on the optimization of the fine patterned trench cell, monolithic integration of IGBT and FWD (RC-IGBT) and vertical shrink of the device with highest accuracy. Additionally it is highly recommended to further enhance R&D efforts for advanced chip interconnect technologies (e.g., cost-efficient sintering technologies) and advanced packages to enable higher device operation temperature and higher power density. The latter is fitting strongly together with major requirements coming from wide bandgap technologies and therefore would pay off multiple times.

3.4.4. SMART POWER

Power device "safe operating area" and reliability are today driving the major challenges for further performance improvement. Tailoring to specific mission profiles will most likely start to become very important in the future to secure power devices improvement.

Integration cost is a key factor to be carefully evaluated. In Smart power IC, power stages are occupying a part of the total product area. Added process cost that may be needed to enable the performance improvement has to be carefully evaluated at global level to evaluate the impact on the product die cost.

Planar isolated architecture is today a must in Smart Power IC for the realization of multiple power topologies (half bridge, full bridges) together with driving circuitry often with different voltage class management.

3.4.5. GAN-BASED DEVICES

One of the major restraints of the GaN semiconductor devices market is the high production cost of pure gallium nitride as compared to silicon carbide, which has been, in addition to main-stream silicon, a dominant semiconductor material for high voltage power electronics for a decade. The various costs involved in the production of GaN devices include cost of substrate, fabrication, packaging, support electronics and development. Thus, high cost is one of the major challenges in the commercialization of GaN based devices. Though producing GaN in large volumes can help overcome these issues, currently there is no widespread adopted method for growing GaN in bulk due to high-operating pressures and temperatures, low material quality and limited scalability. It is therefore highly recommended to further enhance R&D efforts for improving GaN-on-Si epitaxy and corresponding devices with respect to quality, performance, and cost. This will be the all-important basis for a broad adoption of GaN devices in the power electronics market.

Moreover, GaN offers unique possibilities for integration of systems, ranging from simple gate drive and protection concepts, over monolithic integration of multiphase half-bridges, up to the realization of intelligent monolithic Smart Power GaN-based systems. Substantial R&D activities will be needed to prevent unwanted electric coupling between the integrated devices and to solve all the challenges associated with enabling comprehensive device libraries with GaN HEMT process and manufacturing concepts. The ultimate GaN device may even need a paradigm change as GaN-on-Si techniques may turn out problematic for integrating high power switching bridges. In this regard, novel substrates or wafer transfer technologies may need to be considered. Such technologies are already available for other kinds of devices but may be combined with GaN epi and processing technologies.

3.4.6. SiC-BASED DEVICES

It is highly recommended to focus on the growth of thick epitaxial layers with low defect densities and high carrier lifetimes for high-voltage devices, e.g., bipolar devices. To really deal with high voltages, the passivation on chip, e.g., junction termination only or advanced in-chip passivation, as well as in the module for 3D integration has to be addressed.

Next to the costs and the yield of the SiC devices, the reliability issues have to be addressed. The current devices show a high robustness against voltage and temperature. But to derive adequate reliability and lifetime predictions, novel accelerating lifetime testing and modeling of these devices has to be established. To exploit all the benefits of high-current, high-voltage devices, advanced 3D integration concepts have to be developed.

For a successful WBG system integration it is necessary to exploit the full potential of these devices, hence the following infrastructures need to be developed:

- Packaging and system integration technologies enabling low parasitic inductances to master EMC issues
- Packaging and system integration technologies enabling reliability at higher temperatures
- Handling higher voltages on package/module level and system level—SiC in medium voltage (MV) applications e.g., in traction and industry
- Low inductance packaging and integration technologies—power PCB with chip embedding, system-in-package (SIP), switching cell in a package, integrated power modules
- Passive components for fast switching—mainly inductors, reduce losses at high switching frequencies, thermal management of (integrated) passives
- Characterization, testing, modeling and reliability analysis of WBG packages, modules and converters
- Cost of substrate improvement by re-usable substrate technology, e.g., smart-cut, cold split
- Increase productivity by enabling 200 mm wafer diameter transfer projects
- Exploit novel device architectures, like SiC-SJ and SiC-IGBT, to improve device performance
- Further understand SiC-specific reliability issues like bipolar degradation, bulk crystal quality, gate oxide extrinsics
- Further integration of “sensor on a chip” architectures like in-situ current, temp sensors
- Engage novel driver concepts to improve ease of use and improve operational robustness, e.g., short-circuit detection on system level

3.5. SUMMARY

The Smart Energy devices roadmap presents the medium and long-term targets of the innovative silicon devices (superjunction, IGBT, MOSFETs) and the two main wide bandgap semiconductors—WBS, (SiC and GaN). Some indication will also be provided for the new promising WBS— Ga_2O_3 , AlN, and diamond. The aspects that will be covered within this roadmap are as follows: i) materials and processing issues (including device architectures); ii) applications; iii) technology and design challenges, and iv) figures of merit.

Power devices based on wide bandgap semiconductors (WBS) like GaN, SiC, Ga_2O_3 , are poised to play an important role in future power electronics systems in addition to Si based workhorse technologies like IGBTs, superjunction MOSFETs (e.g., CoolMOS), low/medium voltage (trench) MOSFETs (e.g., OptiMOS) and smart power BCD devices. WBS has a high breakdown strength and, in the case of GaN, allows for fabrication of high electron mobility lateral transistors, for which the electron mobility is not degraded as would be the case for traditional silicon MOSFETs. Together, these facts allow the fabrication of devices, which have orders of magnitude better trade-off between the specific on-resistance and the breakdown voltage. The roadmap for devices has been set up along the following four tracks: the first considers silicon-based devices, the second focuses on GaN based devices starting from materials towards integration, the third track is related to the evolution of SiC (again from materials to applications), and finally, future material systems (AlN, diamond, Ga_2O_3) are considered which could offer benefits over the actual WBS in certain domains.

4. ENERGY HARVESTING

4.1. INTRODUCTION

As the communicating systems market is booming, the role of energy harvesting (EH) will increase commensurately. Indeed, the number of connected devices is planned to increase by a huge factor of 200, while the number of mobile phones is just planned to increase by a factor 3. Connected devices are going to be used more and more in several fields such as healthcare, wearable, home automation, etc. The IoT market is also growing considerably, leading to the boom of

wireless connected devices using a portable power source, and so highlighting the importance of energy needed to supply them in view of the limitations of current battery technology. In this particular case, we are focusing on small devices mainly connected at the edge with low power consumption typically in the sub mW range (many at a few tens of μW).

Providing energetic autonomy to electronic devices will be a key factor in booming technologies like sensor networks and IoT. This is true for applications with specific requirements, where a simple battery would not be sufficient; where using power cables increases largely the cost or complexity (i.e., avionics), or when the number of devices are so numerous that changing batteries could increase the maintenance cost and the logistics become unmanageable. Other examples are in harsh environments where electronic devices cannot be reached/accessed easily, or in biomedical devices. The interest in the EH concept also encompasses development of new devices compatible with silicon technologies for implementation in the fabrication line, which would attract the interest of semiconductor companies. New green solutions based on avoiding toxic and rare materials are of high interest for the dissemination of energy harvesters.

Different ambient energy sources can be exploited and converted into electricity—sun or artificial light, heat, RF power (either intentionally transferred or harvested from radiating devices), mechanical movements and vibrations, etc. Moreover, this converted energy needs to be used and transferred wisely to sensors, microcontrollers or other electronic components included in the system. Thus, power management circuits and energy storage devices also become an essential element. (See Figure MtM-6.)

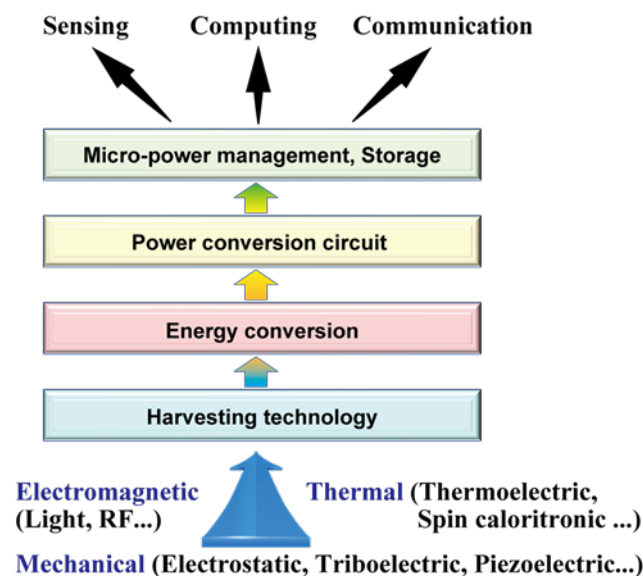


Figure MtM-6 Survey of energy harvesting technologies

In this white paper, we have assessed several promising technologies for EH and power management circuits including photovoltaic cells for outdoor/indoor light E; thermal energy harvesting; mechanical EH based on three concepts: 1) piezoelectric materials, 2) electrostatic and 3) electromagnetic energy conversion; RF energy harvesting/wireless power transfer; power management circuits, and finally microbatteries and microcapacitors for energy storage.¹²

4.2. SCOPE

Targeting EH technologies with low fabrication cost, with high efficiency, and without toxic/rare materials is the main challenge. Adding flexibility and/or transparency is also an increasing demand for compatibility with wearables applications.

For the semiconductor companies, the interest is also to develop new devices compatible with silicon technologies. The fabrication of components dedicated to energy harvesting and in particular to thermal energy is of high interest as no solution based on silicon technologies is available for implementation as of today.

¹² Ahopelto, Jouni, Ardila, Gustavo et al. "NanoElectronics roadmap for Europe: From nanodevices and innovative materials to system integration." *Solid-State Electronics* 155 (2019): 7-19; H. Akinaga, H. Fujita, M. Mizuguchi, T. Mori, "Focus on advanced materials for energy harvesting: prospects and approaches of energy harvesting technologies", *Sci. Technol. Adv. Mater.* 19, 543 (2018). <https://doi.org/10.1080/14686996.2018.1491165>.

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Mechanical EH rely typically on input vibrations, and one of the main challenge is the compatibility with low frequency vibration source (most of applications use frequency vibrations <100 Hz) and the increase of the operational frequency bandwidth.

For materials of the thermoelectric EH, the high electrical conductivity and Seebeck coefficient and low thermal conductivity are required, but the requirement is hard to be achieved simultaneously.

Although photovoltaic EH technology is mature (silicon based) for both outdoor/indoor applications, emerging materials are promising for their potential to add flexibility and low weight (thin films) at reduced cost and high efficiency (organics, dye sensitized, perovskites, etc.).

RF harvesting systems (rectifying antennas or referred to as “rectennas”) have been widely used and studied in recent years due to the vast presence of RF sources in humanized environments. However, too low power densities have usually been experienced because of RF regulations and RF power transfer “on demand” solutions are currently preferred and are exploited in a large number of passive RF system applications, such as RFID, wearable or implantable devices, realized using eco-compatible materials.

Thin film solid-state solutions for energy storage have existed for some years now but more energy dense and higher power options at lower cost are required. Initial prospects to increase those may involve multilayer options and the use of thicker electrodes. New materials for both electrodes and electrolyte with increased conductivities will assist in meeting the targets. Nanostructuring and new printing capabilities are also of interest.

The main challenges associated to power management circuits are related to the miniaturization of the system embedding micro-magnetic components or power converters; the reduction of overall leakage enabling low power consumption, and the development of energy-aware circuit design techniques for achieving operation in ultra-low power regimes.

4.3. STAKEHOLDERS

At present the “power IoT user community” of academic researchers and technologists struggles to develop industry-relevant solutions as there is a lack of focus on system-level assess and optimizations of their innovations. Similarly, there is a lack of cross-disciplinary interactions between stakeholders. However there are a number of initiatives underway to address this such as the EnABLES access infrastructure project (www.enables-project.eu) and associations such as PSMA (www.pdma.com), Energy Harvesting Consortium (<https://www.nttdata-strategy.com/ehc/en/about/index.html>) and the Energy Harvesting Network (<http://eh-network.org/>) creating communities developing technology roadmaps, workshops and networking events (e.g., EnerHarv www.enerHarv.com). The communities need to capture not just the developers and manufacturers of materials and devices but also the system integrators, users, hardware, software and ICT protocol architects creating the ecosystem that needs these technologies. These need to be underpinned by technology offering such as those outlined in this document but introduced in a “solving the grand challenges” way. Combining these will enable the accelerated development of usable energy harvesting/power management solutions to address the battery life challenge. Increasing the stakeholder network, not only in terms of critical mass but also in diversity, will yield many new synergies, particularly in engraining the mindset of “thinking about power” at the very early conceptual stages in designing IoT systems. This will extend beyond electronics to ICT and MEMS, software, industrial design and data analytics spanning a broad variety of end applications such as Medtech, smart cities, Agri-tech, environmental monitoring and Industry 4.0.

Mechanical EH—Among vibrational energy harvesters, the piezoelectric and electromagnetic transduction are the most exploited in research and at industrial level. Several companies commercialize piezoelectric EHs: MIDE, Smart Materials and Piezo Systems in USA, and PI, CEDRAT, Smart Materials GmbH and ARVENI in Europe. Among industries commercializing Electromagnetic EHs, EnOcean, Perpetuum (spin-off from Univ of Southampton, UK), Flexous (spin-off from TU Delft, Netherlands), Revibe (Germany) are active in this particular area.

Thermal EH—All commercially available modules are based on Bi₂Te₃ material with a ZT value close to 1 (Laird Technology, Thermogen in USA and Micropelt in Germany...).

Photovoltaic EH—Silicon technology is very mature for outdoor conditions (Jinko Solar, Canadian Solar, Hanwha Q-cells, Sunpower...) but also for indoor (e.g., Panasonic in Japan, Solems in France). However, other firms are commercializing, for indoor and/or outdoor energy harvesting applications, high efficiency, transparent and/or flexible solar cells (e.g., G24 Power in UK, OPVIUS in Germany) made of different materials (III-V compound, dye, organic, etc.) than Si.

Energy storage—Thin film integrated microbatteries are the option being investigated for distributed sensors coupled with energy harvesting and micropower management. Europe has globally competitive expertise in storage technologies (i.e., Ilika Technologies in UK and ITEN in France).

Micro-power management—Major silicon foundries have proposed in recent years dedicated products operating down to few μW and few hundreds mV, along with very tiny implementations requiring few components. (STMicroelectronics in Europe, Texas Instruments, Analog Devices, Linear Technology, etc.).

4.4. TECHNOLOGY STATUS, REQUIREMENTS AND POTENTIAL SOLUTIONS

The diagram below gives an overview of the energy harvesting concepts that are covered so far in the IRDS.

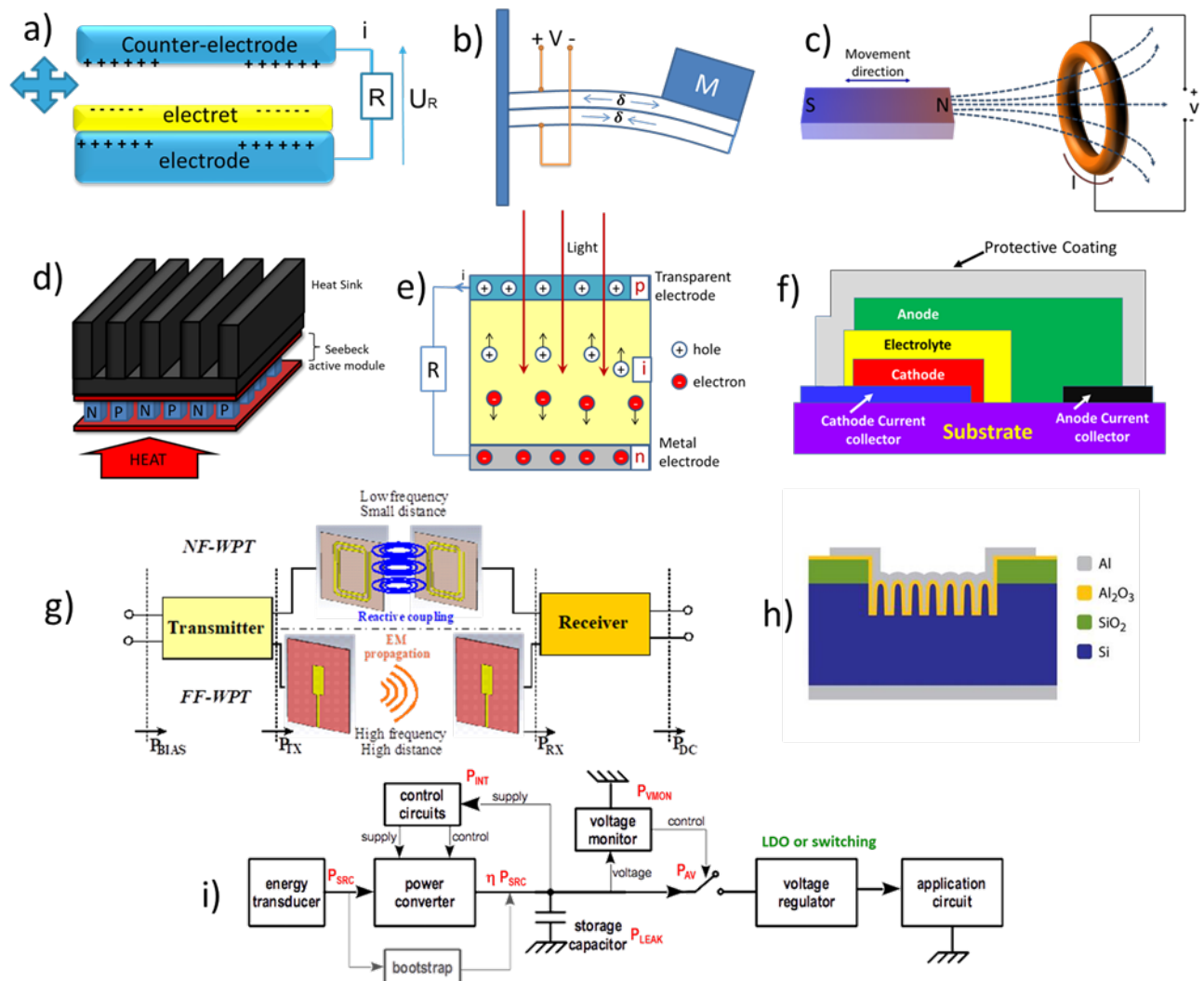


Figure MtM-7 Basic structures of the energy harvesting concepts covered so far in the IRDS Roadmap.

a) cantilever-based electret energy harvesters,¹³ b) classical structure of a piezoelectric energy harvester,¹⁴ c) illustration of Faraday's law that governs electromagnetic generators, d) basic Seebeck thermo-generator structure schematic with heat sink,¹⁵ e) a-Si pin solar

¹³ S. Boisseau, G. Despesse, T. Ricart, E. Defay and A. Sylvestre Published 31 August 2011. IOP Publishing Ltd, Smart Materials and Structures, Volume 20, Number 10.

¹⁴ Larcher, L., Roy, S., Mallick, D., Podder, P., de Vittorio, M., Todaro, T., Guido, F., Bertacchini, A., Hinchet, R., Keraudy, J. and Ardila, G. (2014) Vibrational Energy Harvesting, in Beyond-CMOS Nanodevices 1 (ed F. Balestra), John Wiley & Sons, Inc., Hoboken, NJ, USA. doi: 10.1002/9781118984772.ch6.

¹⁵ Pucasu, O., Monfray, S., Savelli, G., Maitre, C., Pemeant, J. P., Coronel and Guyomar, D. (2012, December). An innovative heat harvesting technology (HEATec) for above-Seebeck performance. In Electron Devices Meeting (IEDM), 2012 IEEE International (pp. 12-5). IEEE.

cell,¹⁶ f) typical thin film microbattery structure, g) End-to-end block representation of a wireless link involving either near- or far-fields,¹⁷ h) Schematic diagram of a Si-nanowire-based MIS capacitor, i) Block diagram of a battery-less power conversion and management system including a duty-cycled load.¹⁸

In the following sections, several promising technologies for EH and power management are assessed, such as: photovoltaic cells for outdoor/indoor light EH, thermal energy harvesting, mechanical EH based on three concepts (piezoelectric materials, electrostatic and electromagnetic energy conversion), RF energy harvesting/wireless power transfer, power management circuits and storage devices (microbatteries and microcapacitors).

4.4.1. MECHANICAL ENERGY HARVESTING

- *Electrostatic transduction*

The principle of operation relies on the use of mechanical forces to do work against the attraction of oppositely charged capacitor's plates; thus those generators can be considered as mechanically variable capacitors whose plates are vibrated by the movement of the vibration source (Figure MtM-7.a). Typical structures include capacitor plates in form of fingers installed in central oscillating mass and in stationary comb. When the capacity is at its maximum value the electric charge stored in the capacitor is transferred to the external battery. To ensure good capacitive coupling between oscillating mass and stationary comb, the distance between fingers has to be as small as possible. In order to avoid the charging and discharging cycles, electrets (dielectric material with trapped electrical charges) can be implanted into one of the two parallel electrodes. This technology is a promising solution for CMOS-compatible, low-cost, micro-scale EHs. An increase of the surface electrical potential with an appropriate electret is one of the difficult challenges. However, the high-density charge of the electret may affect static adhesion and friction forces which hinder the expected motion of the device.

- *Piezoelectric transduction*

Most piezoelectric harvesters are based in a resonating device made of a cantilever beam, covered by a piezoelectric material and an inertial mass attached (Figure MtM-7.b), these devices are tuned to the characteristic mechanical vibration frequency of the application. As the cantilever is bent, strain is transferred to the piezo layer, which induces an asymmetric charge distribution, and therefore a voltage is generated. MEMS devices are very promising because their fabrication is CMOS compatible. Many companies exist actually exploiting this principle and integrating piezoelectric materials (mostly PZT, being toxic) on different substrates (metal foils, PCB, etc.). Since very recently, MEMS devices can be also found on the market by integrating AlN.

- *Electromagnetic transduction*

The operating principle of electromagnetic energy harvesting devices is based on Faraday's law, which states that a relative motion between a magnetic field and an electrical coil or a change in the flux linkage with a coil induces an electromotive force (EMF) in that coil (Figure MtM-7.c). The EMF depends on the strength of the magnetic field; the length of the coil, and the relative velocity (or flux linkage rate) between the magnetic field and the coil. The relative motion between the magnetic field and the coil can be produced by moving the magnets with respect to the coil or vice versa. The coil can be either wire-wound or micro-fabricated. The electromagnetic energy harvesters that have been researched are either macro-sized structures or miniaturized structures utilizing micro electro mechanical system (MEMS) fabrication techniques.

4.4.2. THERMAL ENERGY HARVESTING:

These devices convert thermal energy to electrical energy via the Seebeck effect (Figure MtM-7.d). There are two main technologies—bulk technology and thin film technology. The bulk technology is adapted for applications (e.g., automotive, industrial applications, etc.) for which the size of thermoelectric (TE) devices is not a constraint (sizes vary from some cm² to some tens of cm²) and for which high power is required (W to kW range). The thin film technology is adapted for the confined environment, for which the size is a key point (mm² to few cm²) and for which power from the μ W to mW range is required. Most of the commercialized thin film TE devices are made of Bi₂Te₃ active materials (toxic/rare/expensive/not compatible with Si technologies). The main FoM is ZT. For many years, Bi₂Te₃ has been the best TE material at room temperature with a ZT close to 1, and the objective would be to increase the ZT value up to 3. For realistic implementation of the technologies into our life, a multiscale design is required (Figure MtM-8).

¹⁶ http://panasonic.co.jp/es/pesam/en/products/pdf/Catalog_Amorton_ENG.pdf.

¹⁷ M. Piñuela, P. D. Micheson and S. Lucyszyn, "Ambient RF Energy Harvesting in Urban and Semi-Urban Environments," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 7, pp. 2715-2726, July 2013. doi: 10.1109/TMTT.2013.2262687.

¹⁸ A. Romani et al., *IEEE Computer* 2017.

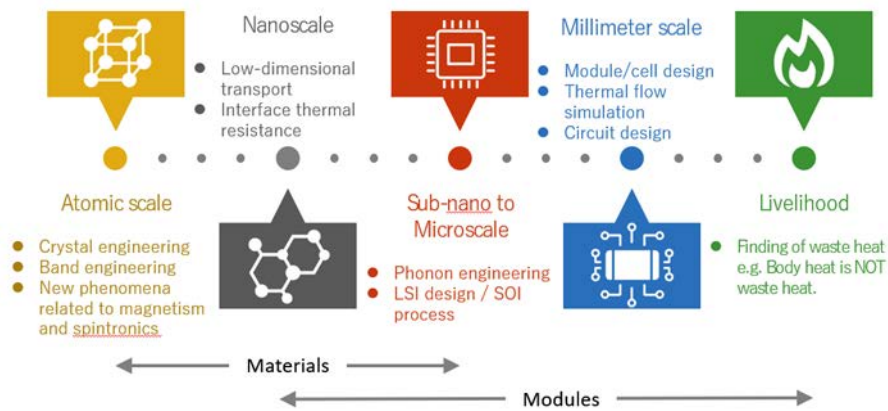


Figure MtM-8 Multiscale thermal design for thermoelectrics

4.4.3. PHOTOVOLTAIC ENERGY HARVESTING

The photovoltaic (PV) effect consists in the absorption of light by the semiconductor; the generation of electron-hole pairs and collection of charge carriers (thanks to the semiconductor device), allowing the generation of power (Figure MtM-7.e). The FoM usually used for solar cells working under sunlight is the power conversion efficiency (output power density divided by incident sun power density of 1 kW/m^2 , Solar spectra: AM1.5@25°C). However, the output power density of the solar cell is dependent on the incident light intensity; absorption and electronic properties of the material; spectral sensitivity of the solar cell to the light; electronic quality, and properties of the semiconductor device. Therefore for solar cells working in indoor conditions, standard outdoor measurement conditions are not relevant because artificial modern light (fluorescent, LED) present a different spectrum and far lower intensity compared to sunlight. For indoor light conditions, the parameter usually used is the output power density under specified artificial light intensity, but no standard measurement conditions are defined.

The photovoltaic production is dominated by silicon-based solar cells due to its abundance, well-known and mature technology, thanks to microelectronic industry. Indeed most of the outdoor commercialized solar cells are made of crystalline silicon (c-Si) and for indoor applications amorphous Si (a-Si) solar cells are commercialized. For outdoor solar cells, thin film cells (CdTe, CIGS, a-Si, organic, dye) are also commercialized, as well as high-efficiency solar cells working under concentrated sunlight. Similarly, for indoor applications, photovoltaic cells are also commercialized based on materials other than Si, e.g., III-V compounds, dye, organic, etc.

4.4.4. RF ENERGY HARVESTING/WIRELESS POWER TRANSFER

The wireless delivery of RF power has been used for many years and for various applications and power needs—from relatively large unmanned systems and associated power needs to very small battery-less devices.¹⁹ To reach this goal, two physically different mechanisms can be used (Figure MtM-7g): 1) the so-called far-field wireless power transfer (FF-WPT), which exploits the radiated far-field radio-frequency (RF) sources, either in the microwave (300 MHz–30 GHz) or millimeter-wave (30 GHz–300 GHz) and 2) the near-field wireless power transfer (NF-WPT), which exploits the near- (or reactive-) EM field in the low-frequency (LF: 30–300 kHz) or high-frequency (HF: 3–30 MHz). In the FF-WPT case, the radiation of an electromagnetic (EM) wave occurs through the exploitation of a radiating structure (antenna), and the corresponding radiated RF power can be intentional (in the case of FF-WPT) or unintentional/environmental (in the case of RF Energy Harvesting (EH) application). When far-field sources are involved, no direct interactions between the transmitting (TX) and receiving (RX) antenna take place, because the TX antenna sends the same amount of power whether or not a receiver is present. In the non-radiative NF-WPT case, inductive links (exploiting magnetic field) or capacitive links (exploiting electric fields) are established between co-located coils/wires or electrodes/metallic plates, respectively—being in the reactive field region, the power delivered by the TX coil/plate may be strongly affected by the presence and location of the RX coil/plate, if suitable design choices are not followed. As regards the commercial/research applications, the FF approach is mainly deployed when low- (FF-WPT) or ultra-low

¹⁹ N. Borges Carvalho et al., "Wireless Power Transmission: R&D Activities Within Europe," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 4, pp. 1031–1045, April 2014. doi: 10.1109/TMTT.2014.2303420.

(EH) power applications are envisaged. Only in space and military targets, where the costs are not an issue, high-power FF-WPT activities are present. For these reasons, the two approaches are almost complementary.

4.4.5. ENERGY STORAGE (ES)

- *Microbatteries*

Microbatteries for energy storage processed on Si have to date achieved volumetric energy densities approaching 1 mWh/cm² with μm scale lithium-based thin film materials, offering capacity retention over thousands of cycles.²⁰ In the 2D, thin-film geometry, current deposition techniques and lithium ion diffusion limits the electrode thickness to several micrometers resulting in a battery dominated by the substrate and other inactive cell components. Silicon integrated microbatteries are typically solid-state utilizing vacuum deposited thin film electrodes and solid electrolytes. Solid-state materials offer advantages in terms of safety, cycle life and energy per electrode thickness. However, the ionic conductivity of the all solid-state electrolytes is usually orders of magnitude lower than the more common liquid based electrolytes of commercial lithium ion batteries (Figure MtM-7.f).

- *Microcapacitors*

Microcapacitors (Figure MtM-7.h) integrated on Si with monolithic ICs have been typically dedicated to RF, timing, filtering, or A/D conversion applications, which require small to moderate capacitance.²¹ More recently, great efforts have been dedicated to integrate the full power supply and thus microcapacitors on-die,²² in combination with a variety of Si-based energy harvesting devices, sensors and transmission circuitry—leading towards truly autonomous sensor systems. The main advantages of microcapacitors compared to other alternatives for micro-energy storage applications, namely microbatteries, electrolytic capacitors and supercapacitors, are their robustness of operation and ease of integration, stemming from the lack of need for an electrolyte. Another important advantage is the much higher voltage of operation than the mentioned alternatives due to much lower leakage currents. Furthermore, microcapacitors use materials that are environmentally and health friendly. Their main drawback so far is their limited value of capacitance density and, therefore, energy storage capability.²³

4.4.6. MICRO POWER MANAGEMENT (MPM):

In order to take advantage of energy transducers, it is essential to develop electronic circuits for converting power, storing energy, and distributing it to application circuits efficiently, consuming less than the available input power (Figure MtM-7.i). The design must tackle several trade-offs in achieving (i) the PM circuits bias the source in its maximum power point (MPP); (ii) high efficiency in power conversion across a wide range of input and output voltages; (iii) the lowest intrinsic power consumption; (iv) the ability to handle multiple type of ambient energies and convert to usable energy; (v) the ability to handle very low levels of ambient energies (1 μW), and (vi) inter-operability with other power consuming components within a device (e.g., sensors, microcontrollers, transceivers in an IoT device) to configure dynamically their operation mode for minimal power consumption whilst meeting the application requirement.

Typically the most critical FoM, which determine the low operating boundaries, are the intrinsic power consumption and the minimum input voltage, either during steady-state operation or during a cold start-up. Other FoMs include efficiency; minimum ambient energy usable; input and output voltage range; inter-operability (difficult to measure uniformly); switching frequency (to reduce the size of ancillary components), and the surface area of the whole converter circuit (including ancillaries, particularly the output inductor). Commercial discrete components allow cost-effective solutions with intrinsic consumptions down to 1 μA and input voltages down to few tens of mV.²⁴ CMOS implementations go

²⁰ Dudney, N. J. *Mat. Sci. Eng. B-Solid* 2005, 116, 245.

²¹ R. Ulrich and L. Schaper, "Materials options for dielectrics in integrated capacitors," in *Proc. Int. Symp. Adv. Packag. Mater., Process., Properties Inter.*, 2000, pp. 38–43.

²² M. Brunet and P. Kleimann, "High-density 3-D capacitors for power systems on-chip: Evaluation of a technology based on silicon submicrometer pore arrays formed by electrochemical etching," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4440–4448, 2013.

²³ M. Burke, A. Blake, V. Djara, D. O'Connell, I. M. Povey, K. Cherkaoui, S. Monaghan, J. Scully, R. Murphy, P. K. Hurley, M. E. Pemble, and A. J. Quinn, "High aspect ratio iridescent three-dimensional metal-insulator-metal capacitors using atomic layer deposition," *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, vol. 33, no. 1, p. 01A103, 2015.

²⁴ S. Boisseau, P. Gasnier, M. Gallardo, G. Despesse, "Self-starting power management circuits for piezoelectric and electret-based electrostatic mechanical energy harvesters," in: *J. Phys. Conf. Ser.*, IOP Publishing, 2013: p. 012080. doi:10.1088/1742-6596/476/1/012080; A. Camarda, A. Romani, E. Macrelli, and M. Tartagni, "A 32 mV/69 mV input voltage booster based on a piezoelectric transformer for energy harvesting applications," *Sensors Actuators A Phys.*, vol. 232, pp. 341–352, May 2015.

further and achieve from hundreds nW²⁵ down to few nW.²⁶ Another useful FoM is the overall volume of the micro-power management system, which may be negatively affected by the present of magnetic components or energy storage capacitors.

Table MtM-3 Energy Harvesting Difficult Challenges

Difficult Challenges 2019-2025	Potential solutions/where the efforts should be focalized or objectives
<p>Mechanical EH In general—(a) Increase input bandwidth, reduce working frequency for portable applications, adaptable devices. (b) Improve efficiency and power with a reduced surface and volume.</p> <p>Electrostatic (ES): (a) Improve scalable technologies at low cost/related to efficiency. (b) Increase reliability of integrated systems/stability vs. time/keep polarization and charges >10 years. Increase performance of electret materials (charges leakage reduction). Increase of the surface electrical potential with an appropriate electret. (c) Develop low-cost solutions and flexible approach to conform body. (d) Develop triboelectricity.</p> <p>Piezoelectric (PZ): (a) Increase performance of piezoelectric materials. (b) Bio-compatibility. (c) Low temperature integration, reduction of process temperature without affecting global performance.</p> <p>Electromagnetic (EM): (a) Development of CMOS compatible, high-performance micro/nano-magnets for MEMS/NEMS-scale integration (b) Development of low-loss, multi-turn micro-coil fabrication method (c) Robust mechanical structure to sustain large amplitude vibrations—reliability (d) Magnet-coil interaction—the most important factor to improve the electromagnetic coupling per unit volume vis-à-vis the output voltage/power (e) CMOS compatible permanent magnets for MEMS application</p>	<p>In general—(a) Exploit non-linear mechanical systems for larger frequency bandwidth, multiple nonlinearities in a single system, addressing the multi-stability issue, use frequency-up converting. (b) For each concept—ES: New materials: Fluorin polymers/surface texturation. PZ: Develop packaging (vacuum), integrate higher density seismic masses. EM: Integration approaches of permanent magnets and coils. For all concepts, if the mechanical stroke is limited by device dimensions, exploit alternative solutions to the conventional impedance-matching condition.²⁷</p> <p>Electrostatic: (a) Higher energy density (b) Develop stable layers with time (polymers) (c) Optimized polymers (d) Fluorin polymers/surface texturation</p> <p>Piezoelectric: (a) Porous materials (b) Piezo-electret, composites without lead (c) Composites, Piezo-electret</p> <p>Electromagnetic: (a) Thick, polymer bonded powdered permanent magnets; nano-structured, high energy product patterned magnet development (b) Improving the packing density, aspect ratio, number of turns (c) Polymer/flexible substrate; alternative spring structures; vacuum packaging to reduce mechanical losses (d) Optimized patterned magnets to improve the EM coupling (e) Looking beyond rare-earth free magnets—multi-nano-layers</p>

²⁵ M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A Nano-Current Power Management IC for Low Voltage Energy Harvesting," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4292–4304, 2015.

²⁶ Jung, S. Oh, S. Bang, Y. Lee, D. Sylvester, and D. Blaauw, "A 3nW fully integrated energy harvester based on self-oscillating switched-capacitor DC-DC converter," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 398–399.

²⁷ Hiroshi Toshiyoshi, Suna Ju, Hiroaki Honma, Chang-Hyeon Ji, and Hiroyuki Fujita, "MEMS vibrational energy harvesters," *Sci. Techno. Adv. Mater.*, vol. 20, no. 1, 2019, pp. 124-143. <https://doi.org/10.1080/14686996.2019.1569828>

<p>Thermal EH (a) Improve efficiency of thermal to electricity transformation near room temperature (<400 K). Maintain the thermal gradient on thin devices / reduce size of heat sink. Develop alternatives to Seebeck approaches. (b) Develop new materials and “green” solutions (use of non-toxic, environment-friendly materials) without Bi₂Te₃, for near-room temperature use cases (<400 K) and improved efficiency. (c) Develop scalable technologies at low cost. (d) Reduce the size of the “bulky systems” integrated with heat sink. (e) Add multifunctionality such as flexibility, combined energy storage capability and optoelectronic properties.</p>	<p>(a) ZT>2.5. Control of electronic and phononic transport on the basis of crystal and nanostructure engineering.²⁸ Suppressing lattice thermal conductivity. Possible alternative approaches: (i) Emerging spintronics via novel mechanisms such as the anomalous Nernst effect and magnon drag²⁹ (ii) New electrochemical thermal cells (iii) New thermoionic/thermophoretic cells³⁰ (b) Nanostructured materials / SiGe based solutions (c) SiGe based solutions (bulk & thin films) (d) Thermal engineering at product level (e) Use of organic and carbon-based conductors³¹</p>
<p>PV EH Improve PV (photovoltaic) cell output power density for (a) indoor and (b) outdoor applications. (c) Develop flexible, stable, high power conversion efficiency and low cost PV cells. Develop high efficiency and low cost transparent photovoltaic.³² (d) Increase the efficiency and reduce the cost of PV cells for energy harvesting applications. When needed (perovskite...), improve stability and lifetime of the solar cell. (e) Optimize the structure of the solar cell for Indoor and/or outdoor applications.</p>	<p>(a) Organic, DSSC (dye sensitized solar cells), semiconductors compounds (III-V, CdTe,...), a-Si, Perovskite (b) Si solar cells, tandem cells on Si, semiconductors compounds (CdTe, CIGS...), DSSC, Organic (c) Thin-film PV cells (III-V, organic, DSSC...) (d) Commercialized organic and inorganic (III-V compounds, DSSC...) for indoor and outdoor applications with improved efficiency and low cost</p>
<p>RF EH/Wireless power transfer (a) i) Transmitter side—Combining beam-forming and signal design to provide directive power transmission. ii) Receiver side—compact antenna solution. (b) Devices for rectifying the RF sources main requirements—high dynamic range, compact receiving antenna solutions. (c) Characterization of non- conventional materials for the rectenna design. (d) Integrated design of the antenna and rectifier for large dynamic range. (e) Design of dedicated signals for enhancing the power transfer.</p>	<p>(a) Exploitation of the signal theory to enhance the link efficiency at ultra-low RF received power levels (under 1 μW) (b) New rectifier topologies based on CMOS technologies rather than on discrete components (c) Wearable solutions for e-health monitoring based on flexible antenna (d) Development of auto-adjusting solutions by sensing the received RF power and exploiting the self-bias mechanism of ultra-low power transistor (e) Proof-of-concept demonstrators of dynamically varying power transmission</p>

²⁸ R. Anufriev, M. Nomura, "Phonon and heat transport control using pillar-based phononic crystals", *Sci. Technol. Adv. Mater.* 19, 863 (2018). <https://doi.org/10.1080/14686996.2018.1542524>.

H. Hori, J. Shiomi, "Tuning phonon transport spectrum for better thermoelectric materials", *Sci. Technol. Adv. Mater.* 20, 10 (2019). <https://doi.org/10.1080/14686996.2018.1548884>.

²⁹ M. Mizuguchi, S. Nakatsuji "Energy-harvesting materials based on the anomalous Nernst effect", *Sci. Technol. Adv. Mater.* 20, 262 (2019). <https://doi.org/10.1080/14686996.2019.1585143>.

³⁰ *Nature Materials*, 18, 608-613 (2019).

³¹ Y. Nonoguchi, A. Takata, C. Goto, T. Kawai, "Thickness-dependent thermoelectric power factor of polymer-functionalized semiconducting carbon nanotube thin films", *Sci. Technol. Adv. Mater.* 19, 581 (2018). <https://doi.org/10.1080/14686996.2018.1500851>.

³² C.J. Traverse et al, *Emergency of highly transparent photovoltaics for distributed applications*, *Nature Energy*, vol. 2 849-860 (2017).

<p>Energy storage</p> <p><u>Microbatteries:</u></p> <p>(a) Improve capacity with a reduced surface area and volume.</p> <p>(b) Increase power capability for portable applications, adaptable devices.</p> <p>(c) Increase performance of electrode and electrolyte materials.</p> <p>(d) Processing on low cost substrates.</p> <p>(e) Patterning active materials.</p> <p>(f) Low temperature integration, reduction of process temperature without affecting global performance.</p> <p>(g) Packaging of microbattery device.</p> <p><u>Microcapacitors:</u></p> <p>(a) Improve capacitance density.</p> <p>(b) Reduction of leakage current.</p> <p>(c) Reduction of series resistance.</p> <p>(d) 3D structuring of the capacitor surface area.</p> <p>(e) Uniform high-k deposition.</p> <p>(f) Integration with on-chip harvesters.</p>	<p><u>Microbatteries:</u></p> <p>(a) Multilayer microbattery structure. Thick film materials deposition.</p> <p>(b) 3D structuring³³</p> <p>(c) Higher conductivity and energy density materials</p> <p>(d) 3D printing</p> <p>(e) Decrease waste</p> <p>(f) Processing improvements for integration on silicon</p> <p>(g) Advanced packaging for reliability</p> <p><u>Microcapacitors:</u></p> <p>(a) 3D structuring and use of known high-k materials (single layers or stack of them)</p> <p>(b) Use of optimized dielectric layers and other device materials</p> <p>(c) Thicker electrodes</p> <p>(d) Capacitance density 5- fold of that of the flat capacitor</p> <p>(e) Known high-k materials</p> <p>(f) Design</p>
<p><u>Micro power management</u></p> <p>(a) Achieve operation with ultra-low input voltage and power levels (minimization of self-consumption and trade-offs with efficiency).</p> <p>(b) Perform battery-less start-up from fully discharged state.</p> <p>(c) Are external passive required (C, L) or can the circuit be fully integrated? Overall size.</p> <p>(d) Type of maximum power point tracking and/or source impedance matching provided.</p> <p>(e) Reduce the power consumption of power management circuit.</p> <p>(f) Power management distributed at many levels.</p> <p>(g) Development of dedicated microelectronic process options and devices.</p> <p>(h) System integration and smart packaging.</p> <p>(i) Accept high input voltages on microelectronic implementations.</p> <p>(j) Ability to handle very low levels of ambient energies (down to 1μW at 10 s of mV).</p> <p>(k) "Multi-source" compatibility with multiple types of ambient energies.</p> <p>(l) inter-operability.</p> <p>(m) Switching frequency (make high to reduce size of external ancillary components (inductors and caps).</p>	<p>(a) Power conversion/management ICs operating with < 1 μW and starting with 50-100 mV</p> <p>(b) Fully integrated step-up converters based on low-V_{TH}/native MOSFETs down to 50 mV. Integrated step-up converters aided by external magnetic or piezoelectric transformers down to few mV.</p> <p>(c) More efficient fully integrated inductor-less switched-capacitor converters. Miniaturization of magnetic components.</p> <p>(d) FOCV or derived techniques for DC sources with more responsive MPPT. Cancellation of reactive components of source impedance in vibrational energy harvesters.</p> <p>(e) <1μW / 70% efficiency</p> <p>(f) Development of energy-aware circuit design techniques for power converters in the 1-100 nA range.</p> <p>(g) Improved availability of low-threshold/native/depletion MOSFETs for supporting energy harvesting from ultra-low voltage sources (tens of mV). Improved power switch performance (lower driving voltage, lower leakage, lower on-resistance).</p> <p>(h) cm-scale energy autonomous systems.</p> <p>(i) Implementations on BCD or CMOS-HV processes.</p> <p>(j) & (k) Innovative configurable PMIC circuits that can offer an ultra-wide input and output voltage range.</p> <p>(l) Application centric configurable PMIC solutions with built in digital interfacing capability.</p> <p>(m) Novel high efficiency, low loss switching topologies.</p>

³³ J.F. Rohan, M. Hasan, S. Patil, D. Casey and T. Clancy, Chapter 6 – Energy storage materials and architectures at the nanoscale, in *ICT-Energy - Nanoscale energy management concepts towards Zero-Power Information and Communication Technology / (2014)* Editors, G. Fagas, L. Gammaitoni, D. Paul and G. Abadal Berini, Intech Publications, Croatia. pp 107-138, ISBN 980-953-307-1005-8, DOI: 10.5772/57139.

Difficult Challenges 2025-2034	Potential solutions/where the efforts should be focalized or objectives
<p>Mechanical EH In general—(a) Increase input bandwidth, reduce working frequency for portable applications, adaptable devices. (b) Improve efficiency and power with a reduced surface and volume.</p> <p>Electrostatic (ES): (a) Increase reliability of integrated systems / stability vs. time / keep polarization and charges >10 years. Increase performance of electret materials (charges leakage reduction). Increase of the surface electrical potential with an appropriate electret. (b) Develop low cost solutions and flexible approach to conform body. (c) Develop triboelectricity.</p> <p>Piezoelectric (PZ): Increase performance of piezoelectric materials. Bio-compatibility. Low temperature integration, reduction of process temperature without affecting global performance.</p> <p>Electromagnetic (EM): (a) Development of CMOS compatible, high performance micro/nano-magnets for MEMS/NEMS-scale integration. (b) Development of low loss, multi turn micro-coil fabrication method. (c) Robust mechanical structure to sustain large amplitude vibrations—reliability. (d) Magnet-coil interaction—most important factor to improve the electromagnetic coupling per unit volume vis-à-vis the output voltage/power. (e) CMOS compatible permanent magnets for MEMS application</p>	<p>In general—(a) Frequency independent adaptable devices. (b) For each concept: ES: Fluorin polymers / surface texturation. PZ: Small scale hybrid devices. Work on mechanical properties (fatigue strength, elasticity...). EM: Developing high energy product integrated magnets; alternative hybrid transductions. For all concepts, if the mechanical stroke is limited by device dimensions, exploit alternative solutions to the conventional impedance-matching condition.</p> <p>Electrostatic: (a) Encapsulated SiO₂ / triboelectric materials (b) Low cost polymers (c) Low cost</p> <p>Piezoelectric: Nanotechnology, nanocomposites without lead</p> <p>Electromagnetic: (a) Thick, rare-earth free, nano-composite, exchange coupled (soft/hard) magnet integration (b) MEMS compatible alternative methods for fabricating coils (c) Alternative topologies incorporating nanowires/nanotubes (d) Suitable micro-coil topology with aligned magnet array to maximize the coupling (e) Super hard, nano-structured integratable magnets.</p>
<p>Thermal EH (a) Improve efficiency of thermal to electricity transformation near room temperature (<400 K). Maintain the thermal gradient on thin devices / reduce size of heat sink. Develop alternatives to Seebeck approaches. (b) Develop “green” solutions (use of non-toxic, environment-friendly materials) for near-room temperature use cases (<400 K), not based on Bi₂Te₃. (c) Develop scalable technologies at low cost. (d) Reduce the size of the “bulky systems” integrated with heat sink. (e) Develop new material for improved efficiency without Bi₂Te₃ near room temperature. (f) Add multifunctionality such as flexibility, combined energy storage capability and optoelectronic properties.</p>	<p>(a) ZT>3. Control of electronic and phononic transport on the basis of crystal and nanostructure engineering. Suppressing lattice thermal conductivity.</p> <p>Possible alternative approaches—(i) Emerging spintronics via novel mechanisms such as the anomalous Nernst effect and magnon drag. (ii) New electrochemical thermal cells.</p> <p>(b) Nanostructured materials/Si based solutions (c) Si based solutions (thin films) (d) High ZT material (e) Phonon engineering / Si based solutions (f) Use of organic and carbon-based conductors</p>

<p>PV EH Improve PV (photovoltaic) cell output power density for (a) indoor and (b) outdoor applications. (c) Develop flexible, stable, high power conversion efficiency and low cost PV cells. Develop high efficiency and low cost transparent photovoltaic. (d) Increase the efficiency and reduce the cost of PV cells for energy harvesting applications. When needed (perovskite...), improve stability and lifetime of the solar cell. (e) Optimize the structure of the solar cell for Indoor and/or outdoor applications.</p>	<p>(a) Perovskite, Multi-junction PV cell, nanostructured materials... (b) Multi-junctions, nanostructured materials, quantum dots... (c) Thin-Film (perovskite...), multi-junctions, nanostructured... (d) Low cost PV cells with increased efficiency (III-V compounds, multijunction, nanostructured, thin film, perovskite...)</p>
<p>RF EH/Wireless power transfer (a) i) Transmitter side—Combining beam-forming and signal design to provide directive power transmission. ii) Receiver side—compact antenna solution. (b) Devices for rectifying the RF sources main requirements—high dynamic range, compact receiving antenna solutions. (c) Characterization of non- conventional materials for the rectenna design. (d) Integrated design of the antenna and rectifier for large dynamic range. (e) Design of dedicated signals for enhancing the power transfer.</p>	<p>(a) mm-wave reconfigurable RF sources and miniaturized power receivers (b) Miniature systems integrating the antenna and the rectifier circuit in CMOS technology with RF-to-DC efficiency comparable with Schottky-diode based topologies (c) Implanted miniaturized rectennas (d) High dynamic range rectennas (e) Power shaping sources adjustable in realtime</p>
<p>Energy storage <u>Microbatteries:</u> (a) Improve capacity with a reduced surface area and volume. (b) Increase power capability for portable applications, adaptable devices. (c) Increase performance of electrode and electrolyte materials. (d) Processing on low cost substrates. (e) Patterning active materials. (f) Low temperature integration, reduction of process temperature without affecting global performance. (g) Packaging of microbattery device. <u>Microcapacitors:</u> (a) Improve capacitance density (b) Reduction of leakage current (c) Reduction of series resistance (d) 3D structuring of the capacitor surface area (e) Uniform high-k deposition (f) Integration with on-chip harvesters</p>	<p><u>Microbatteries—</u> (a) New lithium based electrode and electrolyte materials Multivalent electrode systems (b) With new materials (c) Interface engineering for optimized performance (d) High density materials. Nonvolatile electrolytes (e) Increase loading for higher capacity (f) On flexible substrates (g) Low cost <u>Microcapacitors—</u> (a) 3D structuring in combination with new materials and device geometries (b) New materials (c) Higher conductivity materials (d) Capacitance density 10-fold of that of the flat capacitor (e) New materials not yet used in this application (f) Implementation</p>

<p>Micro power management</p> <p>(a) Achieve operation with ultra-low input voltage and power levels (minimization of self-consumption and trade-offs with efficiency).</p> <p>(b) Perform battery-less start-up from fully discharged state.</p> <p>(c) Are external passive required (C, L) or can the circuit be fully integrated/embedded? Overall size.</p> <p>(d) Type of maximum power point tracking and/or source impedance matching provided.</p> <p>(e) Reduce the power consumption of power management circuit.</p> <p>(f) Power management distributed at many levels.</p> <p>(g) Development of dedicated microelectronic process options and devices.</p> <p>(h) System integration and smart packaging.</p> <p>(i) Accept high input voltages on microelectronic implementations..</p> <p>(j) Use very low ambient energies sub uW.</p> <p>(k) Achieve good efficiency at sub uW level.</p> <p>(l) Simulation models inter-operable with other components and devices to predict system level performance.</p>	<p>(a) Integrated SoC or SiP embedding power conversion/management and their specific functions operating in the 10-100 nW range</p> <p>(b) Miniature systems with embedded micro-transformers (magnetic or piezoelectric) at package level starting from few mV</p> <p>(c) Development of alternatives of inductors for power conversion compatible with wafer-level processing, such as MEMS piezoelectric transformers</p> <p>Nanopower SoC and miniature passive + energy transducer integrated at package level (mm-scale systems)</p> <p>(d) More complex MPPT algorithms implemented on-chip with ultra-low consumption</p> <p>(e) <100 nW/80% efficiency</p> <p>(f) Energy-aware design of all system parts with reduced leakage, lower active currents, and harmonized energy management policies</p> <p>(g) Development of more efficient power switches with low control voltage and negligible leakage (microelectronic, or micromechanical alternatives)</p> <p>(h) mm-scale energy autonomous systems</p> <p>(j) & (k) Innovative power topologies</p> <p>(l) Standardized an inter-operable models for all EH, ES, MPM solutions</p>
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4.5. RECOMMENDATIONS

Concerning the concepts covered in this white paper (vibrational, solar, thermal, RF EH and power management), the improvement of their performance and efficiency is as important as the development of “green” materials, replacing toxic/rare materials used nowadays (lead-based piezoelectrics, Bi₂Te₃ for thermoelectrics, rare earth-based magnetic material, e.g., NdFeB, for electromagnetic conversion). Flexible and low-cost approaches for wearable applications should be developed as well. Increasing the bandwidth at a low frequency target (below 100 Hz) will help to fit applications for vibration-based mechanical energy harvesters. Utilizing spin in thermoelectric EHs and other energy conversion systems is the promising and challenging idea. Concerning indoor photovoltaic applications, adapted structures and materials (light intensity and spectra, etc.) should be developed; on the other hand, standard procedures for indoor photovoltaic cells characterization should be defined (light intensity and spectra, direct and diffuse light, temperature, etc.). Intentional far-field RF WPT will exploit the mm-wave band for enhancing rectenna miniaturization and focusing of the energy transfer. Energy storage is required as a hybrid device with the EH options to alleviate any transient effects and assist with higher power operation. There is a need of innovative power management circuits, such as: topologies, impedance matching, cold start, dynamic configuration, storage device interface, etc. It would be key to investigate size reduction of inductors; enhance the efficiency of inductor-less power converter circuit topologies; develop planar alternative to inductors, and tune microelectronic process parameters and technologies to reduce leakage for reduced power consumption and allowing low input voltages. Finally, the comprehensive system design combining all aspects of the fabrication process, harvester structure, power conversion circuits and storage will be the potential solution for increasing the power generation efficiency. To optimize system-level performance, there is a need of collaborative development between all the stakeholders (developers of EH, ES, MPM solutions) to co-develop models, specifications, platforms, etc.³⁴ They in turn need to agree on common specifications and methodologies for defining parts to ensure standardization, inter-operability and system level performance optimizations.

4.6. SUMMARY

Providing energetic autonomy to electronic devices will be a key factor in booming technologies like sensor networks and IoTs. Various neglected energy sources can be exploited and converted into electricity, such as: sun or artificial light, heat, RF power, mechanical movements and vibrations. Power management circuits and energy storage devices are essential to use this energy and transfer it to sensors, microcontrollers or other electronic components included in autonomous devices.

The energy that can be generated from small EH devices is quite low with most of these technologies, but this could be sufficient for many sensing applications, given the fact that energy is in general randomly generated. In addition, research

³⁴ www.enables-project.eu.

is progressing towards the development of micro-power architectures of application circuits. The evolution of the EH technologies will enable a growing number of possible applications and products to be placed on the market, which were unfeasible up to now. This white paper covers several promising technologies for EH (mechanical, thermal, photovoltaic and RF energy harvesting), power management circuits and energy storage devices (microbatteries and microcapacitors). Their most difficult challenges have been assessed in the medium (2019-2025) and long term (2025-2034) altogether with potential solutions.

5. WEARABLE, FLEXIBLE AND PRINTED ELECTRONICS

5.1. INTRODUCTION

Moore's prediction that the number of transistors per chip would double every 18 months is reaching its physical limits. While the miniaturization of crystalline silicon-based electronic structures has been instrumental to create a huge number of electronic and affordable devices, there are applications where crystalline silicon-based electronics is less competitive with other technologies. One of these applications is flexible and wearable electronics.

The field of the flexible, printed and organic electronics has progressed enormously in the last 10-15 years. It is expected that the printed electronics industry will grow to over \$ 300 billion in 2027 (IDTechEx). Printed and flexible electronic devices and circuits must have much more complex capabilities. Also optoelectronic devices such as light emitting organic devices and organic solar cells have a rapid growth in the clean energy market and are expected to play an important role in the near future in markets such as textiles buildings, notebook computers, transport, health and at home, among others.

Printed electronics is one of the most promising fields of flexible electronics. It is based on creating electronic devices by printing on a variety of substrates. Inks for printed electronics are usually made of carbon-based compounds. Inkjet printed electronics has progressed very fast during the last years and nowadays inkjet printers are capable of printing electrical circuits very quickly and inexpensively. Printed electronics is already being used to make flexible keyboards, antennas, flexible screens, interactive books and posters, electronic skin patches and more. A high number of printed electronics products are already available in the market. Progress in printed electronics is also reflected in smart packaging, ranging from RFID labels to RFID sensing labels. The market for printed electronics is growing because the Internet of Things is expanding and requires low-cost, lightweight technology that can sense, store information securely, and transmit data.

A number of materials may be more adequate for flexible and wearable electronics than silicon, whether used in combination with silicon or not. The more promising of these alternative materials are the organic and oxide materials. In particular, the combination of organic and inorganic materials with printing technologies allows thin, lightweight and very cost-efficient electronic systems.

Current market drivers are organic photovoltaics, flexible batteries, electro-optic devices, displays, logic and memory components—including thin film transistors (TFTs), sensor arrays, and radio frequency identification (RFID) tags.

Another promising field is hybrid electronics, which combines the flexibility and thinness of large-area electronics with the high processing power of crystalline semiconductors, opening a broad range of new applications in areas such as the IoT, healthcare, smart buildings, automotive, and packaging. The flexible hybrid electronics market was valued at USD 82 million in 2018 and is expected to reach USD 198.9 million by 2024, with a CAGR of 16.2% over the forecast period of 2019-2024.

There is the aim of integrating flexible components into their conventional and rigid (including crystalline) counterparts. However, there are several challenges that have to be overcome to achieve this goal. Also, although significant performances has already been achieved by devices based on oxide and organic materials, more research is still needed to further improve their electrical characteristics, increase mobility values and threshold voltage stability, reduce bias and light stress instability, and reduce the voltage operating range.

5.2. SCOPE

Due to unique properties—such as light weight, low cost, stretchability, and wearability—flexible electronics is especially suitable for the development of personalized wearable devices.

Flexible and wearable electronics systems promise to achieve full independence of off grid energy. Besides, such systems can have lower power consumption. Flexible and stretchable electronics is also needed in devices monitoring patients' health with electronic assistance from their homes. Conformal skin patches have already become a billion-dollar industry.

Experts predict a huge growth for the flexible electronics market, especially considering the increasing applications in consumer electronics, automotive, healthcare, military, biometrics, and other industries. The flexible electronics market is expected to increase even more considerably from the recent progress in the printed and wearable technology.

Another important application area of flexible electronics is paper electronics and, in general, biodegradable substrates. The proliferation of computers and personal electronics has not led to the significantly decrease in product lifespan and faster obsolescence. As a result, a global concern on the management of the increased electronic waste (e-waste) has arisen, in the sense that is both difficult to recycle and incorporate many different environmental contaminants. Due to the emergence of the IoT, it is predicted that by 2025 internet nodes may reside in furniture and paper documents. In order to address the growing concerns of e-waste, such devices need to be developed in fully biodegradable substrates, sensors and actuators. A very suitable candidate for a biodegradable substrate is of course paper. Paper as a substrate is already widely used for different printing methods, as substrate for decor applications, as a packaging material or as a functional material in automotive applications. A big advantage of paper as a substrate for printed electronics is its origin from natural and above all renewable fiber sources such as cellulose, linters, or other similar natural fiber.

The combination of flexible electronic devices with novel micro/nanostructured materials will have a huge impact in many practical applications, such as health monitoring, robotics, smart displays, and energy harvesting and storage.

In the near future, a disruptive combination of three technological areas—microelectronics, chemistry and printing—is expected to create markets with annual revenues estimated at more than 200 billion.

5.3. STAKEHOLDERS

There are many existing and potential stakeholders in flexible electronics in both industry and the research sector. Companies working in the sectors where flexible electronics is expanding or expected to expand are of course stakeholders in this technology—companies in the fields of smart displays, healthcare, robotics, smart packages, intelligent labels, biometrics, smart textiles, automotive, defense and others.

Many companies in the display sector are fabricating commercial OLED devices. In particular, Samsung, LG and Sony are frontline contributors in this area. They intend to produce flexible and stretchable devices completely based on OLEDs.

Samsung also started the fabrication of commercial displays based on IGZO TFTs, being the first company to use oxide TFTs in commercial products. Samsung is the present leader in printed electronics. In September 2019 Samsung launched Galaxy Fold, a foldable display smartphone. In May 2019 LG exhibited the world's first rollable OLED TV. It is considered the display of the future.

Other key players in the flexible and printed electronics market include Palo Alto Research Center Incorporated (PARC), Agfa-Gevaert Group, Molex LLC, Solicore, Planar Energy Devices, 3M, E-Ink Holdings, Panasonic Corporation, AU Optronics, Blue Spark Technologies, Cymbet, Royole Corporation, Enfucell, GE Measurement & Control Solutions, ITN Energy Systems, Thinfilm Electronics ASA, BASF, DuPont, Merck, ALTANA, Fujifilm Dimatix, and Solar Frontier.

In Europe, the major players are the German companies BASF, Merck, ALTANA and Solar Frontier, and the Finnish company Enfucell.

A number of projects have been funded by national and European agencies to promote research and innovation in flexible electronics. Some of these projects have been especially industrial oriented. For example, the InSCOPE project, a collaboration by Bosch, Signify, KONE and CSK, focused on printed electronics applications in automotive, smart building and medical packages.³⁵ Another example of recent project is SmartEEs, executed by a consortium consisting of UNITRON, Small Data Garden, Esyst and 3DMA, which focused on the health, packaging/logistics and building sectors.³⁶

Many research and innovation centers are also actively working in the development of new and improved flexible technologies for future industrial exploitation. Examples are VTT (Finland) IMEC (Belgium), Fraunhofer Institute (Germany), Max Planck Institute (Germany), CEA-LITEN (France), Joanneum Center (Austria), TU-Dresden (Germany), UNL (Portugal), and CNR (Italy), among others.

³⁵ <https://inscope-project.eu/>.

³⁶ <https://smarte.es/>.

5.4. TECHNOLOGY STATUS, REQUIREMENTS AND POTENTIAL SOLUTIONS

Research efforts are focused on improve the performance and stability of devices suitable for flexible electronics, such as oxide- and organic-based devices. Many of these devices still are early-stage prototypes. There are important scientific and engineering challenges to be overcome before these prototypes can become products suitable to be put in the market. However, some devices are already used in the fabrication of commercial products. For example, both small molecules and polymers are being used to manufacture OLED displays (TV and mobile phone displays). IGZO materials are also used in commercial TFT displays. Indeed, many companies around the world have been manufacturing OLED devices in recent years.

There are still important technological challenges to surmount for a more widespread extension of flexible electronics in the coming years. Several solutions have been suggested. In Table MtM-4 the main difficult challenges for the period 2019-2025 as well as potential solutions have been listed.

Table MtM-4 Wearable, Flexible and Printed Electronics Difficult Challenges

Difficult Challenges 2019-2025	Potential Solutions
<i>Manufacturing of integrated circuits on plastic or other flexible substrates that do not withstand the high temperature conditions of silicon-based device manufacture.</i>	Organic and oxide TFTs Carbon-based TFTs including carbon-nanotube and graphene
<i>Combination of different manufacturing technologies to integrate flexible electronics into traditional products.</i>	High mobility TFTs, complementary circuits, new and improved inks, high resolution printing process
<i>Reduction of ink costs.</i>	Inks with specific optimized properties (such as semiconducting, dielectric, higher conductivity, rheology, adhesion,...); for example silver or other metallic components based inks, need to be developed for printed electronics applications as affordable solutions. Silver or other metallic components based inks seem promising.
<i>Improved environmental stability to enable operation in more robust environments and to reduce barrier requirements.</i>	Excellent stability of p-type organic and n-type metal-oxide TFTs (compared to e.g., n-type organic TFTs) in complementary circuits
<i>Complementary TFT circuits difficult because of imbalanced charge transport, high driving voltage and process incompatibilities.</i>	Controlled doping to balance the charge transport for complementary circuits. This approach can be combined with dedicated circuit design and the development of advanced patterning techniques such as high-resolution printing. This can allow TFTs with reduced parasitic capacitances, high transconductance, and low driving voltage (<15V). High-k dielectrics have also shown to reduce the voltage operating range and increase the mobility—reported mobilities as high as 80 cm ² /(V s). Recently, HIZO TFTs fabricated with a mobility of 150 cm ² /(V s). In 2020 mobilities as high as 100 cm ² /(V s) are foreseen in organic TFTs.
<i>Increase of electron mobility in organic materials; this could be instrumental for a complementary organic circuit.</i>	New poly(benzothiadiazole-naphthalenediimide) derivatives and fine-tuning the material's backbone conformation. This can be possible by the introduction of vinylene bridges capable of forming hydrogen bonds with neighboring fluorine and oxygen atoms. Introducing these vinylene bridges required a technical feat so as to optimize the reaction conditions.
<i>Large TFT device variabilities, which can be due to non-uniform thicknesses of the materials, variability in the size of the devices during fabrication or inhomogeneities within the thin film materials leading to variable mobilities.</i>	Circuit design for device performance compensation Dynamic performance (V_{th} , etc.) control using top-gate or floating-gate structure
<i>For printed electronics, combination of materials with high uniformity and high mobility in industrial quantities with high reproducible quality.</i>	Inks (perhaps metal-oxide precursor ones) for printed high mobility TFTs with controlled doping allowing for an improved uniformity and higher device-to-device reliability of the threshold voltage (V_T).

<i>Overcome the lack of self-assembly in organic materials. Improve controlled self-assembly. Gain better control over the self-assembly of organic electronic molecules into ordered patterns to ensure that the structures being assembled are reproducible. This requires a better understanding of the electronic properties of organic materials, especially when those materials are in contact with other materials (i.e., their interfacial behavior).</i>	Material design for self-assembled molecules.
<i>Improve 3D processing technology to achieve a precision comparable to 2D printing technologies. Many organic electronic structures can be assembled on flexible substrates using existing printing technologies. However, fabrication of 3D organic electronic structures with the same precision achievable with 2D printing technology remains a major challenge to reliable high throughput manufacturing of organic electronic devices. However, defect-free 3D processing of organic electronic structures remains a major challenge to industry-scale manufacture.</i>	Engineers need to build on what has already been done with 2D lithography so that they can fabricate uniform 3D structures in a controlled manner on a nano-level.
<i>Improvement of roll-to-roll processing. Although it is an ideal, fast and low-cost technology is very much restricted by the substrates. In the case of stretchable devices, during the roll to roll processing, materials may be deformed, which would cause huge problems in roll to roll processing. Multi-layer making with roll-to-roll is prone to high mismatch.</i>	
<i>Paper as a substrate for electronics responding to renewable and recyclability criteria. It is predicted that by 2025, internet nodes may reside in furniture and paper documents. In order to address the growing concerns of e-waste, such devices need to be developed in fully biodegradable substrates, sensors and actuators.</i>	Smooth, nanoscale porosity and flexible composite structures on the bases of cellulose nano-fibrils (CNF). Simultaneous production of multiple controllable microporous structure by foam forming. Specifically designed coating layers for high quality graphics.
<i>High thermal stability needed in biomedical devices; otherwise they will not survive high-heat sterilization.</i>	High thermal stability achieved in several TFT types, including organic ones.
<i>Increase of efficiency in OLEDs</i>	Double-doped polymers.
<i>Expanding solar cell production is industry-scale reproducibility</i>	Increase of the efficiency. 20% is foreseen. . This increased performance would be driven by newly developed polymers with improved solar light absorption properties and superior mobilities.
<i>Improvement of environmental stability of organic electronic materials for products. This requires an improved environmental stability, water vapor transmission rates $< 10^{-6} \text{ gm}^{-2} \text{ d}^{-1}$ at 20°C/50% RH and oxygen transmission rates $< 10^{-6} \text{ cm}^3 \text{ m}^{-2} \text{ d}^{-1} \text{ bar}^{-1}$.</i>	Organic and inorganic multilayer encapsulation.
<i>Flexible crystal semiconductor electronics</i>	Deposition or transfer of 1D and 2D semiconductor materials on flexible substrates. This is not difficult for 1D materials, but 2D materials can rupture due to their mechanical properties.
<i>Manufacturing of CMOS systems with acceptable costs and reliability</i>	Non-planar coin-like 3D architecture with some components are placed in the outer sides of both planes, and other elements remain in the middle which are also physically flexible.
<i>Flexible crystalline solar cells</i>	A corrugation structure-based flexible crystalline solar cell with 19% efficiency fabricated.
<i>Microwave flexible electronics</i>	Substrates with high thermal conductivity. Single crystalline nanomembranes to implement high frequency flexible transistors due to their transferability, scalability, and relatively low cost. The frequency figure of merit of nanomembrane-based flexible transistors has already reached 100 GHz.

5.5. RECOMMENDATIONS

Technological improvements are needed in order to increase mobility values and threshold voltage stability in TFTs—reducing the voltage operating range, reducing bias and light stress instability, and reducing the voltage operating range. High-k dielectrics are helpful to reduce the bias operating range. A suitable complementary TFT technology is still a challenge, but can be achieved by using an n-type oxide TFT and a p-type organic TFT. Another possible solution is the control of doping to balance charge transport in complementary circuits.

For biomedical devices, high thermal stability is essential. This is possible in flexible electronics. Indeed, several TFT technologies (including organic ones) already show high thermal stability.

On the other hand, further progress in printed electronics needs better inks in order to achieve higher mobility TFTs with improved uniformity and reliability. A reduction of the costs of inks would also help in the extension of printed electronics applications.

Regarding the growing concerns of e-waste, it is recommended to develop devices in fully biodegradable substrates. Paper as a substrate is a very promising choice.

Other important challenges to be surmounted in organic electronics are the improvement of roll-to-roll processing (which is very much restricted by the substrates) and the improvement of environmental stability, which can be achieved by encapsulation.

Besides, there is still a need for the development of 3D printing electronics with the same precision as 2D printing technology. 3D printing flexible electronics is especially useful in the healthcare sector, where 3D printers can be used for direct printing of biomedical devices onto human skin and can facilitate the manufacturing of flexible electronic sensors of body pressure. 3D printed flexible electronics has also applications in the field of prosthetic organs for the disabled.

Regarding OLEDs, double-doped polymers can lead to an increase of efficiency.

Concerning the extension of organic photovoltaics (OPVs) technologies, efficiency needs to be improved. A 20% efficiency is foreseen, thanks to newly developed polymers with improved solar light absorption and higher mobilities. Also, flexible crystalline organic cells with 19% efficiency have been developed.

Finally, microwave flexible electronics is still a major challenge. It may be surmounted with substrates with high thermal conductivity or single crystalline nanomembranes.

5.6. SUMMARY

Flexible electronics has experienced an enormous growth in the last years and is expected to be used in an increasing number of products as the technology continues to advance. As substrates become thinner, devices become thin, light, and flexible. A higher increase of flexible electronics applications is foreseen in the coming years due to the expansion of the Internet of Things, which requires low-cost, lightweight and flexible and wearable technologies. The market of flexible and printed electronics and is expected to reach over \$73 billion by 2025.

Components used or to be used in flexible electronics, such as TFTs, OLEDs and OPVs have considerably improved their performances in the last years. However, further expansion of flexible electronics needs to surmount several technological challenges, including improvements in mobility, environmental stability, bias and light stress reduction, thermal conductivity, biodegradable substrates, and incorporation in crystalline and rigid electronics. Several solutions to overcome these challenges have been proposed, and the performance improvements are expected to continue in the coming years.

6. GLOSSARY/ABBREVIATIONS

Acronym/Abbreviation	Definition
Smart Sensors Acronyms	
ADAS	advanced drive assistance system
CCD	charged coupled device
GHG	greenhouse gases
HDR	high dynamic range
IMU	inertial measurement unit
LiDAR	light detection and ranging
MEA	microelectrode array
PM2.5	particulate matter <2.5 μm
PM10	particulate matter 2.5 – 10 μm
VOC	volatile organic compound
Smart Energy Acronyms	
2DEG	two dimensional electron gas
AI	artificial intelligence
AlN	aluminum nitride
BCD	bipolar, CMOS, DMOS
CL	cathodoluminescence
CMP	chemical mechanical polishing
DMOS	double diffused metal oxide semiconductor
EV	electrical vehicle
FinFET	fin field effect transistor
FoM	figure of merit
FWD	freewheeling diode
GaN	gallium nitride
GW	gigawatt
HEMT	high electron mobility transistor
HV	high voltage
IGBT	insulated gate bipolar transistor
ME	multi-epi
MI	multi-implant
MOS	metal oxide semiconductor
R_{on}	on resistance
Si	silicon
SiC	silicon carbide
SJ	super-junction
SoI	silicon on insulator
UID	unintentional doping
WBS	Wide bandgap semiconductor
Energy Harvesting Acronyms	
EH	energy harvesting
ES	energy storage
MPM	micro power management
FoM	figure of merit
IoT	internet of things
PV	photovoltaic
RF	radio frequency
RFID	radio frequency identification

TE	thermoelectric
ZT	dimensionless parameter used in thermal EH defined by $ZT = \sigma S^2 T / \lambda$, with σ the electrical conductivity, S the Seebeck coefficient, λ the thermal conductivity and T the temperature
Wearable, Flexible And Printed Electronics Acronyms	
HIZO-TFT	Hf-In-Zn-O thin film transistor
CNF	cellulose nano-fibrils
OLED	organic light emitting diode
OPV	organic photovoltaics
RFID	radio frequency identification
TFT	thin film transistor