INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

2018 UPDATE

CRYOGENIC ELECTRONICS AND QUANTUM INFORMATION PROCESSING

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CRYOGENIC ELECTRONICS AND QUANTUM INFORMATION PROCESSING

1. INTRODUCTION

The goal of this International Roadmap for Devices and Systems (IRDS) chapter is to survey, catalog, and assess the status of technologies in the areas of cryogenic electronics and quantum information processing. Application drivers are identified for sufficiently developed technologies and application needs are mapped as a function of time against projected capabilities to identify challenges requiring research and development effort.

Cryogenic electronics (also referred to as low-temperature electronics or cold electronics) is defined by operation at cryogenic temperatures (below −150 °C or 123.15 K) and includes devices and circuits made from a variety of materials including insulators, conductors, semiconductors, superconductors, or topological materials. Existing and emerging applications are driving development of novel cryogenic electronic technologies.

Information processing refers to the input, transmission, storage, manipulation or processing, and output of data. Information processing systems to accomplish a specific function, in general, require several different interactive layers of technology. A top-down list of these layers begins with the required application or system function, leading to system architecture, micro- or nano-architecture, circuits, devices, and materials. A fundamental unit of information (e.g., a bit) is represented by a computational state variable, for example, the position of a bead in the ancient abacus calculator or the voltage (or charge) state of a node capacitance in CMOS logic. A binary computational state variable serves as the foundation for von Neumann computational system architectures that dominated conventional computing.

Quantum information processing is different in that it uses qubits, two-state quantum-mechanical systems that can be in coherent superpositions of both states at the same time, which can have computational advantages. Measurement of a qubit in a given basis causes it to collapse to one of the basis states.

Technology categories covered in this report include:

- Superconductor electronics (SCE)
- Cryogenic semiconductor electronics (Cryo-Semi)
- Quantum information processing (QIP)

Note: In 2018, Cryogenic Electronics and Quantum Information Processing became an International Focus Team (IFT) responsible for preparing a separate IRDS chapter. In 2017, Cryogenic Electronics appeared as an emerging application within the Beyond CMOS chapter.

2. SUPERCONDUCTOR ELECTRONICS (SCE)

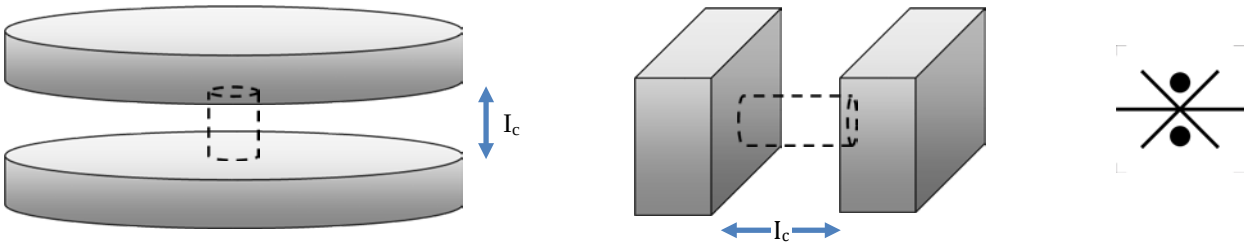
2.1. INTRODUCTION

Superconductor electronics (SCE) uses circuits and components at least some of which are in the superconducting state. Some materials become superconducting below a critical temperature, T_c. Critical temperatures of known superconductors range from near absolute zero to about 203 K (–70 °C). The unique physics of superconductors, such as zero dc resistance for sufficiently small currents, allows construction of circuits that are otherwise difficult or impossible to realize. SCE applications tend to cluster in temperatures around the boiling point of liquid nitrogen (77 K, –196 °C), the boiling point of liquid helium (4.2 K, –269 °C), and the superfluid helium-4 temperature range below about 2.17 K.

This report does not seek to explain the operation of superconductor electronic components or circuits except where necessary and consequential to technology roadmapping. Similarly, the focus is on applications that could benefit from technology roadmapping. Following is a very brief introduction. For those seeking to fill in the gaps, a recent and open access review of superconductor electronics is a good next step [1].

Both passive (linear) and active (nonlinear) superconducting components exist. Examples of passive components are superconducting wires used as inductors, transmission lines, or resonators.

Josephson junctions (JJs) are active superconductor devices used for their nonlinear behavior and switching. Physically, JJs are 2-terminal devices commonly made like a thin-film capacitor with superconducting plates or contacts. Other configurations are shown in Figure CEQIP-1. Quantum tunneling of Cooper pairs through the thin barrier layer allows a supercurrent to flow between the contacts with zero voltage drop. The maximum supercurrent is called the critical current, I_c.



a. Vertical orientation b. Horizontal orientation c. Electrical symbol

Figure CEQIP-1 Josephson Junction Device Structures

Superconductor electrodes are shown in gray. Contacts to other circuit elements are not shown. The space between the electrodes can be filled with an insulator, semiconductor, or metal. Dashed lines show an optional weak link, which can be made of the same material as the electrodes. Shown is the modern electrical symbol, which includes two dots symbolizing a Cooper pair [2, 3].

When the current through a critically damped JJ exceeds the critical current, it switches (the superconducting phase difference across the junction jumps by 2π) and produces a SFQ output. Note that the time-dependent voltages and currents produced by the SFQ output depend on the JJ and circuit characteristics, respectively. The switching energy $E_{sw} \sim I_c\Phi_0 = 2 \times 10^{-19}$ J = 0.2 aJ for I_c = 100 μA. Smaller values of critical current I_c are desirable for energy-efficient applications, within limits due to noise and required bit error rate or ratio (BER).

Only discrete values of magnetic flux are possible in a superconducting loop due to the quantum nature of the superconducting state. A simple description is that the superconducting state is associated with a wave function and that the superconducting phase change around a loop must be $2\pi n$, where n is the number of flux quanta in the loop. The value of the magnetic flux quantum is $\Phi_0 = 2.07$ fWb. Expressed in practical units, 1 fWb is equivalent to 1 mA·pH or 1 mV·ps. Phase differences between points within superconductor circuits can be produced by magnetic flux, electric currents, and certain devices engineered to exhibit a strongly spatially dependent superconductor wave function. Superconductor phase engineering is an important part of SCE circuit design without analogy in CMOS circuit design [4].

Superconductor circuits switch magnetic flux using Josephson junctions and store flux in inductors. This is very different from semiconductor circuits, which switch electric charge using transistors and store charge in capacitors. A superconducting loop with inductance L and circulating current I stores magnetic flux $\Phi = LI$. Unlike a loop made with normal, resistive material, the current can circulate for as long as it stays superconducting. The behavior is analogous to an ideal capacitor, but the loop stores magnetic flux instead of charge.

Single flux quantum (SFQ) digital logic represents digital ‘1’ and ‘0’ by the presence, absence, polarization, or location of magnetic flux quanta within a circuit element.

Current supplied to SCE circuits is used to both compensate for energy dissipated and to shift superconducting phase differences within the circuit, biasing operation in a desired direction. Supply current type (ac or dc) and magnitude depend on the circuit or logic family.

2.2. Applications and Market Drivers for SCE

Few of the application areas and market drivers considered by the IRDS Systems and Architectures (SA) and Application Benchmarking (AB) teams [5, 6] are currently relevant for superconductor electronics. The reason is that cryogenic electronics must continue to serve niche and emerging markets until it can build the capability and capacity to address larger markets.

The initial list of application areas for cryogenic electronics is shown in Table CEQIP-1 along with technology areas specific to superconductor electronics. The SCE-specific technology areas were added to enable initial tracking prior to application readiness. The matrix of application and technology areas and market drivers shown in Table CEQIP-2. The example applications and drivers included here are preliminary and require further development. Starting points include a survey of applications and markets for superconductor electronics published in 2010 [7].

Table CEQIP-1 Initial Application and Technology Areas Considered for Superconductor Electronics (SCE)

Application or technology area	*Desired metric*	*Description*
Optimization	Solutions per second	Integer NP-hard optimization problems
Media processing	Frames per second	Discrete processing, including the filtering, compressing, and decompressing of unknown streaming media
Cryptographic codec	Codons per second	Encrypting and decrypting of data at the edge of cryptographic science
Feature recognition	Accuracy, training and inference time and energy	Graphical dynamic moving image (movie) recognition of a class of targets (e.g., face, car). This can include neuromorphic or deep learning approaches such as DNNs.
Sensors *	Accuracy, resolution, rate	Sense physical quantities such as voltage, current, magnetic flux density, or magnetic flux gradient. Example sensors: superconducting quantum interference device (SQUID), superconducting nanowire single photon detector (SNSPD), transition edge sensor (TES), THz superconductor-insulator-superconductor (SIS) and superconducting hot electron bolometer (HEB) heterodyne detectors
Signal processing *	Digital clock rate, bit depth	Filters, analog to digital conversion (ADC), digital to analog conversion (DAC), digital signal processing (DSP) circuits operating either on streaming digital data or in conjunction with ADC and DAC
Sensor array readout *	Rate, multiplexed inputs	Multiplex sensor arrays
Digital computing *	Operations per second, energy per operation, circuit density	Digital computing using single flux quanta (SFQ) in superconductor circuits
Quantum computing *	Coherence time, energy per solution	Qubits, interface and control circuits for quantum computing

* Technology areas specific to superconductor electronics

Applications can be divided into those that already require cryogenic temperatures for some part of the system and those that do not. Applications already requiring a cryogenic environment provide a much lower barrier of entry for cryogenic electronics. Examples where cryogenic environments are required include: cryogen storage and transport, superconducting magnets such as those in magnetic resonance imaging (MRI) machines and nuclear accelerators, cryogenic devices such as single photon detectors and Josephson junctions, and quantum computing. Note that Josephson junctions are key devices for superconductor electronics, metrology standards, THz detectors in radio astronomy, and for magnetic field sensors and gradiometers based on superconducting quantum interference devices (SQUIDs).

Other applications do not require cryogenic temperatures; however, use of cryogenic electronics can improve metrics such as sensitivity, resolution, or energy efficiency. Examples might include: feature recognition, discrete event simulation, optimization, and media processing.

Following is further information about the market drivers included in Table CEQIP-2. Roadmaps will be considered to help provide the required technologies when needed by these market drivers.

Table CEQIP-2 Matrix of Application or Technology Areas and Market Drivers for SCE

Application or technology area	*Market Drivers*			
	*Measurement and calibration systems **	*Digital radio **	*Cloud*	*Cyber-physical systems*
Optimization			G	
Media processing		X		X
Cryptographic codec			X	
Feature recognition		X	X	X
Sensors *	G	X		
Signal processing *	X	G		X
Sensor array readout *	X	X		X
Digital computing *	X	X	P	X

* Technology areas specific to SCE. X: important application; G: critical gating application; P: power-sensitive application.

2.2.1. CLOUD (DIGITAL COMPUTING)

Microprocessor units and memories are currently under development but not yet available as commercial products. Further in the future are large-scale computing applications that require many parallel processors for high-performance computing or data centers [8]. While the market for digital superconductor computing could be large [9], small-scale systems must be developed first and markets found.

2.2.2. MEASUREMENT & CALIBRATION SYSTEMS

Many of the systems in this section make use of quantum sensing, the use of a quantum system, quantum properties, or quantum phenomena to perform a measurement of a physical quantity [10]. Included is signal processing.

SQUID sensors utilize the Josephson and Meissner effects to create sensors [11, 12, 13] that can detect magnetic flux changes at or below the $\mu\Phi_0$ level. The use of flux transformers can allow SQUID sensors to detect field changes at the fT level. Additional circuitry can allow SQUID sensors to detect a wide variety of electromagnetic quantities [14, 15]. SQUIDs with a flux capture area less than 1 μm^2 (nanoSQUIDs) have high-spatial resolution [13, 16, 17, 18].

Table CEQIP-3 Typical Sensitivities of SQUID Instruments

Measurement	*Sensitivity*
Current	10^{-12} A/√Hz
Magnetic flux density	10^{-15} T/√Hz
dc voltage	10^{-14} V
dc resistance	10^{-12} Ω
Mutual or self inductance	10^{-12} H
Magnetic moment	10^{-10} emu

A SQUID can also be used as a null detector in a cryogenic current comparator (CCC) [19] to achieve part-per-billion current resolution with < 0.1 fA/√Hz sensitivity. CCCs have applications in voltage standards [§**2.2.2.2**], quantum Hall effect [20], and in particle accelerator beam diagnostics [21].

The bandwidth of commercially available electronics is typically dc to 100 kHz with flat frequency and flat phase response. Bandwidths of 10 MHz can be achieved by operating in an open loop configuration where the maximum signal does not exceed $\Phi_0/2$. Placing multiple Josephson loops having different loop areas in a series-parallel array [22] offers the potential to achieve < 0.1 fT sensitivity levels. Known as a superconducting quantum interference filter (SQIF), these devices have already demonstrated >10 GHz bandwidths [23]. A combination of sub–fT/√Hz sensitivity levels and GHz bandwidths may allow SQIFs

to be used a wide variety of yet to be discovered applications. While laboratory applications of SQUIDs have been the springboard for significant commercial successes in the areas of biomagnetism, magnetic property measurement systems, and geophysics, the commercial market for laboratory systems is typically at the 2 to 3 million USD level [24]. One potential use of SQUIDs with a significant commercial application is in the detection of low-field MRI signals [25].

Alternatives to SQUID sensors include the superconducting quantum interference proximity transistor (SQUIPT) [26], and possibly Josephson tunnel junctions incorporating stacked structures of normal metal and ferromagnetic layers [27, 28].

2.2.2.1. Biomagnetism and Medical Measurements

The sensitivity of SQUIDs has allowed non-invasive measurements of electrophysiological activity that has led to the development of number of medical instruments [14]. The major use, responsible for over half a billion USD in sales to date, has been magnetoencephalography (MEG) for magnetic source imaging (e.g., focal epilepsy regions). Another area where SQUID-based methodologies offer diagnostic capabilities is magnetocardiography (MCG), particularly in fetal MCG to diagnose fetal heart rhythm abnormalities. Other uses of SQUID biomagnetometers include magnetoenterography (measurements of the stomach and intestines), magnetopneumography (magnetic remnance measurements of the lung), and magnetomyography and magnetoneurography (muscle and peripheral nerve studies). One disadvantage of ultra-sensitive SQUID biomagnetometers is the need for magnetically shielded rooms to reduce the effects of external electromagnetic noise.

The major drivers in the adoption of medical instrumentation are clinical acceptance, cost and safety. Clinical acceptance requires the demonstration of superior, rather than incremental, diagnostic capabilities in a modality that the physician can easily interpret. Medical equipment costing above 1 million USD is limited to medium to large hospitals. When instrument prices drop to the 250,000 USD level, the potential market expands to small hospital and medium to large clinics. Currently the per channel cost for high channel count SQUID biomagnetometers (e.g., MEG) is at or above a few thousand USD. Significant reductions in per channel cost or eliminating the need for expensive magnetically shielded rooms could significantly increase the market for SQUID biomagnetometers.

Improvements in high-temperature SQUID sensors, which are currently more expensive than low-temperature SQUID sensors, could also reduce the cryogenic requirements with a subsequent reduction in system cost.

2.2.2.2. Voltage Standards

Voltage standard systems based on superconducting Josephson junction arrays became commercially available in 1996 and have continued development [29, 30]. An economic impact assessment of NIST's Josephson volt program performed in 2001 found a net present value of 45 million USD in the year 2000 [31]. At least 16 Josephson voltage standard systems were in operation in the United States at that time. Current information is needed about markets and market drivers for voltage standard systems.

Two complementary types of Josephson voltage standards used today are the programmable Josephson voltage standard (PJVS) and the Josephson arbitrary waveform synthesizer (JAWS, also known as the ac Josephson voltage standard or ACJVS) [30]. The main dc application for PJVS systems is the direct calibration of secondary voltage standards. With the 2019 redefinition of base units in the International System of Units (SI), both PJVS and JAWS systems will become key components for the direct realization of the unit volt.

The push to improve ac voltage standards is presently a driver for cryogenic circuit development [32, 33]. One reason is that the output voltage of a JAWS is limited by the number of Josephson junctions (JJs) that can be driven by a single pulse-generator channel. In one paper [33] the number of JJs driven by one generator channel was doubled to 51,200.

2.2.2.3. Magnetic Property Measurement Systems

Since the discovery of high-temperature superconductors, SQUID based susceptometers have been a mainstay in magnetic property measurements. Gradient detection coils surround the sample region of a variable temperature (typically 1.8 to 400+ K) insert. Surrounding the detection coils is a moderately high-homogeneity (100 ppm) superconducting magnet (0 to 9 T). The sample is moved inside the detection coils, and the resulting changes in flux are used to calculate the magnetic moment of the sample. Some systems have both axial and transverse coils. AC susceptibility can be measured by adding ac coils, although the applied fields are much smaller (μT). The dynamic range can vary from 10^{-8} to 2 emu. To date, over 1,300 SQUID susceptometers (from all suppliers) have been delivered generating over 250 million USD in revenues. Commercially available since the late 1970s, this market segment is the premier example that needed a SQUID-based product in quantity. Commercial manufacturers include Quantum Design and Cryogenic, Ltd.

The variable temperature platform can be expanded (without SQUID detection coils) to a variable temperature physical property measurement system allowing a wide variety of measurements to be taken from 50 mK to 800 K in fields exceeding 14 T. The variable temperature susceptometer concept can be converted to remnant field geophysical measurements (§**2.2.2.5**) by removing the dc superconducting magnet and placing three orthogonal detection coils in a magnetically shielded region. Typically placed

in a horizontal orientation, nearly 150 systems have been delivered generating nearly 30 million USD in revenues. Commercial manufacturers include 2-G Enterprises and Tristan Technologies.

Nondestructive evaluation (NDE) systems using SQUID sensors have been reviewed by [34].

2.2.2.4. MICROSCOPY

Microscopes with SQUID or magnetic tunnel junction sensors image surface magnetic flux density with micrometer-scale resolution [35, 36, 37, 38]. Recent developments include a vector-scanning SQUID microscope [39, 40] and a system for investigation of geological samples [41]. Commercial manufacturers include Neocera [42] and Tristan Technologies [43].

2.2.2.5. GEOPHYSICS

Magnetic field gradiometers are used to prospect for magnetic ores [14]. The value of ore deposits discovered is reported to be several billion USD, however, the cost of the cryogenic electronics is a tiny fraction of that amount. These systems require only a few Josephson junctions and can use high-temperature superconductors operating at liquid nitrogen temperatures (~77 K). A survey of applications affecting the environment found additional applications such as the detection of unexploded ordinance (UXO) [44].

2.2.2.6. ASTRONOMY

Radio and Infrared Astronomy has played an essential historical role in superconductor electronics by pulling the developments of sensitive quantum-limited superconducting SIS and HEB heterodyne detectors for millimeter, then submillimeter/THz radio telescopes and infrared telescopes like the Herschel Space Observatory or the Planck satellite. Some astronomy applications using cryogenic sensor arrays [45, 46] are growing in array size to the point that multiplexing and signal processing is needed close to the sensors. The need to go from single pixel detection at THz frequencies to array sensors with thousands or more pixels also exists for THz detectors but suffers currently from technological limitations of back-end processing.

2.2.3. COMMUNICATIONS

Developed communications applications are covered in the following sub-sections. Proposed communication applications include chaos encryption using a circuit with a Josephson junction in parallel with a memristor [47].

2.2.3.1. WIRELESS COMMUNICATIONS

High-temperature superconductor (HTS) filters are used in wireless base stations to increase base station coverage area and data throughput. Superconductor Technologies Inc. has products that operate in over 10,000 base stations [48].

2.2.3.2. DIGITAL RADIO

Software-defined radios perform signal processing entirely in the digital domain. By contrast, traditional radios perform signal processing in the analog domain at a single frequency. Software-defined radios require both ultra-high-speed analog-to-digital converters (ADCs) and equally fast digital signal processing (DSP) of the converted signals, but do not require much memory. ADC and DSP circuits based on superconductor electronics have been demonstrated at speeds up to 40 GHz [49]. The commercial digital-RF receiver manufactured by HYPRES [50] performs ADC and DSP using superconductor electronics [51]. The superconducting components operate at about 4 K with a fully automated and cryogen-free refrigeration system. The application space extends beyond communications to many other uses of the radio frequency spectrum for surveillance, navigation, and spectrum management.

2.3. PRESENT STATUS FOR SCE

Recent advances include the 2015 D-Wave Washington chip with 128 000 Josephson junctions and the 2016 Lincoln Lab shift register chip with 809 150 junctions [52, 53]. Considering that state-of-the-art CMOS processors are available with more than a billion transistors [54], superconductor electronics is still far behind the semiconductor industry in key metrics such as integrated circuit density and complexity. Prospects remain for higher operating speeds and improved energy efficiency, especially for applications requiring operation at cryogenic temperatures.

2.3.1. LOGIC

The most common SFQ logic families and some important characteristics are summarized in Table CEQIP-4 and further described below. Clocked (dynamic) gates can produce only one output per clock cycle, whereas combinational (static) gates have the advantage of allowing greater logic depth per clock cycle. For an explanation of how a simple SFQ gate operates, see [9]. For a recent review article, see [55]. To be identified are additional parameters for future logic family monitoring and comparison. Candidates include average number of junctions or other resources per logic gate (e.g., area, number of layers), energy per operation, or overhead for clock and power supply.

Table CEQIP-4 Superconductor Digital Logic Families

Name	*References*	*Power*	*Static Power*	*Dynamic power (per JJ)*	*Trans-formers*	*Static Gates*	*JJ count $log_{10}(n)$*
RSFQ: rapid single flux quantum	[56]	DC	High	$\alpha I_c \Phi_0 f$	No	No	5
LR-RSFQ: inductor-resistor RSFQ	[57, 58]	DC	Low	$\alpha I_c \Phi_0 f$	No	No	
LV-RSFQ: low-voltage RSFQ	[59, 60]	DC	Low	$\alpha I_c \Phi_0 f$	No	No	
ERSFQ: energy-efficient RSFQ	[61, 62]	DC	0 *	$I_b \Phi_0 f$	No	No	4
eSFQ: energy-efficient SFQ	[63, 64]	DC	0 *	$I_b \Phi_0 f$	No	No	
DSFQ: dynamic SFQ	[65]	DC			No	Some	0
RQL: reciprocal quantum logic	[66, 67, 68]	AC	~0	$\alpha I_c \Phi_0 f$ 2/3	Yes	Some	5
PML: phase mode logic	[69]	AC	~0	$\alpha I_c \Phi_0 f$ /3	Yes	Some	
AQFP: adiabatic quantum flux parametron	[70]	AC	~0	$\alpha I_c \Phi_0 2\tau_{sw}/\tau_x$	Yes	No	3

JJ count : Josephson junction count in largest circuit demonstrated as INT[$\log_{10}$(n)]; α : activity factor (fraction of JJs that switch in a clock cycle); I_c : average critical current; I_b : bias current; τ_{sw} : intrinsic switching time; τ_x : excitation rise/fall time; * : for I_b within the energy-efficient range

2.3.1.1. RSFQ, LR-RSFQ, LV-RSFQ

RSFQ circuits use resistors to distribute dc supply currents. While the use of resistors simplifies superconducting circuit design, the static power dissipated is typically between 10 and 100 times the dynamic power [63]. The required bias current per switching Josephson junction is about $0.7I_c$, roughly 100 μA, and limits the number of junctions in a circuit block to a few thousand. A technique called current recycling allows a smaller dc bias current to cascade through multiple circuit blocks and thus reduce the required supply current [71].

Several large-scale RSFQ integrated circuits have been demonstrated at high clock frequencies around 50 GHz, which include 8-bit microprocessors with memory [72, 73], single-precision floating-point units [74], FFT processors [75], and reconfigurable data paths [76]. These circuits were designed based on bit-serial architecture, and therefore the system performance is somewhat low. Recently gate-level bit-parallel RSFQ circuits have been developed to enhance the performance, and 40 TOPS/W operation of an 8-bit ALU was demonstrated [77]. The circuits were fabricated using the Nb 9-layer, 100 μA/μm^2 process and composed of 10,000 to 20,000 junctions. A bit-serial microprocessor successfully operated at 106 GHz using the 200 μA/μm^2 process [78].

Low-voltage operation of RSFQ circuits improves energy efficiency [79]. A 0.5-mV, 35-GHz, bit-serial microprocessor showed 14-fold improvement [80] compared with the first demonstration [81].

2.3.1.2. ERSFQ, eSFQ

Energy efficient RSFQ (ERSFQ) was developed by Hypres [63, 82, 83]. ERSFQ gates are similar to those in RSFQ, but bias current (power) is distributed using a current-limiting Josephson junction in series with a large bias inductor as well as a clocked feeding JTL to maintain adequate bias voltage, all of which add overhead to gate circuit area. Power distribution for energy-efficient operation adds about 30% to ERSFQ circuit overhead [84]. ERSFQ has been used to make 8-bit parallel adders with 560 and 1360 JJs [85] and a decoder for RAM [86]. Proposed is a superconducting magnetic FPGA based on ERSFQ logic [87].

Efficient SFQ (eSFQ) was also developed by Hypres [63, 88]. In eSFQ the biasing network is designed so that in each clock period the superconducting phase at all bias injection points goes through the same change. Smaller bias inductors are required than for ERSFQ, however the gates must be designed differently. Demonstrations of eSFQ include asynchronous [89] and wave-pipelined circuits [88].

2.3.1.3. DSFQ

Dynamic SFQ was developed recently by Rylov at IBM [65] and is currently at the demonstration stage.

Most logic gates in the existing dc-powered SFQ logic families like RSFQ and ERSFQ operate intrinsically as state machines, i.e., they have internal logic states and normally require a clock signal to reset them to the ground state after each clock cycle. Such explicit use of clock signals in logic networks creates significant challenges with the application of the RTL (register transfer level) design paradigm, a cornerstone of VLSI digital design methodology. RTL subdivides large digital circuits into clocked registers and clock-free, state-free logic networks called combinational logic clouds.

DSFQ uses a nonlinear leakage mechanism that makes the usable hold time of gate storage loops large compared to the subsequent self-reset time. This means that the hold time and hence the gate input skew tolerance become a significant portion of the clock cycle and therefore such gates can be used to build combinational logic clouds.

2.3.1.4. RQL AND PML

Reciprocal quantum logic (RQL) [90, 91, 92] and phase mode logic (PML) [93] are related logic families. RQL encodes a digital 1 using two flux quanta of opposite sense and corresponds to wave pipeline operation. PML encodes digital data as high and low states of the superconducting phase, which dissipates less dynamic power. Both use energy-efficient ac resonator-based distribution for power and clock signals. The power is applied in parallel providing scalability to VLSI. Resonators also provide clock stability with zero jitter and skew. Both RQL and PML include combinational gates that allow 12 levels of logic per pipeline stage at 10 GHz. RQL and PML logic provide component-efficient superconducting gates with the same number of junctions as transistors in CMOS gates as well as full compatibility with standard RTL based synthesis design flow.

Design achievements include tile-based physical design to facilitate automated layout, mitigation of flux trapping, and a resonant clock network for chip-level power distribution with 50% power efficiency. A complete RTL-to-GDSII automated design flow has been developed and used to design a 16-bit CPU [94]. Circuit demonstrations include individual logic gates with 7 dB clock margin; 3.5 GHz resonator powering a shift register with 72,800 JJs and 4 dB clock margin [95]; 16-bit ALU and 16-bit register file [96]; 0.25 MJJ resonator based yield vehicle; and an 8-bit CPU with fully functional debug logic, register file, 8-bit CLA, and performance of write and read memory instructions [97].

2.3.1.5. AQFP

Adiabatic quantum flux parametron (AQFP) logic achieves extremely high-energy efficiency by changing the potential shape adiabatically between double-well and single-well during switching [98]. The typical switching energy is about 4.3×10^{-22} J at 5 GHz clock frequency assuming unshunted junctions with critical current density of 100 $\mu A/\mu m^2$ [99]. The switching energy can be further decreased in proportion to the clock frequency and perhaps even below the Landauer thermal limit by using reversible quantum-flux-parametron (RQFP) gates [100, 101, 102, 103]. Operation at high frequencies with low bit energy and low bit error rate or ratio (BER) was confirmed experimentally [104, 105]. Functional operation has been demonstrated for 8-bit carry-lookahead (CLA) adders [106, 107] and 16-word, 1-bit register files [108]. Multi-excitation circuits (ME-AQFP) can multiply the excitation current frequency, which typically has a maximum of about 5 GHz, by a factor of 2 or 4 to allow AQFP circuit operation up to about 20 GHz [109]. AQFP logic circuits are typically clocked by four-phase AC clocks. Therefore, the logic depth per clock cycle is four. This phase number can be increased to more than 20 for 5 GHz clock frequency assuming a 100 $\mu A/\mu m^2$ junction process [110]. A standard cell design approach is used in the AQFP circuit design, which is similar to CMOS circuit design. An AQFP NAND gate requires 6 junctions, whereas the corresponding CMOS gate uses 4 transistors. Because a majority gate is a fundamental logic gate in AQFP logic, majority-based logic synthesis is desirable [107]. Several circuits components are designed and demonstrated by using an automated top-down design flow, which includes logic synthesis, and placement and routing [111, 112].

2.3.1.6. REVERSIBLE LOGIC STYLES

There has been a long history of efforts to develop superconducting logic styles capable of approaching (logically and physically) reversible computation, starting with Likharev's work on parametric quantrons (PQ) in the 1970s [113], and reversible versions of the original 1987 quantum flux parametron (QFP) of Goto *et al.* [114]. These early efforts relied on adiabatic transformation of the potential energy function in one or more coupled SQUID loops, a theme which continues today in the recent work on negative mutual-inductance SQUIDs (nSQUIDs) [115, 116] and on reversible quantum flux parametron (RQFP) logic [101, 117, 118], a variation on AQFP logic. In addition, several groups have investigated alternative *ballistic* styles of superconducting reversible logic, including a group in Hokkaido in 2008 [119, 120], at Northrop Grumman in 2010 [121], and ongoing work [122, 123] and at Sandia National Laboratories [124, 125]. These efforts aim to surpass the energy efficiency of the existing irreversible logic styles such as those in Table CEQIP-4 and can potentially eventually push beyond the Landauer limit of ~kT energy dissipation per operation that applies to irreversible logic.

2.3.1.7. OTHER SCE LOGIC

Other superconductor logic families to be tracked include those based on nano-cryotrons [126, 127, 128], Josephson junction oscillators [129], and control of magnetic flux quanta using magnetic fields [130].

Quantum phase slip junctions (QPSJ) are superconductor nanowire devices with a nonlinear I-V characteristic. QPSJs are a dual to Josephson junction devices, with the roles of phase and charge interchanged as well as current and voltage [131, 132, 133, 134, 135, 136]. Nanowire devices might have fabrication advantages over Josephson junctions, although recent fabrication experience with NbN nanowires indicates that challenges remain [134]. While the switching energy is expected to be lower for QPSJs than for JJs, phase slips are susceptible to charge and thermal noise and thus might require lower temperature operation. Needed is demonstration of QPSJ-based circuits.

Weak-link nanobridges are being investigated as scalable alternatives to SIS Josephson junctions [13, 137, 138].

Chiral nanotubes of tungsten disulfide might be useful as superconducting diodes [139].

Magnetic elements are incorporated in devices such as SFS junctions [140], SFIS junctions [141], SIsFS junctions [142, 143, 144], and superconducting ferromagnetic transistors with SISFIFS structures [145]. SIsFS junctions are promising due to their high-I_cR_n product, up to about 2 mV, that determines the maximum switching frequency of the device. Such junctions have non-single-valued current-phase relationships (CPR) as discussed in §**2.3.2.2**. Magnetic junctions can be used as phase shift elements not intended to switch [146]. Benefits can include reduction in bias current required, reduction in junction count, and increased operating margins.

High-temperature superconductors (HTS) have a critical temperature T_c greater than 30 K. Josephson junctions produced in $YBa_2Cu_3O_{7-\delta}$ (YBCO) films by helium-ion beam irradiation have been fabricated with junction widths down to 50 nm [147]. A step-edge HTS Josephson-junction mixer operated at 600 GHz and temperatures of 20–40 K with superior performance [148]. Progress on applications of high-temperature superconducting microwave filters has been reviewed [149]. Still, the large spreads typical in HTS device characteristics are problematic for SFQ logic. The small coherence lengths typical of HTS materials cause junctions made of these materials to be very sensitive to fabrication variations. So, requirements for Josephson nanostructures must be even stronger than for low T_c systems, while the accuracy of HTS junction fabrication is much more difficult to achieve.

Spintronic superconductor electronics is a new field since about 2000. Like traditional spintronics, the approach is to utilize spin currents for information processing. Contrary to charge current, spin current does not conserve and is not always accompanied by charge transfer, so might be more energy efficient. Reviews of superconductor spintronics include [150, 151, 152, 153]. This new field is at the stage of development and demonstration of device concepts rather than production. It is not easy to produce spin superconducting currents, however, once created they persist in superconductors much better in both equilibrium [154] and nonequilibrium transport [155, 156, 157]. The use of spin currents to switch memory devices is covered in §**2.3.2.2**.

2.3.2. MEMORY

Superconductor electronic memory can be classified by memory device technology: 1) Josephson junction logic circuits, 2) magnetic devices, or 3) nanowire superconductor devices; and by use: (a) register, (b) cache, or (c) main memory.

In JJ logic circuits and in nanowire superconductor devices, the magnetic flux in a superconducting loop in steady state is quantized and thus can be used to provide the physical basis for a digital memory element. The absence or presence of a flux quantum in the loop represents binary ‘0’ or ‘1’. Superconducting memory cells have one or more Josephson junctions in the loop to control and sense the number or location of flux quanta present.

2.3.2.1. JJ MEMORY

The largest demonstrated superconducting random-access memory (RAM) is still only 4 Kibit (4096 bits) [158, 159].

RQL-RAM uses pure RQL logic and is under development by Northrop Grumman [160]. The unit cell consists of three RQL gates, including a single NDRO gate for state and readout and two gates to implement the multiplexer. Projected energy per read or write is 1 fJ per 64-bit word, and projected memory cell density is 300 Kibit/cm^2 at 90 nm feature size. A variant called PRAM combines NDRO storage with a SQUID-based readout multiplexer. Both RQL-RAM and PRAM read and write in a single clock cycle. PRAM is expected to achieve better density, speed, and power than RQL-RAM at sizes greater than 2 Kibit. RQL-RAM has been demonstrated as a complete array of size 16×8 [161]. PRAM has been demonstrated as a complete array (drivers, unit cells, sense amps) in a 4×4 array [162]. The read path shared by JMRAM and PRAM has been demonstrated as a 16×16 array (decoders, drivers, unit cells, sense amplifiers, and test wrappers).

2.3.2.2. MAGNETIC MEMORY

Magnetic materials affect nearby superconductors and layers with aligned magnetizations have a stronger effect. The effects can be used for superconductor logic as covered in §**2.3.1.7**. Here the concern is only memory devices. One method to make a memory element uses two magnetic layers, one that can be switched (free) in direction and a second that is magnetically hard and serves as an unswitched reference. Switching the free layer so the two layers are either parallel or antiparallel changes the effect on nearby superconductors and can be read as memory states ‘0’ and ‘1’. Magnetic memory devices for SCE have similarities to magnetoresistive RAM (MRAM) developed for conventional electronics, however, there are also significant differences. Several types of magnetic memory devices for superconductor electronics are shown in Figure CEQIP-2.

Memory cells can be based on changes in magnetic memory device (i) Josephson critical current [163], or (ii) superconducting phase difference in the ground state [55].

2.3.2.2.1. SUPERCONDUCTING SPIN VALVES (SSV)

Figure CEQIP-2a shows an example device structure. Two magnetic layers affect a single superconductive layer, changing the superconducting critical current. A similar device type with only one magnetic layer containing multiple domains works by changing the degree of domain alignment.

Status: Superconducting spin valves with magnetic control of superconducting critical temperature (T_c) require some effort to implement in SCE, nevertheless, they are actively developed in two main configurations: FSF [164] and SFF [165]. Parallel configuration of F-layers magnetization suppresses superconductivity and provides lower T_c, while antiparallel configuration provides higher T_c of a thin superconducting film. In the range between these two critical temperatures, the magnetization reversal of one free (F) layer switches between normal and superconducting states. Long-range triplet creation may provide an additional way to drain Cooper pairs from the superconductor, and thus produce an even larger T_c shift [166]. The use of a half-metallic ferromagnet in SFF spin valves produces a giant spin-valve effect with T_c shift ~ 1 K [167]. These structures require that the T_c shift at magnetization reversal be larger than the superconducting transition width to fully switch the superconductor, a challenge that appears manageable [164, 167, 168, 169].

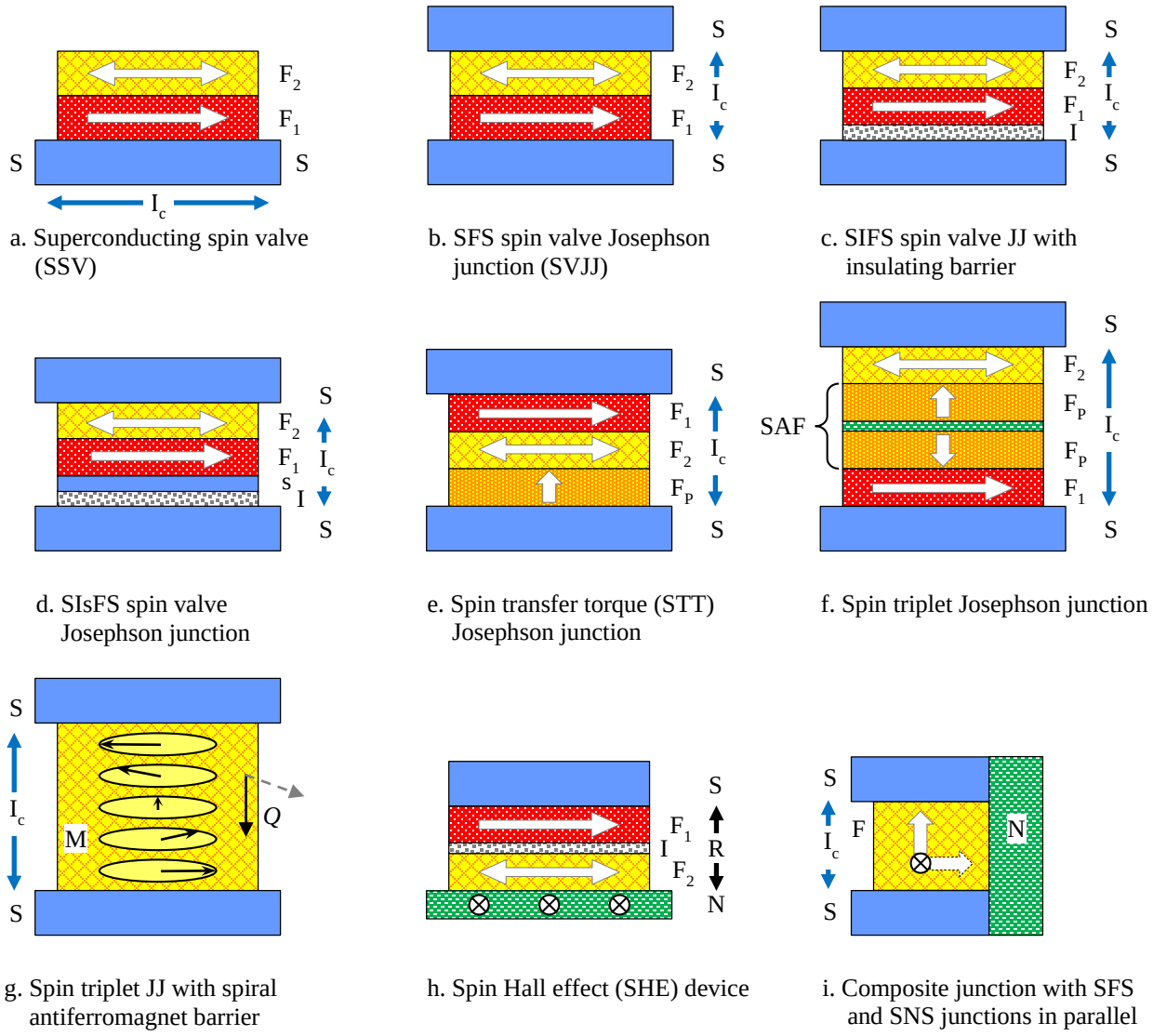


Figure CEQIP-2 Magnetic Memory Device Structures

Superconductors (S) are shown in solid blue. Ferromagnetic materials (F) are shown with magnetization direction either fixed (hard) or bidirectional (soft). Insulators (I) are speckled gray. Normal metals (N) are checkered green. Buffer layers are not shown except within a SAF.

2.3.2.2.2. SPIN VALVE JOSEPHSON JUNCTIONS (SVJJ)

Figure CEQIP-2b shows the basic superconductor-ferromagnet-superconductor (SFS) device structure. The superconducting critical current passes directly through the magnetic layers. Adding an insulator layer (SIFS) as shown in Figure CEQIP-2c increases the normal state resistance and can provide a larger characteristic voltage V_c if the combined barrier layers are sufficiently transparent for the device to have a large critical current. The tunnel current through the insulating barrier can be increased by sandwiching it between two superconductor layers (SIsFS) as shown in Figure CEQIP-2d.

Challenges include sensitivity to magnetic layer thicknesses and quality, and the need to switch the free layer using magnetic fields produced by external control circuits.

Status: Spin valve Josephson junctions are under development by Northrop Grumman in collaboration with Michigan State University [160, 170, 171], Hypres (USA), Lomonosov Moscow State University, Institute of Solid State Physics RAS (Russia), and others. Northrop Grumman is developing Josephson magnetic random-access memory (JMRAM) using a spin valve Josephson junction for state and a SQUID-based readout multiplexer. Unit cell size, set by the readout multiplexer, scales to 32 Mibit/cm^2 with 90 nm feature size. The projected read and write energies per 64-bit word at 4 K are 10 aJ and 50 fJ, respectively. Advantages of JMRAM are high density and reads that are fast and low energy. Writes are expected to take longer than 1 ns but could be tolerable using memory latency hiding techniques. The JMRAM unit cell and its write drivers have been demonstrated as stand-alone devices [172].

SIsFS junctions with a single ferromagnetic layer are under development experimentally [142, 143, 173] and theoretically [144, 174]. These junctions include a soft ferromagnetic layer of PdFe with about 1% iron that changes magnetic state in a weak external field, thereby shifting the Josephson current Fraunhofer pattern and thus the current-phase relationship (CPR).

2.3.2.2.3. SPIN TRANSFER TORQUE JOSEPHSON JUNCTIONS (STTJJ)

Figure CEQIP-2e shows an example device structure. Spin transfer torque (STT) devices use spin-polarized currents to switch the magnetization direction in one layer within the device. Switching the free layer is performed by passing current through a spin polarizing layer F_P. The resulting spin current produces a torque on the free layer that depends on current direction. Spin current production is covered in §**2.3.1.7**. STT junctions might scale to smaller sizes than SVJJs as they do not rely on magnetic fields produced by nearby control wires. Challenges include the need for bi-directional write currents, high current density required for switching, and difficulty fabricating the polarizing layer.

Status: STT switching has been observed in Josephson junctions with pseudo-spin-valve barriers $Ni_{0.8}Fe_{0.2}$/Cu/Ni, although the switching currents were high [175]. Orthogonal spin-transfer (OST) devices are under development by a team including Raytheon BBN Technologies and New York University [176].

2.3.2.2.4. SPIN TRIPLET JOSEPHSON JUNCTIONS (S3JJ)

Figure CEQIP-2f shows an example device structure. The synthetic antiferromagnet (SAF) in the structure shown serves to fix the F_P layers in a perpendicular orientation. Noncollinear magnetization of the magnetic layers can create spin triplet Cooper pairs, which have a longer range than the ordinary spin singlet Cooper pairs [152, 177, 178]. Also required are nonmagnetic spacer layers to decouple magnetic layers while promoting high magnetic quality in the subsequent layer. An advantage is that the 0-π switching is caused by spin rotations rather than phase accumulation as in SVJJs, so device behavior is less sensitive to the exact thicknesses of the F_1 and F_2 layers. Challenges include getting sufficiently high critical current density in a structure with so many layers.

Status: Birge's group at Michigan State University is developing memory devices based on Josephson junctions with spin triplet supercurrent [178, 179, 180]. The most recent work demonstrated controlled switching of the ground-state phase difference between 0 and π, but the critical currents were less than 10 μA.

Spiral (helical) antiferromagnets have been proposed as an alternative barrier material for superconducting spin triplet spin valves [181, 182, 183, 184] and spin triplet Josephson junctions [185]. Figure CEQIP-2g shows an example device structure that replaces multiple barrier layers with a single layer with spiral magnetization. Switching the spiral magnetization vector Q between stable states can change both I_c and the ground state (zero current) superconducting phase difference φ_0. MnSi develops helical magnetic order below a transition temperature of 29.5 K and might be a suitable material that could produce 0-π junctions with layer thickness in the range of 3.2 to 4.0 nm. The potential barrier separating spiral magnetic orientations might make these devices less susceptible to half-select problems. Needed is demonstration of memory elements.

2.3.2.2.5. Spin Hall effect (SHE) devices

Figure CEQIP-2h shows an example device structure with current ⊗ going into the normal metal layer at the bottom. Spin-orbit torque (SOT) from the spin Hall effect in heavy metals can rapidly and reliably switch an adjacent ferromagnet (F) free layer of a nanoscale magnetic tunnel junction in a three-terminal configuration. Challenges include the need for bi-directional write currents and write voltages difficult to provide with SFQ circuits.

Status: Buhrman's group at Cornell University together with Raytheon BBN (USA) have demonstrated cryogenic spin Hall effect memory devices [186]. SHE devices with perpendicular magnetization are projected to have very good switching characteristics [187] but have not been demonstrated. Recent developments include better spin Hall materials that combine high spin torque efficiency with low resistivity [186, 188, 189]. Writing is fast but requires more voltage than SFQ circuits can provide, so memory cells with nano-cryotron drivers are under development [190]. Needed is demonstration of memory arrays.

2.3.2.2.6. Composite junctions

Figure CEQIP-2i shows an example composite junction consisting of two parallel regions with different characteristics. In the structure shown, the SNS portion functions as a Josephson junction with 0 phase difference at zero current and the SFS portion can function as a π-phase junction. The composite junction functions as a SQUID consisting of the two junctions in parallel. The readout time of such memory elements is estimated as 10s of picoseconds. Writing by magnetization reversal requires times on the order of 10 ns [55]. Composite junctions with a non-single-valued current-phase relationship (CPR) might be able to switch between two logic states by changing the current through the device, which could occur on the picosecond timescale. Some of these theoretical predictions were based on nonuniform SF-FNS junctions with different structures [191, 192]. Recent theoretical work indicates that the structure shown in Figure CEQIP-2i is most suitable for practical realization among those considered [193]. Challenges are likely to include fabrication, scalability to small sizes, and incorporation into accessible memories.

2.3.2.2.7. Other magnetic memory devices

Josephson junctions with Si barriers containing Mn magnetic nanoclusters have been demonstrated to function as memristive elements capable of synaptic weight training using electrical pulses with energies as small as 3 aJ [194]. Proposed is a memory element containing a magnetic EuS magnetic film on top of a NbN nanowire [195]. Proposed is a hybrid memory using Josephson junctions and Toggle MRAM [196].

2.3.2.3. Other cryogenic memory

Hybrid superconductor-CMOS memories are covered in section **3.3**.

Nanowire-based memory devices are under investigation by a few groups [126, 197].

Ternary memory cells using Josephson junctions have been proposed [198, 199].

Superconducting memristors [200, 201] and meminductors [202] have been proposed, but not yet demonstrated.

2.3.3. Other Circuit Elements for SCE

Inductance required in superconductor circuits can be provided by wires. A complication is that magnetic inductance depends on the full geometry of the circuit, including ground planes that carry current return paths [203]. Magnetic flux from the inductors can also interfere with nearby circuits. Inductance can also be provided by thin superconducting films with high kinetic inductance [204] or by stacks of Josephson junctions [205]. Tolpygo et al. [204] argue that fabrication of thin-film inductors is much simpler and expected to have a higher yield than stacked junctions, although the relative advantages of each deserve further study.

Phase shift elements set or change the superconducting phase φ between locations in a superconducting circuit. Bias currents through circuit elements also can be used to shift the phase but must be supplied to the circuit and can decrease circuit operating margins due to bias current variation. Devices to provide a phase shift are reviewed in [206].

2.3.4. Architecture

Von Neumann microarchitectures typical in CMOS microprocessors are also common in superconductor processors using SFQ logic. Recent examples include 8-bit microprocessors with memory [72, 73], a 16-bit bit-slice ALU for 32- or 64-bit RSFQ microprocessors [207], and design of a 16-bit RQL CPU [94]. Gate-level deep pipelining with bit-parallel architecture can be disadvantageous for CMOS due to pipeline register overhead but appears promising for SFQ processor designs [208]. A RISC-based 4-bit AQFP microprocessor is also under development [209].

The small amount of SFQ-compatible memory available for microprocessors has driven alternative architectures such as reconfigurable data-path processors [76], and the use of so-called MAGIC cells incorporating the functions of both memory and logic [210, 211].

Superconductor field-programmable gate arrays (SFPGAs) were first proposed in 2007 using RSFQ logic circuits and RSFQ NDROs as memory elements [212]. Proposed is an RSFQ SFPGA using magnetic Josephson junctions (MJJs) for implementation of area-efficient switches [87]. An all-SFQ FPGA design that allows both combinational and sequential logic is analyzed for chip sizes from 5 mm × 5 mm to 50 mm × 50 mm [213]. An AQFP SFPGA with a cryo-CMOS memory has been designed and a 2×2 unit system demonstrated [214]. FPGAs can provide significant benefits to users in flexibility and reconfigurability, but at a cost of significant circuit overhead. Challenges for superconductor FPGAs include switch matrix overhead using SFQ logic and the low density of superconductor circuits, which does not yet allow sufficient functionality in a single-chip SFPGA. Still, work is needed to prepare for the time when sufficient circuit density and complexity is available.

Neuromorphic approaches to computing using superconductors and Josephson junctions are under development [134, 136, 194, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226]. As intrinsically nonlinear elements, Josephson junctions might have advantages for artificial neural networks such as speed and energy efficiency. An artificial synapse based on ferromagnetic Josephson junctions demonstrated a spiking energy per pulse less than 1 aJ [194].

Memcomputing uses logic elements containing memory. Digital memcomputing machines with self-organizing logic gates have been simulated with promising results [227, 228, 229]. Needed is replication of the results reported.

2.3.5. FABRICATION FOR SCE

Josephson junctions are typically made by forming a barrier layer sandwiched between two superconducting electrodes, a structure like a thin-film capacitor shown in Figure CEQIP-1a. A variety of materials can be used, but most common for SFQ logic operating in the 4 K temperature range are junctions made with niobium electrodes separated by a thin aluminum oxide barrier layer (for details, see §**2.3.5.1**). The horizontal orientation shown in Figure CEQIP-1b is also possible, although less common as the barrier is more difficult to fabricate.

Weak link or nanobridge junctions consist of a small filament of superconductor or normal metal between larger electrodes. The diameter and length of the weak link need to be around the superconducting coherence length, which is about 38 nm for Nb and 5 nm for NbN (see Table CEQIP-6). Such dimensional control was difficult until recently and sandwich junctions were easy to produce, so processes for making weak link junctions have not been refined to the extent necessary for fabrication of complex circuits. Prospects for weak link junctions are explored, for example, in [16, 137, 138].

Acceptable process variations are typically tighter for Josephson junctions than for CMOS transistors, which presents fabrication challenges, especially as the push for greater energy efficiency drives designers toward smaller junctions. On the positive side, superconductor electronics has less need to reduce device sizes as Josephson junction switching speed does not depend directly on device size and superconducting interconnects reduce the penalty for sending signals over a distance. Still, there are significant advantages to increasing the number of devices on a chip, so the push to smaller device and feature sizes continues.

Planarized processes for superconductor integrated circuit fabrication have been developed by AIST [230, 231, 232], MIT Lincoln Laboratory [233, 234, 235], and Hypres [236]. Unplanarized processes are in use at IPHT, Star Cryoelectronics, and SIMIT [237, 238]. The Chinese fab at SIMIT is among the most recent additions. Materials and devices recently added to foundry processes include MoN_x superconductor layers with high kinetic inductance and self-shunted Josephson junctions [204, 239, 240].

SCE fabrication processes are summarized in Table CEQIP-5. The barrier material Al-AlO_x indicates formation by thermal oxidation of an aluminum layer that is only partially consumed. To be identified are key process parameters for future monitoring. Candidates include variability of I_c and J_c, R_n and I_cR_n product, sub-gap resistance R_{sg} or R_{sg}/R_n ratio, inductance per square, metal layer thickness, dielectric thickness, and yield.

Table CEQIP-5 Fabrication Processes for SCE

Organization	*Process*	*Wafer sizes*	*F [nm]*	*Wire material, layers*	*Barrier material*	*J_c [$\mu A/\mu m^2$]*
AIST, Japan	SDP [230]	3 inch	1500	Nb, 4	Al-AlO_x	25
AIST, Japan	ADP2 [232]	3 inch	800	Nb, 9	Al-AlO_x	100
MIT LL, USA	SFQ4ee [233]	200 mm	500	Nb, 8	Al-AlO_x	100
MIT LL, USA	SFQ5ee [233]	200 mm	350	Nb, 8; MoN_x, 1	Al-AlO_x	100
MIT LL, USA	SFQ5hs	200 mm	350	Nb, 8; MoN_x, 1	Al-AlO_x	200

Organization	*Process*	*Wafer sizes*	*F [nm]*	*Wire material, layers*	*Barrier material*	*J_c [$\mu A/\mu m^2$]*
MIT LL, USA	SC1 [235]	200 mm	250	Nb, 8; MoN_x, 1	Al-AlO_x	100, 200
D-Wave, USA	SFQ	200 mm	250	Nb, 6	Al-AlO_x	100
NGC, USA	RQL25	150 mm	250	Nb, 7	Al-AlO_x	100
Hypres, USA	RIPPLE-2 [236]	150 mm	250	Nb, 6	Al-AlO_x	100
STAR Cryoelectronics, USA	Delta-1000 [241]	150 mm	1000	Nb, 3	Al-AlO_x	1
Leibniz-IPHT, Germany	SQUID [242]	100 mm	2500	Nb, 2	Al-AlO_x	0.7–3.5
Leibniz-IPHT, Germany	RSFQ1H [242, 243]	100 mm	2500	Nb, 3	Al-AlO_x	10
NIST, USA	SQUID	3 inch, 150 mm	600	Nb, 3	Al-AlO_x	10
SIMIT, China	SFQ [237, 238]	100 mm	350	Nb, 4	Al-AlO_x	10, 0.3–100
SUNY Polytechnic, USA	Qubit Rev.0 [244, 245]	300 mm	140	Al, 2	Al-AlO_x	0.2–2
NIST, USA	Voltage std [246]	3 inch, 150 mm	600	Nb, 2	Nb_xSi_{1-x}	200
NIST, USA	SFQ [239]	3 inch	600	Nb, 4	Nb_xSi_{1-x}	50–100
PTB, Germany	Voltage std [240]	3 inch	250	Nb, 4-5	Nb_xSi_{1-x}	40, 100

F : feature size, minimum; J_c : critical current density

2.3.5.1. NIOBIUM-BASED JUNCTION FABRICATION

Josephson junction fabrication for non-quantum applications (T > 1 K) typically involves formation of the junction layer stack, commonly called the trilayer, followed by junction definition. The layer stack is typically formed as a series of steps without exposure to atmosphere. Key layers include base superconductor, barrier, and top superconductor (or counter electrode). While the barrier can be any non-superconductor or weak link, most common for superconductor electronics are insulator or semiconductor barriers are as they produce higher switching voltages and speeds. The critical current through a Josephson junction depends on the quality of the superconducting electrodes, especially near the barrier layer.

2.3.5.1.1. BASE SUPERCONDUCTOR FORMATION

Nb (niobium) has a critical temperature T_c of about 9.2 K and is the most common superconductor for electronic applications at liquid helium temperature, near 4 K.

The superconductive properties of Nb are strongly dependent on purity [247]. Degradation of Nb films can occur by exposure to hydrogen [248, 249] or oxygen [250]. Properties can also change over time by diffusion through the Nb and between adjacent materials such as Ti [251]. Good superconducting properties favor Nb films with a columnar grain structure and large grains, however a rough surface under thin barrier layers can cause problems. A smooth Nb surface is desired as junctions fabricated on rough surfaces show increased variation [252]. One way to reduce Nb surface roughness is to deposit the base electrode using Nb/Al/Nb multilayers [253]. Nb surface morphology also can be controlled by bias target ion beam deposition (BTIBD) [254]. Other factors affecting Nb quality include residual stress in sputtered Nb films, film thicknesses, surface morphology, deposition rate, substrate temperature during deposition, and substrate preparation [270].

2.3.5.1.2. BARRIER LAYER FORMATION, ALO_X

As seen in Table CEQIP-5**,** aluminum oxide is the most common barrier for SCE with Nb electrodes. The usual process involves deposition of 5 to 10 nm of Al on the base Nb layer, exposure to oxygen gas to form ~ 1 nm of AlO_x on top of the Al, and deposition of the Nb top electrode [234]. The Al layer wets Nb well, smooths out roughness in the underlying Nb surface, and provides a relatively flat surface for growth of the oxide layer. The Al layer is only partially consumed during oxidation. Formation of the Al/AlO_x barrier is a complex process and conduction through the barrier can depend on many factors. Plots of critical current density J_c as a function of oxygen exposure show regions with different slopes at low and high J_c [234]. Very thin

barriers with high J_c shows evidence of conduction through numerous, small channels, perhaps related to defects or impurities in the oxide. As the oxide thickness increases, the number of high-conductivity channels decreases and conduction transitions to percolation between high-conductivity regions. Thicker oxide layers are dominated by tunneling of Cooper pairs (supercurrent). For a recent summary of understanding, see Koberidze et al. [255].

Although remarkable progress has been achieved using Al/AlO_x barriers, several challenges will need to be addressed for scaling circuits to higher complexity, integration density, or speed. Perhaps the most serious challenge is the thermal stability of the amorphous aluminum oxide barrier, often designated AlO_x as it is not necessarily Al_2O_3. Many groups have observed a significant degradation of junction properties when processing temperatures exceed 200 °C. The necessity to keep processing temperatures low limits the temperature allowed for the interlayer dielectric deposition (typically SiO_2), which has been optimized for Si-based microelectronics above 200 °C. The low processing temperature limit for AlO_x also complicates integration of these junctions with other circuit components such as magnetic memory elements and CMOS devices.

Another concern for AlO_x is the need for monolayer thickness uniformity in high critical current density, self-shunted junctions. The properties of junctions are expected to be exponentially dependent on the thickness of the oxide layer, so that as the oxide thickness is reduced below 1 nm, high yield requires limiting thickness variations to less than a monolayer across large wafers, which is extremely challenging. Recent fabrication improvements have dramatically reduced the number of junctions with properties outside the design range (“outliers”), but the mechanism responsible for the remaining outliers is not yet completely understood. If related to non-uniform oxide thickness or the presence of a non-uniform defect population, new approaches will be needed to achieve high yield upon further scaling [256]. Barrier formation by atomic layer deposition (ALD) shows promise but needs to be demonstrated in a production process [257].

Self-shunted junctions for use in SFQ circuits can be made by various methods reviewed in [258]. Methods with AlO_x barriers include very thin barrier layers [234] or increasing the Al thickness so that the barrier includes a thicker normal metal layer in series with the insulating oxide layer [259].

2.3.5.1.3. Barrier Layer Formation, Alternatives to AlO_x

Nb-Si barriers are deposited as amorphous silicon with niobium in solid solution. Other designations for this barrier material include Nb_xSi_{1-x} and a-Si-Nb. Nb-Si films of interest for SFQ circuits are on the insulating side of the metal-insulator transition, which means less than about 11% niobium [260]. Nb-Si has lower resistivity than AlO_x, so greater thickness is required. Nb-Si barrier Josephson junctions have been used for several years in commercial voltage standard chips containing many thousands of Josephson junctions (see §**2.2.2.2**). The potential for application of Nb-Si barriers in SFQ circuits that operate at higher clock frequencies is under active investigation [239, 240, 261]. Advantages include a thicker barrier layer and thus less sensitivity to small changes in thickness. Disadvantages include low thermal stability [262], high dielectric constant [239], and difficulty in achieving uniformity across a wafer.

Aluminum nitride (AlN_x) tunnel barriers have good characteristics up to high current densities, although formation by plasma nitridation of an Al layer is more difficult than the formation of AlO_x barriers [263]. Although nitride barriers are expected to have higher thermal stability than AlO_x above 200 °C, statistical studies on the stability of junction properties fabricated with higher processing temperatures have not yet been performed. Halfnium oxide (HfO_x) was investigated as an insulating barrier material, but fabrication of good junctions was found to be difficult [264]. Tungsten nanorod weak links have been fabricated with MoRe electrodes and might also work with Nb electrodes [265, 266]. Graphene barriers have been demonstrated using CVD compatible with wafer-scale fabrication [267]. Needed are further studies of alternative barriers to determine whether they have significant advantages over AlO_x.

2.3.5.1.4. Top Superconductor Formation

The top Nb layer is typically deposited directly on top of the AlO_x barrier using the same deposition parameters for other Nb layers. There is some concern that the thin AlO_x layer could be damaged by energetic deposition of Nb atoms or that chemical reactions could occur at the AlO_x/Nb interface. A thin layer of Al deposited on top of the barrier and under the Nb top layer can improve junction properties [268].

2.3.5.1.5. Junction patterning and definition

After deposition of the junction trilayer, individual junctions are defined by photolithography followed by wet anodization of exposed Nb and Al [269]. Note that wet anodization is not a common process in semiconductor foundries. Processes have been developed without anodization and are being evaluated for production use [270].

2.3.5.2. ALTERNATIVE SUPERCONDUCTORS

While a variety of materials exhibit superconductivity [271], only a few are used in electronic circuits. Superconductor materials and properties relevant to superconductor electronics are given in Table CEQIP-6. The status of superconductor electronics based on materials other than Nb is summarized in following subsections.

Table CEQIP-6 Superconductor Properties for SCE

Material	*T_c [K] Bulk*	*T_c [K] Thin Film (thickness)*	*Band gap $2\Delta_0$ [meV]*	*Coherence length, ξ [nm]*	*Mag. pen. depth, λ_L [nm]*	*J_c [mA/μm^2]*	*Crystal structure*	*T melt [K]*
Al	1.18		0.34	1600	16		fcc, A1	933
In	3.41		1.0				tetragonal	430
MgB_2	39	close to bulk	1.8-7.5	3.7-12 ab 1.6-3.6 c	85-180		C32	1100
MoGe	7.4	4.4 (7.5 nm) [272]	2.2			12 (250 mK)	amorphous	
MoN	12						hexagonal	
$Mo_{0.6}Re_{0.4}$	15	12 (20 nm) [273]					A15	
MoSi	7.5	4.2 (4 nm) [272]				11–25 (1.7 K)	amorphous	
Nb	9.2		3.0	30–38	90		bcc, A2	2750
NbN	16	8.6 (3 nm) [272]	4.9	5	270	20–40 (4.2 K)	cubic, B1	2846
NbTiN	12–16							
NbSi	3.1	2 (10 nm) [272]	0.94			0.14 (300 mK)	amorphous	
Nb_3Sn	18.3		7	4	30		A15	
NbTi	9.0		3	5	150			
Pb	7.2						fcc, A1	601
TiN	5.5						cubic, B1	3200
WSi	5	3.7 (4.5 nm) [272]	1.52			8 (250 mK)	amorphous	
$YBa_2Cu_3O_7$	92		50-60	1.5 ab ~0.3 c	140 ⊥ 700 ||		perovskite	> 1270

⊥ : magnetic field perpendicular to the layers; || : magnetic field parallel to the layers; Strukturbericht symbols for crystal structures

2.3.5.2.1. NBN AND NBTIN

NbN (niobium nitride) and NbTiN (niobium titanium nitride) each have bulk T_c of about 17 K, which can be approached for films thicker than about 100 nm. Both materials have a crystal structure that does not match well with Si or SiO_x, but buffer layers can be used to improve the superconducting properties [274]. NbTiN films just 4 nm thick have been fabricated with a T_c of about 10 K [275].

Josephson junctions have been fabricated with insulating barriers of deposited AlN [276, 277, 278], AlN formed by nitridation of an Al layer [279], thermally oxidized Al [280], deposited MgO [281, 282, 283, 284, 285], deposited MgO-AlN-MgO [286], and thermally oxidized HfO_x [287]. Self-shunted junctions can be made using conductive barrier materials such as Ti-N [288] or Ta_xN [286, 289, 290, 291, 292]. Note that pure Al is far more difficult to nitridize than to oxidize, which is one reason that directly deposited barriers are more common on NbN and NbTiN. Another reason is that pure Al pulls N from adjacent NbN or NbTiN, which degrades the superconducting properties of both layers. Using a Hf diffusion barrier along with tunnel junction barriers of either HfO_x or Al-AlO_x showed limited success and sensitivity to the thickness of the Hf layer [293].

Fabrication processes for integrated circuits have been developed [277].

Ferromagnetic Josephson junctions using NbN have been fabricated [294, 295]. GdN can function as a spin filter in NbN junctions [296].

Needed is work on magnetic shielding and flux trapping in NbN and NbTiN circuits. The magnetic penetration depth of these materials (λ_L > 200 nm) is large, which means that much greater thickness might be required for shielding than in pure Nb (λ_L ~ 90 nm). Nb layers might be used for shielding.

2.3.5.2.2. MgB_2

Magnesium diboride (MgB_2) has a critical temperature T_c of about 39 K and exhibits s-wave superconductivity, which implies that it can be used to make three-dimensional materials and devices more easily than with the d-wave, planar superconductors. MgB_2 films of good quality have been fabricated using hybrid physical-chemical vapor deposition (HPCVD) on Si wafers coated with a boron buffer layer to prevent chemical reactions between Mg vapor and the Si substrate, however deposition and growth temperatures are high (~700 °C) [297]. Josephson junctions fabricated in sandwich geometry with MgO barriers have some attractive properties, but also unacceptably large critical current distributions [298, 299]. In-plane Josephson junctions with barriers formed by helium ion beam irradiation show reduced parameter spreads, but work is needed to increase the I_cR_n product of the junctions [299, 300, 301]. Additional challenges include lack of multi-layer interconnects and degradation of MgB_2 on exposure to atmosphere, which makes patterning more difficult.

2.3.5.2.3. YBCO

Yttrium barium copper oxide (YBCO) is a family of crystalline compounds with a defect perovskite structure consisting of layers. $YBa_2Cu_3O_{7-x}$ (also known as Y123) can have a superconducting critical temperature around 90 K, although the superconducting properties are much better in the a-b plane than in the c direction. The small coherence length (ξ ~ 1.5 nm in the ab plane) makes YBCO sensitive to grain boundaries and makes fabrication of Josephson junctions difficult. Challenges include high-synthesis temperatures (> 700 °C), poor conductivity across high-angle grain boundaries, brittleness, lack of multi-layer interconnects, and large scatter in Josephson junction critical currents.

Grain boundary junctions in YBCO have been used to make small RSFQ circuits [302]. Large numbers of step-edge junctions have been fabricated by argon ion milling steps into an MgO substrate before deposition of the YBCO film, although I_c variation was high (1σ = 20 to 30%) [303]. In-plane Josephson junctions with barriers formed by helium ion beam irradiation show promise [147]. Applications tolerant of Josephson junction variation seem most promising, including junction arrays for magnetic sensors and amplifiers, microwave generators, and vortex-flow transistors [304]. Applications without junctions might include superconducting interconnects between environments below 10 K and intermediate temperatures in the 20 to 80 K range where semiconductor circuits can operate with less refrigeration penalty.

2.3.5.2.4. Other Superconductors

Re (rhenium) is a superconductor with a relatively weak tendency to oxidize, which is advantageous in superconducting quantum circuit and qubit applications. Re/Al-AlO_x/Re Josephson tunnel junctions have been fabricated with a T_c of 4.8 K [305].

Molybdenum–rhenium (Mo–Re) alloys exhibit superconducting transition temperatures up to 15 K in bulk and up to about 9 K in thin films [273]. Mo–Re thin films can be sputter deposited at room temperature and are stable even under typical carbon nanotube CVD growth conditions that require a hydrogen-methane atmosphere at 900 °C. Josephson junctions have been fabricated with barriers of Si(W) [306, 307, 308, 309], tungsten nanorod weak links in Si [265], and graphene [310]. Challenges include the cost of Re, which is roughly 100 times that of Nb.

TiN (titanium nitride) with a T_c of 5 K has been used to make TiN/AlN/TiN junctions for use as photon detectors [311].

2.3.5.3. Fabrication Facilities and Equipment

The IC Insights forecast for 2018 is that 300 mm wafers represent about 70% of worldwide integrated circuit capacity, 200 mm wafers represent about 25% of capacity, and almost all the remainder is for wafers of 150 mm or smaller diameter [312]. The choice of wafer size is important for SCE fabrication as fabrication processes and yield depend on the tooling available. Processes developed for one wafer size can require significant changes when migrated to a different wafer size. SCE fabrication on 300 mm wafers has begun and should help inform when or whether the benefits justify the cost [244, 245].

Magnetic layers in superconductor circuits can be fabricated using equipment developed for the general electronics and MRAM industries [313].

2.3.6. Electronic Design Automation (EDA) for SCE

EDA tools developed for semiconductor circuits require modifications to be useful for designing superconducting circuits. For example, inductance—whether self or mutual—is critical in superconducting circuits. Connecting wires must have inductance values within a specified range to allow either pulse transmission or quantized flux storage. Mutual inductance within tight margins is required for the successful operation of logic gates that contain transformers, such as AQFP and RQL, while parasitic inductance and coupling must be minimized to maintain acceptable circuit operating margins. Standard EDA tools have poor

inductance extraction capability, ignore the kinetic inductance important in superconductors, and cannot route wiring subject to inductance limits. Numerical inductance solvers are needed, and InductEx [314] is one three-dimensional inductance extraction tool developed for superconductor integrated circuit structures such as logic gates [315].

Further, SFQ circuits use pulse-based logic, not the voltage-state logic for which most EDA tools have been developed, so that timing definitions differ. Timing parameters in SFQ circuits are state-dependent, and critical timings can exist between any pair of inputs that may exclude the clock [316]. EDA tools for SCE must thus include timing extraction and HDL model generation tools that handle state-dependent pulse-based timing characteristics.

EDA for SCE must also address phenomena that do not affect semiconductor circuits, of which the most important is flux trapping analysis and mitigation. Moats in the ground planes of superconductor circuits provide low-energy locations for magnetic flux to trap during cool-down, but flux trapping analysis tools are required to calculate optimal moat positions and analyze the detrimental effects of persistent currents in superconducting loops induced by nearby trapped flux [317].

The status of EDA for SCE has been reviewed [318, 319, 320] and recent work includes [203, 321, 322, 323, 324]. The ongoing IARPA SuperTools program seeks to develop a complete EDA tool chain for SCE [320, 325, 326] that includes back-end capabilities for device and gate design, and front-end capabilities for behavioral-to-logic and clock tree synthesis and automated placement-and-route methods. Models for Josephson junctions are fundamental to circuit simulation. The RCSJ model is easy to implement in circuit simulators like SPICE, but the accuracy can be inadequate for high-J_c, self-shunted JJs [327]. The more accurate Werthamer model is easiest to implement in simulators based on superconducting phase like PSCAN2 [328] rather than in simulators based on voltage levels like SPICE, which has resulted in the rise of dual-capability superconductor circuit simulators such as JoSIM that allows both voltage and phase-based simulation [329].

2.3.7. Packaging and Testing for SCE

Superconductive multichip module (S-MCM) technology has been developed for superconductor chips [330, 331, 332]. The most advanced process can make S-MCMs up to 35 mm × 35 mm using interposers with 4 layers of Nb and 600 nm minimum feature size fabricated on 200 mm silicon wafers [332].

Packaging for cryogenic optoelectronic devices is reviewed by [333].

Semiconductor chips are typically tested before wafer dicing and packaging of good die. Needed are systems capable of wafer testing at cryogenic temperatures so that SCE chips can also be tested at wafer scale. Thermally induced voltage alteration (TIVA) is a room-temperature failure analysis technique recently found useful with SCE circuits [334, 335]. Needed is research on the extent to which TIVA at room temperature can take the place of circuit testing at cryogenic temperatures.

Failure analysis (FA) techniques for SCE are largely similar to those for other nanoelectronic technologies, but with some different materials and concerns [336].

2.3.8. Interconnects for SCE

On-chip data interconnects can be either Josephson transmission lines (JTLs) or passive transmission lines (PTLs) [337, 338, 339]. JTL cells include 2 JJs, both of which switch when transmitting a digital ‘1’. Long JTLs consume too much energy and result in too much time delay and jitter, so PTLs are often preferred for distances longer than a few gate lengths. SFQ signals travel ballistically on PTLs at roughly one third the speed of light and can travel several millimeters before regeneration is required. A drawback of PTLs is that matching the stripline impedance to a Josephson junction driver, which typically has low impedance, can require a stripline with signal line width of 1 to 10 μm. Stripline and microstrip impedance scaling is discussed in [337]. Losses in Nb striplines of 250 nm width were found to be dominated by losses in the dielectric at low power and in the superconductor at high power [340].

Chip-to-chip communication using SFQ pulses has been demonstrated at data rates up to 117 Gbit/s over microstrip lines 6.4 mm long [341] and up to 82 Gbit/s over microstrip lines almost 20 mm long [331]. Double-flux-quantum pulses can be used for longer distances or improved signal-to-noise [342]. ERSFQ circuits for 16-bit parallel data transmission have been demonstrated [343].

Within the cryogenic environment, superconductors can be used for both power and data. Niobium has a superconducting critical temperature T_c of about 9 K and has been used to make coaxial cables [344] as well as flexible ribbon cable transmission lines on thin film polyimide [345]. NbTi has a similar critical temperature, but lower thermal conductivity, and has also been used to make coaxial cables [346] and microstrip ribbon cables [347]. Electroplated rhenium (Re) in multilayers with noble metals has an enhanced critical temperature of about 6 K and could have fabrication advantages [348].

Power and data need to move between the cryogenic and room temperature environments with very low heat load to the cryogenic environment. Most challenging is movement of data from a cryogenic environment due to the small energy in an SFQ pulse and the refrigeration penalty on any energy dissipated in amplifying or converting signals at cryogenic temperatures [349]. Placing signal amplifiers at multiple temperature stages can reduce total power dissipation [350, 351, 352, 353]. An approach using

polarization modulation vertical cavity surface emitting lasers (PM VCSELs) at 4 K showed some promise but was never fully developed [354]. An electro-optical modulator based on graphene was patented recently [355].

2.3.9. REFRIGERATION

Cryogenic cooling technologies have developed steadily over the past three decades based on various well documented thermodynamic heat engine cycles [356] moving the industry away from a reliance on liquid cryogens towards new cryogen-free closed cycle apparatus. This has been beneficial for the research community and is increasingly being adopted for industrial and medical applications. It is estimated that helium usage for low-temperature physics is ~4% of global helium consumption and declining [357]. Not only does this enable greater access to cooling technologies through reduced operating costs, ease of use, reduced safety considerations and reduced reliance on access to liquefiers and gas supply chain it has also introduced a change in design considerations. Gone are the constraints placed on vessel size and shape considerations due to optimal cryogenic consumption performance such as neck diameter for services, cabling, cryoelectronics thermalization and staging. New considerations are available cooling powers at intermediate temperatures, the interdependence of the available cooling power at these stages, mechanical vibrations, electrical & acoustic noise, and utility & power requirements. Furthermore, applications with 'ride through' or 'duty cycle' requirements such as MRI and gyrotron beamline injection magnets have already demonstrated that hybrid structures utilizing a helium bath with integrated closed cycle cooler continuously recondensing the boiling liquid can maintain steady state operation for long term continuous operation.

Cryogenic technologies require refrigeration, unlike most other beyond CMOS technologies. Comparison at room temperature, taken as 300 K, requires accounting for the power cost of cryogenic refrigeration. The specific power of a refrigerator is defined as the input power divided by the cooling power. Note that specific power is the inverse of the coefficient of performance (COP). The specific power of an ideal Carnot refrigerator varies with temperature as $(T_H - T_L)/(T_L)$ where T_H is the high temperature at which heat is rejected and T_L is the low temperature at which cooling takes place. Cryogenic refrigeration system efficiency, and thus specific power, varies depending on cold-end temperature, refrigeration capacity and design [358].

The approach taken is to use box plot statistics for specific cooling powers of commercial refrigeration systems at cold-end temperatures of interest. The effect of refrigeration can be presented using a simple whisker plot using only the minimum, median, and maximum specific power values rather than a full box plot. Specific powers for benchmarking and metrics use are summarized in Table CEQIP-7. Details are in Table CEQIP-8 through Table CEQIP-10. Note that refrigeration at $T \sim 4$ K is split into high- and low-power groups as their performance characteristics too different to combine. Low-power refrigerators for $T \sim 4$ K are often called cryocoolers. Cryogenic refrigeration systems for T ≤ 1 K are listed in Table CEQIP-10 and are typically dilution refrigerators [359].

Needed is a model for specific power values at other temperatures, perhaps using cryogenic refrigeration performance models [360, 361]. Such a model might be used to produce nominal values that are less sensitive to the collection of existing refrigerators.

Table CEQIP-7 Specific Power Ranges for Cryogenic Refrigeration

T cold	*Cooling Power Range*	*Specific Power * [W/W]*			
		Average	***Low***	***Median***	***High***
80 K	1.4 W to 600 W	59.6	13.3	**51.0**	150.0
40 K	1.0 W to 200 W	279.3	58.5	**167.4**	750.0
20 K	3.2 W to 100 W	444.9	117.0	**446.4**	937.5
4.5 K	(≥ 10 W) 130 W to 1000 W	403.5	315.0	**390.6**	576.9
4.2 K	(< 10 W) 0.08 W to 2.0 W	1.07E+04	4.00E+03	**8.30E+03**	3.75E+04
100 mK	0.1 mW to 1.0 mW	3.72E+07	1.27E+07	**2.95E+07**	1.07E+08
20 mK	6 μW to 30 μW	1.13E+09	4.56E+08	**9.75E+08**	2.08E+09

* Specific power: (W at 300 K)/(W at T cold)

Table CEQIP-8 Cryogenic Refrigeration Systems for T > 10 K

Table CEQIP-9 Cryogenic Refrigeration Systems for 1 K < T ≤ 10 K

Table CEQIP-10 Cryogenic Refrigeration Systems for T ≤ 1 K

2.4. BENCHMARKING AND METRICS FOR SCE

Beyond-CMOS electronics must consider new devices, circuits, and architectures. Determining which emerging or novel technologies are most promising and thus most deserving of development effort can be difficult, especially for significantly non-conventional technologies such as cryogenic electronics. Fair and effective metrics and figures of merit are needed for comparison.

2.4.1. DEVICE AND CIRCUIT BENCHMARKING

Recently, there have been efforts to benchmark a variety of beyond-CMOS technologies [362, 363, 364, 365]. Nikonov and Young [362] included in traditional energy-delay comparisons some state variables other than voltage (e.g., magnetization, polarization, spin current, orbital state) and extended comparisons from switching devices alone to logic circuits as large as an arithmetic logic unit (ALU). Still, the existing benchmarks and metrics did not consider superconductor electronics, and are limited as computing also requires interconnects and memories, not just logic circuits.

First, consider intrinsic device switching energy versus switching time (delay) and how to add superconductor electronics to existing comparisons. Nikonov and Young include data for beyond-CMOS devices fabricated at the 15 nm scale in Table 5 of their supplemental material [362]. For Josephson junctions in RQL technology with critical current density J_c = 100 μA/μm^2 and device current I_c = 100 μA, the intrinsic switching energy $E_{sw} = I_c\Phi_0/3$ = 69 zJ [90, 99]. The intrinsic switching time is taken as the SFQ pulse width, roughly FWHM [366, 367], $t_{sw} = (\pi\Phi_0 C_s/2J_c)^{1/2}$ = 1.5 ps with specific capacitance C_s = 70 fF/μm^2 typical of junctions with this J_c.

AQFP-based logic is a benchmarking challenge as the switching device is a circuit that moves between two states semi-adiabatically. The switching energy depends on ramp rate as $E_{sw} = 2I_c\Phi_0\, t_{sw}/t_x$, where t_x is the excitation time [99, 100] The intrinsic switching time is $t_{sw} = (2\pi\Phi_0 C_s/\beta_c J_c)^{1/2}$ = 0.21 ps for the AIST, Japan ADP2 junction fabrication technology with J_c = 100 μA/μm^2, specific capacitance C_s = 63 fF/μm^2, and unshunted junctions with damping parameter β_c = 190. For a 5 GHz clock frequency with t_x = 100 ps and I_c = 50 μA, E_{sw} = 0.43 zJ. For AQFP gates, the delay is given not by the intrinsic junction switching time t_{sw} or by the excitation time t_x, but by the clock period divided by the number of phases. For 4-phase clocking at 5 GHz, the delay is 50 ps. Multi-excitation AQFP (ME-AQFP) [109] could increase clock frequency to 20 GHz and reduce the delay to 12.5 ps, however the energy-delay product remains constant, so the energy would increase by a factor of 4 to 1.7 zJ.

Figure CEQIP-3 shows the energy versus delay for several switching devices including RQL and AQFP. The energy-delay product for these superconducting logic technologies is seen to be competitive, even including the cost of cryogenic refrigeration. This is due to the fact that the energy-delay product is the ratio of the consumed power by the square of the speed (clock frequency) of the circuits. Since the power is fixed by external constraints (cost, volume, mass, etc.) this factor is fixed for a given application, independently from the technology that is used. Then speed, hence superconductors, come into play.

Next, consider interconnects. The energy versus delay for beyond-CMOS interconnects of 10 μm length is plotted in Figures 7 and 8 of Pan and Naeemi [365]. For RQL, Dorojevets, et al. [368] give data transfer energies for 32-bit Josephson transmission lines (JTL) and passive transmission lines (PTL) with I_c = 38 μA in their Figure 1. On a per-bit basis and removing the refrigeration allowance, the transmission energies for a 1 mm distance are (6.3 fJ)(1000 μm)/[(50 μm)(96 bit)(1000 W/W)] = 1300 zJ/bit for 100 μm by JTL and (12.5 fJ)/[(96 bit)(1000 W/W)] = 130 zJ/bit for up to 20 mm by PTL. The delay for a JTL is about an SFQ pulse width times the number of JTL cells t_{JTL} = (1.5 ps)(1000 μm)/(25 μm) = 60 ps. A PTL consists of 2 JTL cells on each end of a ballistic transmission line, so the delay for a PTL is t_{PTL} = (4)(1.5 ps) + (1000 μm)/(100 μm/ps) = 16 ps, where c/3 ≈ 100 μm/ps is the approximate speed of propagation on the PTL. Note that JTLs and PTLs have different characteristics beyond energy and delay. For example, the repeater distances are 25 μm for JTL versus 20 mm for PTL, and area is required from different layers. For JTLs and PTLs in the RSFQ logic family, see [338].

AQFP gates output currents, not SFQ pulses, and have different interconnect characteristics. Buffer (repeater) cells have the energy and delay of a single AQFP gate with a maximum drive distance of about 1 mm [369]. AQFP (5 GHz) interconnect energy and delay are thus 0.43 zJ and 50 ps for distances of 0 to 1 mm. For 20 GHz operation the delay decreases to 12.5 ps, and the energy increases to 1.7 zJ.

Figure CEQIP-4 shows the energy versus delay for interconnects of 1 mm length including RQL and AQFP. The energy-delay product for these superconducting logic technologies is seen to be better than the alternatives, even including the cost of cryogenic

refrigeration. This plot for interconnects of a single length does not show that the energy remains the same for AQFP out to 1 mm and for PTL (RQL) out to 20 mm. Note that an error was made in the equivalent 2017 figure (BC4.1b) that made the differences appear smaller: the alternative technologies were plotted for 10 μm length and the superconductor technologies for 100 μm length, 10 times longer.

Some applications require the electronics to operate at cryogenic temperatures. Examples include some digital-RF receivers, focal plane arrays for astronomy, quantum computing, and magnetic resonance imaging (MRI). For operation at 4 K, all technologies would require refrigeration, in which case RQL and AQFP have a clear advantage.

A generalized methodology for comparing superconductor electronics with other technologies will require several developments. To avoid the effort of full-circuit simulations, performed in [368], models must be developed for energy, delay, and circuit area for a variety of superconductor technologies. The effort can start from previous work such as [99, 370, 371], but will need to be extended considerably. Metrics are needed that allow comparison of technologies at very different feature sizes. Interconnect benchmarking is needed as a function of transmission distance. Clocking delay must be included for logic families such as RSFQ that require clocking of each gate.

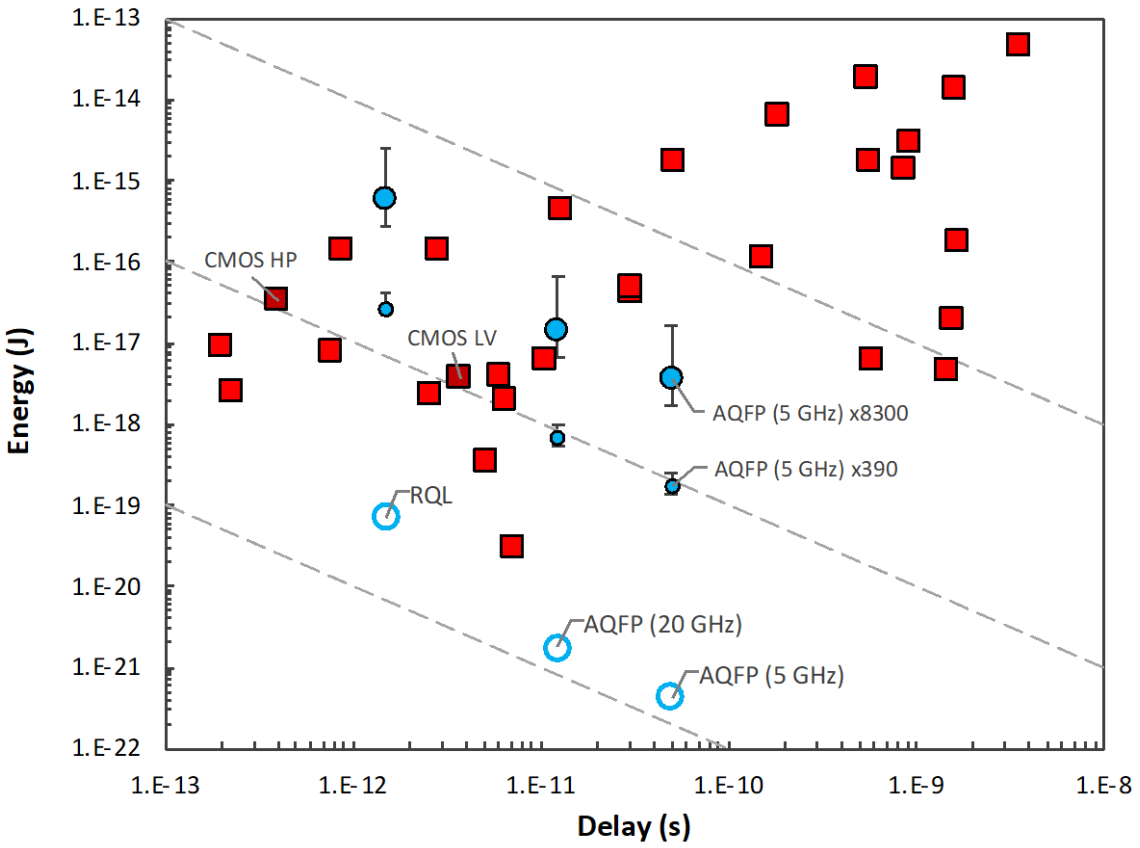


Figure CEQIP-3 Energy versus Delay for Intrinsic Elements

Note: Superconductor devices (AQFP, RQL) have open circles for operation at ~4 K and solid circles with whiskers showing ranges including refrigeration power from Table CEQIP-7. The upper solid circles with ranges are for small-scale refrigerators (cryocoolers) with cooling powers less than 10 W. All other devices are from [365]. Dashed lines show constant energy-delay products.

Table CEQIP-11 Energy versus Delay for Intrinsic Elements

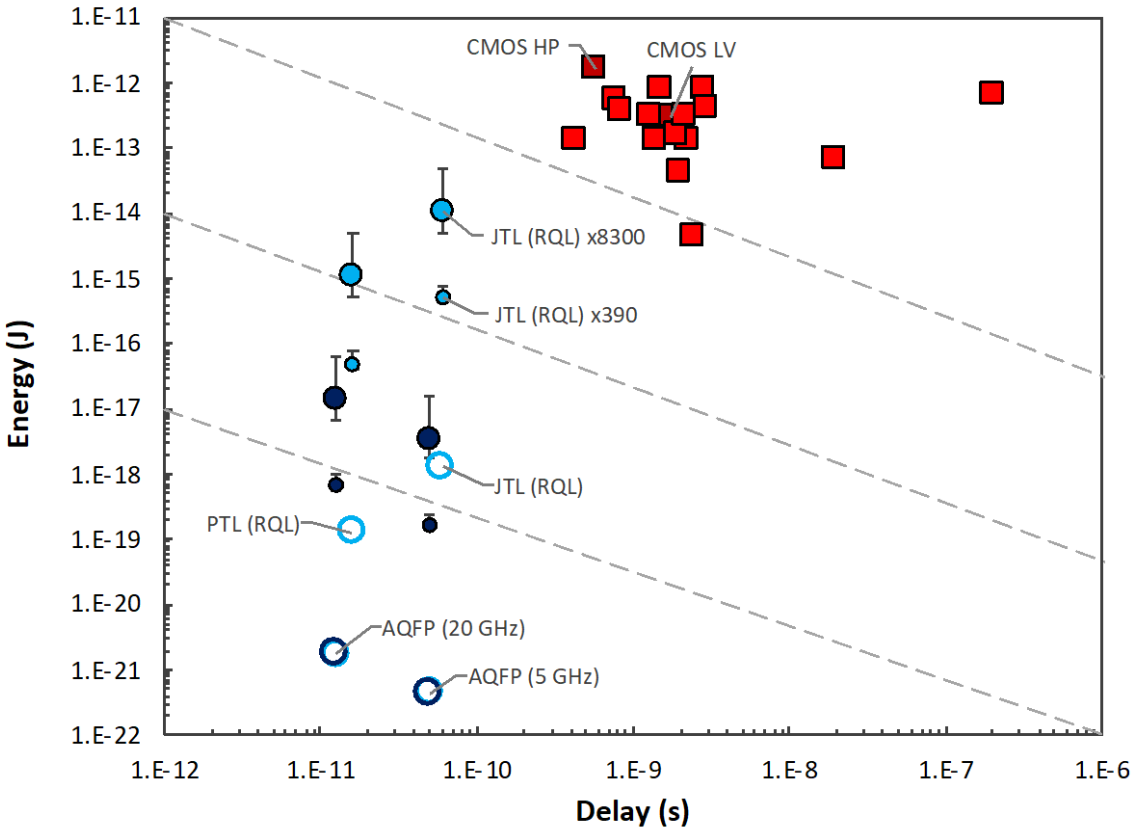


Figure CEQIP-4 Energy versus Delay for Interconnects of 1 mm Length

Note: Superconductor devices (AQFP, RQL) have open circles for operation at ~4 K and solid circles with whiskers showing ranges including refrigeration power from Table CEQIP-7. The upper solid circles with ranges are for small-scale refrigerators (cryocoolers) with cooling powers less than 10 W. All other devices are from [365]. Dashed lines show constant energy-delay products.

Table CEQIP-12 Energy versus Delay for Interconnects of 1 mm Length

Table CEQIP-12b Energy versus Delay for Interconnects of 0.01 to 1 mm Length

2.4.2. System and Application Benchmarking

Pan and Naeemi [364] make the case that some beyond-CMOS devices offer fundamentally different or unique characteristics best suited to novel circuit implementations not well evaluated by traditional metrics and benchmarks. IRDS will need methods for including energies, delays, and other parameters of key system components to more accurately predict the performance of complete digital computing systems based on emerging technologies. For cryogenic electronics, relevant figures of metrics including computation, communication (data movement), memory, and resources such as chip area are needed.

2.5. Active Research Questions for SCE

Difficult challenges for SCE are described in Table CEQIP-13. Future work includes identification of key challenges and tracking of active research.

Table CEQIP-13 Difficult Challenges for SCE

Near-Term Challenges: 2018-2025	*Description*
Integrated circuit fabrication	Foundries for commercial production now process 200 mm or smaller wafers using equipment lacking state-of-the-art capability. Achieving the yield and throughput for large-scale applications will require process improvements and, possibly, a move to 300 mm wafers. Planarization and thickness control is challenging in stacks of multiple superconductor layers when the layer thicknesses remain the same, rather than increasing with layer number as in CMOS back-end processes.
Device variability	Variation in device parameters reduces the operating margins of circuits. Needed is better process control, better device designs, or circuit designs that tolerate or compensate for device variability.
High critical current density junctions (J_c > 100 μA/μm^2)	The AlO_x barrier in Josephson junctions with J_c = 100 μA/μm^2 is now approximately 1 nm thick. Thinner barriers increase J_c, allowing smaller and faster JJs. For J_c > 500 μA/μm^2 the sub-gap resistance can be sufficiently low to eliminate the need for shunt resistors. Uniformity control will be challenging as defects typically dominate conduction through thinner barrier layers and thickness control is also difficult. Materials and process development is needed to improve uniformity and control of devices with high J_c.
Superconducting materials with higher critical temperature (T_c)	Higher T_c materials would allow operation at higher temperatures, which would significantly reduce the required cooling power, or would make circuits less sensitive to self heating at temperatures well below T_c. Niobium (Nb) is the superconducting material most common for 4 K applications. Changing the superconducting material would require significant development and might also require changes in the junction barrier. Processes for large-scale integrated circuit fabrication require multiple superconductor layers, vias, and high-uniformity junctions. Changes in other materials-dependent properties such as magnetic penetration depth λ, superconducting coherence length ξ, and kinetic inductance would require redesign of devices and circuits.
Magnetic materials fabrication process integration	Magnetic materials are desired to make both memory and passive devices and can enable compact high-value inductors and high-coupling factor mutual inductances. Integrating magnetic materials into foundry processes will be difficult. Materials and device geometries with lower magnetization are needed to reduce switching energy. Magnetic properties at room and cryogenic temperatures do not seem to correlate, so measurement is required until adequate theory can be developed. Better fixed magnetic layer materials are needed as nickel has problems that will prevent scaling to small sizes. Interface roughness and morphology must be controlled for good magnetic properties.

Near-Term Challenges: 2018-2025	*Description*
Electronic design automation (EDA) tools	EDA tools for CMOS are not adequate for SCE. Inductance is critical in superconducting circuits and connecting wires must have inductance values within a specified range. Circuit simulators and timing analysis must be modified for pulse-based logic. Flux trapping analysis—both for trapping probability and the coupling of trapped flux in moats to circuits—is required, while analysis of the coupling of bias current and ground plane return currents to circuit structures are also important and difficult at chip level. The modeling of Josephson junction dynamics for EDA simulation tools is currently not sufficiently accurate for self-shunted junctions, and the extraction of more complete simulation models with the aid of technology CAD (TCAD) methods will become important as device size shrinks.
Switching devices	Fan-in or fan-out greater than one requires additional circuitry due to the low gain and low isolation provided by Josephson junctions (in contrast to semiconductor transistors). SFQ-compatible devices with greater gain and isolation are under development, but not yet proven in large-scale fabrication.
Shrinking devices and interconnects at dimensions of tens of nanometers	The state of the art for complex superconducting circuits deal with Josephson junctions with sizes down to 200 nm and passive circuitry with linewidth down to about 90 nm (for nanowire-based detectors for instance). These dimensions are of the order of the London penetration depth but higher than the superconductor coherence length in most of cases and really much higher than CMOS typical scales. What happens in practical electronic circuits when 1, 2 or even the 3 dimensions of a superconducting object reach or go even below the coherence length? Can we make nanodevices of the same dimensions of semiconductor circuits?
Interconnects, on-chip and chip-to-chip	Superconducting passive transmission lines (PTLs) used for ballistic transport of SFQ pulses must have low impedance to match the low impedance available from Josephson junction drivers. Grounded shields are also required to avoid crosstalk, which require more area and reduce circuit density. Also needed are higher-impedance Josephson junctions or methods for making smaller transmission lines with lower impedance.
Interconnects between cryogenic and room temperature environments	Interconnects for both digital and analog signals require careful optimization to balance electrical and thermal properties. Use of cryogenic semiconductor and photonic components in data links require further development.
Packaging for SCE	Operation at cryogenic temperatures requires different materials, packaging, testing, and cooling systems, much of which will require new development. State-of-the art systems package a few superconductor ICs in a commercial cryostat. Scaling up to systems with higher complexity chips and multi-chip modules will require further reduction of power consumption by all components. Josephson junctions are extremely sensitive to magnetic fields and require shielding, which becomes more challenging as system volumes grow.
Long-Term Challenges: 2025-2032	*Description*
Temperature limits compatible with CMOS fabrication processes	Nb/Al-AlO_x/Nb Josephson junctions are sensitive to temperature. Fabrication processing temperatures are currently limited to less than 200°C, which requires different processes than those used in CMOS technology, which has a limit of 400°C. A different barrier to allow use of standard CMOS processes would allow access to existing processes used to make fine features and reduce process development costs, but requires new barrier development.

Near-Term Challenges: 2018-2025	*Description*
Cryogenic refrigeration	The cost of refrigeration can be prohibitive for small systems that do not require a cryogenic environment for some other reason. Cryogenic refrigerators have improved immensely, driven in part by the requirement for the trouble-free operation of MRI systems in hospitals. Still, improvements in the efficiency of small refrigerators (less than 1 W at 4 K) would reduce the system size for which superconducting computing becomes competitive. More efficient or lower cost refrigeration systems for temperatures below 10 K would help to reduce operating costs.
Optical input/output (I/O)	Communication with room-temperature systems and networks will require a high-data-rate I/O, but interconnection cannot introduce significant heat into a low-temperature environment. Optical fiber digital links would be ideal, but efficient SFQ-to-optical converters must be developed.
Cost	Costs of superconductor electronic devices, circuits, and systems are presently high, partly due to low fabrication volumes.
Higher temperature (T_c) superconductors	The energy-delay product of a digital gate is given by the power consumption divided by the square of the speed. It gives a good advantage to superconductors, counterbalanced by the fact that the integration density is currently much smaller than for CMOS. Moreover, interconnects are necessary for complex multi-chips systems and their limitations between chips and between temperature stages will dominate the ultimate system performances. The use of self-shunted Josephson junctions **with T_c above 30 K and with R_nI_c products in the 5-10 mV range is very challenging**, but would open the range of applications and increase circuit performance significantly, for example: clock frequencies close to 1 THz, reduced need for signal amplification for transmission to room temperature environments, much more energy-efficient refrigeration above 20 K, and higher circuit density in absence of external shunt resistors.

2.6. ROADMAP FOR SCE

Of the areas in cryogenic electronics (SCE, cryo-semi, QC), the largest market potential and need for improved capability are in the SCE and QC areas. A roadmap for SCE will be developed first as the technology and needs are better understood. Past SCE roadmapping efforts provide a base for future efforts [7, 318, 367, 372, 373, 374, 375, 376, 377, 378].

Foundry and fabrication are key technology areas for SCE and face some challenging decisions. Foremost is identification of suitable foundries. Of the facilities currently capable of producing complex superconductor circuits (> 100,000 Josephson junctions), MIT Lincoln Laboratory is not allowed to produce commercial products, and D-Wave Systems has limited access. At least one foundry that can handle the materials specific to SCE and produce commercial products with sufficient yield is needed. Multi-project wafer (MPW) service is desirable and will require well-characterized processes and more complete process design kits (PDKs) than currently available.

Technology areas in the SCE roadmap might include foundry and fabrication processes, packaging and integration, and design tools. Proposed and under consideration are the following goals for the SCE roadmap.

Near term (0–7 years)

- self-shunted junctions
- 150 nm linewidth
- 200 nm vias
- 5 μm diameter through-silicon vias
- 10 million JJ circuit complexity

Long term (8–15 years)

- 15 metal layers
- 3 JJ layers
- 100 nm vias
- bump density comparable semiconductor industry

New materials, processes, and devices will need to be added. Approaches to increase circuit density and complexity include: smaller feature sizes, stud vias, high sheet resistance layer, increase critical current density J_c, self-shunted JJs, increase wiring layers, multiple JJ layers, high kinetic inductance layers, magnetic JJs, stacked JJ inductors, or ac-to-dc rectifiers. How these will be developed and incorporated into the foundries is an open question. The achievable rate of progress must be considered. The packaging and integration area might include parameters such as chip sizes, contact count and layout, and memory interface specification.

3. CRYOGENIC SEMICONDUCTOR ELECTRONICS (CRYO-SEMI)

3.1. INTRODUCTION

Reasons for operating semiconductor electronics at cryogenic temperatures include: 1) performance improvement (e.g., lower noise, higher speed, increased efficiency) or 2) to support a sensor, actuator or other device in a cryogenic environment. For a brief introduction, see [379].

In the 1980s ETA Corporation built several computers with as many as 2000 CMOS chips operating in liquid nitrogen [380]. More recently, commercial cryogenic electronic components were evaluated for suitability at 4.2 K and used successfully to build a complete digital to analog multiplexer [381].

In addition to cryogenic CMOS circuits, bipolar technologies (e.g., SiGe heterojunction bipolar transistors) offer advantages in higher operating speeds when cooled to lower temperatures. While standalone cryogenic semiconductor circuits may not offer a compelling advantage over their room-temperature counterparts due to the higher power consumption required for cryogenic refrigeration, they might in applications requiring cryogenic devices and circuits. Since cryogenic semiconductor devices operate over a wide range of temperatures, one can optimize the overall power consumption of a hybrid-temperature system by selecting the appropriate operating temperature of different cryogenic semiconductor circuits and subsystems. In combination with superconductor electronics, a wide range of cryogenic semiconductor circuits have potential use. These include memory, processor, and amplifiers for digital data links [350, 351, 352], as well as microwave analog signals.

General references include [382, 383]. A review by Valentine and McCluskey covers cryogenic semiconductor devices and packaging [384].

3.2. APPLICATIONS AND MARKET DRIVERS FOR CRYO-SEMI

Advances in cryogenic semiconductor capabilities historically have been driven by the needs of sensors such as low-bandgap semiconductor detectors operated at cryogenic temperatures. Applications tended to be in the medical, scientific and aerospace/defense markets. In recent decades, the rapid improvement of semiconductor performance following to Moore's law and Dennard scaling made development of cryogenic semiconductors for higher performance too difficult to justify. However, as Moore's law nears its end and new paradigms are being explored for high-performance computing, cryogenic semiconductors could play an enabling role.

Quantum computing research and development is driving increased investment in cryogenic electronics, including cryogenic semiconductors. Quantum computers that operate at cryogenic temperatures, typically in the millikelvin temperature range, require communication with and control by classical (non-quantum) electronic systems. The closer the classical systems can operate, both in distance and temperature, the better. Cryogenic semiconductor electronics developed for quantum computing is also finding applications elsewhere. For example, Rambus initially started development of cryogenic semiconductor memory in support of quantum computing efforts at Microsoft, but more recently has been pursuing broader applications that benefit in power/performance metrics [385].

Application areas and market drivers considered by the IRDS Systems and Architectures (SA) and Application Benchmarking (AB) teams [6] are shown in Table CEQIP-14. Current status of applications in operating temperature ranges above and below 10 K are covered in §**3.3.2** and §**3.3.3**, respectively.

Table CEQIP-14 Matrix of Application Areas and Market Drivers for Cryogenic Semiconductors

Application Areas	Market Drivers			
	Aerospace/Defense	Cloud	Scientific	Medical
Sensors & Sensor Interfaces	G		G	G
ADC/Mixed Signal	G		X	X
Digital Logic	X	P	X	
Memory	X	X, P		

X: important application; G: critical gating application; P: power-sensitive application.

3.3. PRESENT STATUS FOR CRYO-SEMI

3.3.1. TRANSISTOR CHARACTERIZATION AND MODELING

While some semiconductor devices and circuits have been found to function at cryogenic temperatures, design and optimization specifically for cryogenic operation will require further device characterization and model development.

Early work showed that MOSFET models covering a large temperature range from cryogenic to room temperatures need to consider incomplete ionization in addition to the usual expressions for temperature dependence in compact models [386, 387]. As a first step to a full compact model ranging from 4.2 K to 300 K, long channel equations covering the full temperature range were developed and verified against experiment [388].

Transistor characterization was extended over time to more modern technologies, either down to 77 K [389, 390, 391] or to near 4 K [392, 393, 394, 395]. One publication studies behavior at 4 K and at 100 mK and discusses compact modeling [396]. Advanced semiconductor device physics and performance down to 20 K has been reviewed, including fully depleted ultrathin film SOI devices, tri-gate, FinFETs, omega-gate nanowire FETs, and 3D-stacked SiGe nanowire FETs [397].

Research needs for high-energy physics applications presented in 2013 included cryogenic CMOS device models for technology nodes 130 nm and below [398]. Since that time, considerable advances have been made in cryogenic modeling, driven by both digital and sensing applications. Compact models supporting 4 K operation have been developed and validated nanometer scale technologies (160 nm, 40 nm, 28 nm) [396, 399]. It has been experimentally demonstrated for a 40 nm CMOS process that variability increases at cryogenic temperatures, and that the conventionally-used Pelgrom and Croom models for mismatch continue to apply at higher temperatures [395]. Development of unified models that offer accuracy across the deep cryogenic to room temperature range is an area of active research [388, 400, 401]. Reliability studies for cryogenic CMOS have focused on hot carrier degradation, which is generally accepted as the dominant failure mechanism at low temperatures [402]. Nevertheless, BTI stress could play a role at cryogenic conditions, especially in modern CMOS devices, and should be addressed.

3.3.2. APPLICATIONS ≥10 K

3.3.2.1. DRAM

In the late 1980s DRAM at 77 K was evaluated for performance improvement giving the shortest access latencies at the time [403, 404]. More recently, DRAM at 77 K was proposed as a memory system for computers using superconducting electronics [405]. Several commercial DRAM chips have been found to work at temperatures as low as 77 K [406] and their retention behavior between 77 K and 360 K was studied [407].

3.3.3. APPLICATIONS < 10 K

3.3.3.1. SENSORS AND SYSTEMS

Cryogenic multi-channel readout systems using gallium arsenide junction field-effect transistor (GaAs JFET) integrated circuits (ICs) were developed for a multipixel camera for astronomical observation [408].

3.3.3.2. CONTROL OF QUANTUM COMPUTERS

Quantum computing applications of cryogenic CMOS have been under development recently. An initial overview of the needs for cryogenic CMOS is given in [409]. Further work includes FPGA based approaches [410, 411, 412] and circuit designs of low noise amplifiers and oscillators [413, 414].

3.3.3.3. Hybrid Semiconductor – Superconductor Circuits

Hybrid circuits combining semiconductor and superconductor elements operating at cryogenic temperatures have been developed [415, 416, 417]. Van Duzer et al. [418] demonstrated a hybrid RSFQ-CMOS memory operated at 4 K. The 64 Kibit CMOS memory chip was fabricated by TSMC using 65 nm technology. The power dissipation of 12 mW at 1 GHz operation at 4 K is acceptable for small to medium circuits. Konno, et al., [419] improved the design, reducing the power by 54%. Proposed is an even more energy-efficient hybrid memory using superconducting nanocryotron (nTron) drivers and CMOS memory arrays [420].

A superconductive field-effect transistor might be useful as an interface between CMOS and SFQ circuits [421].

Hybrid superconductor-semiconductor digital data links using cryogenic SiGe heterojunction bipolar transistors (HBTs) are being developed. In these links the gain and the corresponding power consumption are distributed over the 4 K to 300 K temperature range for overall optimization of the link figure of merit (energy per bit) [350, 351, 352, 353].

Optoelectronic devices combining superconductors with semiconductors are under development and might have applications in quantum information processing or interfaces between cryogenic electrical and optical communications [422]. Packaging for cryogenic optoelectronics is reviewed in [423]. Proposed are hybrid semiconductor-superconductor neural networks for neuromorphic computing [215].

Superconductive multichip module (S-MCM) technology has been developed to support integration of superconductor and semiconductor circuits [332].

3.4. Active Research Questions for Cryo-Semi

One critical impediment to effective utilization of these cryogenic models is the lack of integration into foundry process design kits. This has historically been a captive effort within the organization performing circuit design activities, and hence has been a barrier to entry for newer design teams.

A review paper has recently been published by IMEP-LAHC comparing the physics and performance of various nanoscale devices at cryogenic temperatures [397]. In addition to research oriented towards the cryogenic utilization of semiconductor devices, observation of cryogenic operation also has general utility in understanding and measuring the physics of carrier transport [424].

4. Quantum Information Processing (QIP)

4.1. Introduction

Quantum computing [425] offers the potential to carry out exponentially more efficient algorithms for several important problem classes [426]. Devices for quantum computing are very different from conventional devices and fine-tuning their characteristics to avoid decoherence while organizing them effectively into scalable architectures has, to date, proved to be a formidable engineering challenge.

Quantum computing takes a very different approach to computation, relying on quantum bits, or qubits. In addition to representing a ‘0’ or ‘1’ as a conventional bit does, a qubit can be in a quantum-mechanical superposition of ‘0’ and ‘1’ at the same time and multiple qubits can be correlated through quantum entanglement. This allows for the use of massive quantum parallelism on a single quantum core. Although quantum mechanics is typically relevant only when describing behavior at the atomic level, it can apply to the behavior of superconducting circuits at extremely low temperatures, typically below 0.1 K.

Quantum annealing, a technique related to adiabatic quantum computing, is a computing approach in which binary variables are represented with qubits, each of which is initialized into a superposition of ‘0’ and ‘1’. The algorithm works by gradually adjusting an arrangement of programmable qubit fields and qubit-to-qubit interactions in a way that encodes an optimization problem defined by a cost function. Qubit states that correspond to a minimization of the cost function are most likely to emerge at the end of the algorithm, at which point the result can be read. Quantum annealing was developed originally to solve NP-hard discrete optimization problems; it has shown promise in optimization and sampling, in particular Boltzmann sampling which is a core technique in machine learning. It can be shown that, at least in the absence of errors, any algorithm of the quantum gate model can be efficiently mapped to quantum annealing [427]; however, achieving error-free operation in these systems may prove challenging [428]. Quantum annealing can also be applied to problems in quantum simulation, by querying the qubit superposition states mid-anneal.

Another approach to quantum computing, the quantum gate model, uses quantum logic gates to achieve a general-purpose quantum computer, essentially creating a quantum von Neumann architecture using quantum gates instead of classical gates [429]. Potential applications include classically challenging computational problems, such as factoring large numbers. Recent

advancements include a theoretical proof that the number of steps needed to solve certain linear algebra problems using parallel quantum circuits is independent of the problem size, whereas the number of steps grows logarithmically with problem size for classical circuits [430]. Further applications include database search, portfolio optimization, machine learning, and combinatorial optimization. This so-called quantum advantage comes from the quantum correlations present in quantum circuits, but not in classical circuits. At a scale of 50 sufficiently coherent qubits, known classical supercomputers cannot simulate quantum computers anymore.

Note that no general physical computing method (including analog and quantum approaches) has yet been clearly demonstrated to be capable of solving NP-hard problems without requiring exponential physical resources (energy or time) to be invested in the physical process performing the computation. The prevailing view among computational complexity theorists [431] is that solving NP-hard problems in polynomial time would require uncovering new physics (i.e., beyond standard quantum mechanics).

4.2. Applications and Market Drivers for QIP

Consumer applications of quantum computing include secure computation, trusted data storage, and efficient applications [432].

Application areas and market drivers considered by the IRDS Systems and Architectures (SA) and Application Benchmarking (AB) teams [6] are shown in Table CEQIP-15 and described in following subsections.

Table CEQIP-15 Matrix of Application Areas and Market Drivers for Quantum Computing (QC)

Application Areas	*Market Drivers*			
		Cloud		
Optimization		G		
Cryptographic codec		X		
Physical system simulation – Quantum simulation		X		
Feature recognition		X		

X: important application; G: critical gating application; P: power-sensitive application.

4.2.1. Optimization

Quantum-annealing processors are designed to solve NP-hard logistics and scheduling problems with applications in industry, military, government, and science. Optimization is a core subproblem in machine learning applications and requires many samples of optimal and near-optimal solutions. These processors are based on superconducting flux qubits that are commercially available from D-Wave Systems [433]. For details, see §**4.3 Present Status for QIP**. About 5 systems have been sold since 2011, representing revenues of about 50 million USD [434]; these systems can also be accessed online in a cloud computing model. Quantum computing approaches that require cryogenic temperatures are likely to need RF signal processing and control as well as digital computation within the cryogenic space.

Quantum algorithms, which could be applied to problems in optimization and machine learning on sufficiently large system are known for gate model quantum systems.

4.2.2. Cryptanalysis

It is conjectured that quantum computers (gate model and/or annealing-based processors) of sufficient size could be used to break current cryptographic protocols (notably RSA encryption). Quantum devices for secure key exchange have been developed that would be necessary to support certain post-RSA cryptographic methods.

4.2.3. Quantum Simulation

Simulators model systems to give information about their behavior. Quantum simulators use quantum effects and are expected to scale better than classical simulators and thus to allow simulation of systems beyond the capabilities of classical simulators [435]. Research and Markets projects that the global simulation software market will grow from USD 6.26 billion in 2017 to USD 13.45 billion by 2022 [436]. Quantum simulation is currently a tiny fraction of the overall simulation market.

Quantum simulators can be classified as analog and digital simulators. In analog simulators, a controlled physical system described by the model to be investigated is built and investigated. In the context of cryoelectronics, this has a long tradition from

the Josephson Junction Arrays studied since the 1990s to modern cavity areas. In digital simulators, the model to be simulated is encoded into a quantum computer algorithm that allows to extract the desired property. The required compilation is often very economical, making these the first expected applications of quantum computers.

Digital quantum simulation can have a major impact on the investigations of molecules and materials, allowing their electronic structure to be simulated even in the case of strong correlations. Techniques to take this to disruptive levels on gate-based quantum computers are known [437, 438, 439] and small instances have been demonstrated [440, 441]. A long-term goal of this activity is the simulation of nitrogenase [442].

Quantum annealing processors have been applied to problems in quantum simulation and materials simulation, e.g., for spin systems [443, 444, 445].

4.2.4. QUANTUM MACHINE LEARNING

Machine learning assisted or enhanced by quantum computing is a relatively new application area under evaluation and development [446, 447, 448]. Known applications contain image recognition for vehicles and healthcare, neural networks, and recommendation systems.

4.3. PRESENT STATUS FOR QIP

While there are few commercial products based on quantum information processing, research and development activity continues to ramp up. A striking development during recent years has been an informal competition to produce circuits for quantum computing with the highest qubit count. The competition shows tantalizing improvement, although the results are announced by press releases without independent verification and benchmark results are not comparable from one qubit type to another.

Quantum communications requires different technological elements such as quantum memory and quantum optical interface. These fundamental elements for quantum communications are still under development. The most matured quantum communication application is quantum key distribution (QKD), which is still limited to relatively short distances. Implementing QKD on a network over practical distances still requires a quantum repeater, which has not been demonstrated to date.

4.3.1. REGIONAL EFFORTS IN QIP

In 2018, Australia, Canada, China, the EU, Germany, the Netherlands, Singapore the UK, and the USA have made separate announcements of additional funding for quantum computing or QIP.

4.3.1.1. CHINA

China is building a new multi-location quantum information laboratory and investing over 100 billion RMB in QIP [449].

4.3.1.2. EUROPE

European quantum technologies roadmap reports have been published since 2005 [450, 451]. The European Commission started a quantum technologies flagship program and will begin selection of research and innovation projects in 2018 [452, 453].

4.3.1.3. JAPAN

Quantum computation in Japan is focused almost entirely on superconducting implementations. Examples of this emphasis include a flagship project within Q-LEAP (2018–2027) funded by MEXT as well as the ERATO project (JST 2016–2021, 1.5 billion yen) for macroscopic quantum machines. The architecture is based on the topological surface code. The goal of this effort is to implement a quantum computer using 100 qubits by 2028. Architectural development is quite advanced in Japan with architectures also being developed for distributed, optical-based and ion-trap based quantum computing systems. Hardware development has started for those approaches where the current focus is on realization of the necessary hardware building blocks.

Japan has also been putting significant effort into quantum annealing systems with AIST being the core research institute involved. The hardware is based on superconducting qubits hardware using double-bonding technique. The current coherence time is on the nanosecond scale, which is three orders of magnitude smaller than the computational time. The software development in this area has focused on mappings between the problem to be solved and the chip design.

The unique situation in Japan for computation is the development of non-quantum unconventional computers. These are often referred as quantum stimulated computers. These are in effect dedicated single purpose machines using conventional technology, and hence there is no quantum coherence involved during the computation. These developments are mainly done in industry sector with government funding. (Example projects: ImPact 2014–2018, 3 billion yen; NEDO 2016–)

Japan has two further strengths in quantum communications research. One is quantum key distribution (QKD) and the second is quantum repeaters. Japan has a long history in QKD development, centered at NICT. After 20 years of fundamental research development, the project has involved industries to run field experiments for a trusted node based QKD network and has now reached an implementation stage where it will be used for commercial purposes. A national project funded by MIC for satellite based QKD has recently started in 2018 which aims to integrate the satellite and trusted node approaches together to explore the

feasibility of physical layer security. (Projects: MIC 2018–, satellite, 5 years; SIP 2018–, commercial development, 2.5 billion yen)

Quantum repeater research has been led by theory development and combined with optical and CQED technologies. The architecture designs are advanced in nature, though their implementation is still in the fundamental research phase. The key technology to be developed is the light matter interface. As the architecture design are well established, a breakthrough would provide a scalable growth for quantum communication networks.

The current implementations within the quantum sensing arena are mostly a quantum enhanced technology. The sensitivity is still within that achievable with conventional approaches, however these new technologies show several real advantages. These technologies are based on variety of quantum systems including nitrogen vacancy (NV) centers in diamond, nuclear spin ensembles, low-dimensional quantum systems and nano- or opto-mechanical systems to highlight a few main examples. Hybridization of these systems is also quite popular to control those systems as well as to generate new applications and physical phenomena. (Projects: MEXT 2015–2019, 1 billion yen; JST-CREST 2016–2023, 4.5 billion yen; a Flagship Q-LEAP 2018–2027)

Quantum sensing beyond the standard quantum limit and current sensitivities is still a challenge to realize. The main obstacle is the noise effect on the probe. Error control mechanisms and applications are currently investigated. Further, the principle of a number of these schemes has been demonstrated; however, it will take more time to realize true sensing prototypes.

4.3.1.4. USA

US gate-type quantum computers lead the world in qubit count, with Google at 72 qubits, IBM at 50, and Intel at 49. For ion trap qubits, IonQ has announced 160 qubits, of which 79 are functional and the others are for storage. These are all US companies, although Intel had a non-US partner. While these systems were top-in-class worldwide when announced, qubit count is widely regarded as having limited value as a metric.

The latest new US activity is the National Quantum Initiative Act (NQI), passed by the US government in December 2018 (1.2 billion USD over 5 years). While the new NQI funding is substantial, overall US government investments are even larger. US industrial investments are difficult to assess exactly, but a speaker in the NQI Senate hearing estimated them to be in the billions but probably less than10 billion USD [454].

The NQI includes the expected funding for science and engineering research, but additionally includes government support for an industry-government consortium intended to increase the efficiency of the human enterprise that will develop quantum computing. The consortium is called the Quantum Economic Development consortium (QED-C) and currently includes over 50 voting member companies and a board including large companies, small companies, and key government agencies. QED-C is like the semiconductor consortium SEMATECH when it was started in the 1980s. QED-C will identify common needs and communicate them to the US government with the intent of better aligning government R&D with industrial needs. These needs include research funding for the most crucial science and technology, yet also include indirect albeit crucial areas such as workforce development, the supply chain, and standards.

While quantum computing is still very much in the research stage, US companies are beginning to offer access via the Internet. Access typically includes software that abstracts the underlying qubit operations into a form more easily learned by programmers—or in some cases into an application-specific framework that offers a “turnkey” solution within a limited problem domain.

4.3.2. QUBITS AND DEVICES FOR QIP

Many types of quantum hardware have been proposed or demonstrated, including trapped ions, cold atoms in optical lattices, liquid and solid-state NMR, photons, quantum dots, superconducting circuits, and NV centers. Reviews include [435, 455, 456].

4.3.2.1. SUPERCONDUCTING QUBITS

Superconducting qubits are formed by thin-film inductors, capacitors and Josephson junctions. These elements allow one to create, control, and read out an artificial atom of macroscopic size [457], [458], [459]. There are many ways for implementing and coupling superconducting qubits [460]. Popular materials used to build superconducting qubits are niobium, aluminum and aluminum oxide [461]. Recent advances include the first demonstration of a voltage-tunable transmon qubit with graphene-based Josephson junctions, although the coherence time needs improvement [462].

Single qubit gates as well as gates between two coupled qubits can be implemented in various ways, where a common method applies microwave pulses tuned to specific frequencies for driving the needed actions [460, 463]. A general issue in the required control and read out processes are the decoherence effects on the qubit. Qubit dehorenence is a sign of interactions between the

qubit and its surrounding environment [507, 464]. To mitigate errors caused by various decoherence sources, including fluctuations of magnetic and electric fields, error correction is applied, e.g., surface codes [465, 466].

On the base of error corrected superconducting qubit devices, higher complexity can be implemented. This is the base for future quantum information processing architectures [429, 467, 468].

4.3.2.2. Quantum Dot Qubits

Quantum dots are nanometer-scale boxes defined in a semiconductor, initially mostly GaAs, currently predominantly SiGe. Quantum dots can hold a precise number of electron spins starting with 0, 1, 2, etc. By the means of electrodes, individual electrons can be controlled. This allows the rotation of electron spin into a superposition of up and down. The technology has the capability to control interactions between two neighboring spins by the Heisenberg exchange interaction [469]. On that base, one- and two-quantum-bit gates for quantum computation using the spin states of coupled single-electron quantum dots can be implemented [470, 471]. Dipole coupling of quantum dots could be demonstrated by a superconducting microwave resonator [472]. This enables the construction of complex processing architectures. Quantum dots are expected to benefit from advanced semiconductor manufacturing processes [473, 474].

4.3.2.3. Topological Qubits

Due to theoretical predictions of improved coherence behavior, topological qubit technologies are currently a field of focused research activities. Topological qubits can be formed by Majorana fermions in topological superconductors [475, 476]. Alternative designs for topologically protected qubits that can be formed from conventional superconductors and Josephson junctions are also being pursued [477].

4.3.2.4. Superconducting Devices

Future quantum computing systems rely on several components grouped around the qubits. In the circuit quantum electrodynamics (cQED) architecture pioneered in 2004 [459], the qubits, which are inherently nonlinear devices, are coupled to linear resonant structures, which can be used for coupling between qubits, as well as the measurement of qubits for transferring readout results to the outside classical world [478]. Commonly these linear resonators are formed from thin-film coplanar waveguide (CPW) resonators, which are straightforward to fabricate with quite low microwave losses [479], although to obtain the proper resonance frequencies for integrating with qubits, these CPW resonators must be rather long, typically several mm, posing a challenge for reducing device areas. Inserting a Josephson junction in such a CPW resonator allows one to tune or modulate its resonance frequency [480]. Alternatively, lumped-element linear resonators offer the ability to form significantly more compact structures for coupling and measuring qubits. However, fabricating lumped-element resonators with sufficiently low microwave loss can be challenging [481]. Fully superconducting indium-bump interconnects have been demonstrated that allow for the three-dimensional integration of quantum circuits without introducing lossy amorphous dielectrics [482].

Measuring the state of a quantum system in general requires more care than detecting a classical bit due to subtleties of the fundamental quantum measurement process. For superconducting qubits in a cQED environment, measurement is typically done with extremely weak microwave signals that must then be amplified by another class of superconducting devices that work very close to the quantum limit [483]. This includes Josephson parametric converters [484], Josephson parametric amplifiers [485, 486] and traveling wave amplifiers [487]. This amplifier-based measurement approach requires strong microwave pump tones for driving the parametric nonlinearity of the amplifier. In order to prevent these pump tones or other noise processes in the amplifier from perturbing the qubit, it is necessary to include significant amounts of non-reciprocal elements, such as microwave isolators or circulators, between the amplifiers and qubits and resonator circuits. Conventional cryogenic microwave isolators and circulators are bulky, magnetic, and difficult to thermalize at millikelvin temperatures, posing a challenge for scaling to large systems. Alternative approaches to forming non-reciprocal elements are currently being developed using superconducting circuitry and parametric active devices [488].

An alternative to amplifier-based qubit measurement involves the use of a microwave photon detector, the Josephson photomultiplier (JPM) [489], which can provide a digital result from qubit measurement at the millikelvin stage of the cryostat [490] for interfacing with a cryogenic digital coprocessor in the low-temperature environment [491]. In addition, because no parametric pump tone is needed, JPMs can be coupled to superconducting qubits and resonators without the need for intervening isolators or circulators [490].

The conventional approach to the control of superconducting qubits and the implementation of quantum gates involves the use of resonant microwave pulses with carefully controlled amplitude and phase. Microwave-based gates have been refined to the point where gate fidelities exceed 99.9% [466, 492], exceeding the fault-tolerant threshold for implementing quantum error correction. However, the generation of microwave signals for qubit gates requires a significant hardware overhead of room-temperature equipment outside of the cryostat, including microwave sources, arbitrary waveform generators, mixers, and amplifiers. An alternative approach currently being explored involves the use of SFQ-based superconducting digital electronics

to drive quantum gates using resonant trains of SFQ pulses [493, 494, 495], thus greatly reducing the requirements for room-temperature hardware and moving much of the control elements into the low-temperature environment [491].

4.3.3. ANNEALING-BASED QUANTUM COMPUTING (QA)

Quantum-annealing processors based on superconducting flux qubits have been developed by and are commercially available from D-Wave Systems [9, 433, 496, 497, 498]. The D-Wave TwoX includes a superconducting chip with 128,000 Josephson junctions, of which 75% are in classical SFQ digital control circuitry to program the processor and read out the results and the remainder are either directly in qubits or in the analog coupling elements that allow qubits to interact in a programmable way. Benchmarking results remain controversial.

Quantum annealing algorithms are reviewed in [499] and evidence for advantages are presented in [500]. A method to factorize integers using quantum annealing was recently developed and demonstrated using the D-Wave 2000Q [501].

4.3.4. GATE-BASED QUANTUM COMPUTING (QC)

Quantum architectures based on quantum gates and circuits are in active research. Several research groups are working to develop superconducting qubits with sufficiently long quantum-coherence times and scalable architectures [502].

The publications of Shor's algorithm providing an exponential speed-up for factorizing a number [503] and Grover's algorithm providing polynomial speedup for unstructured search [504] gave theoretical grounding to the concept of using quantum mechanics to enhance computing performance. In the following years a variety of physical realization methods for quantum computing have been proposed. Some of these methods relay on cryogenics and superconductivity. The superconducting qubit technology is currently one of the most promising methods. However, it has been shown that other technologies, such as solid-state spin quantum dots and topological qubits may also rely on superconducting elements. On the side of the technologies used for information processing devices, a variety of superconducting devices are required to build up quantum computing systems. These are namely resonators, amplifiers and non-reciprocal devices.

Research on gate-based quantum devices is ongoing at numerous universities, governmental facilities, and companies (see Table CEQIP-16). Industry has started to integrate these devices and to scale up towards computing systems.

Table CEQIP-16 Example Companies in Gate-based Quantum Computing Using Superconductors

Company	*Country*	*Qubit Technology*	*References*
Alibaba	China	Superconducting	[505]
Google	USA	Superconducting	[506]
IBM	USA	Superconducting	[440, 507, 508, 509]
Intel	USA	Superconducting, Spin quantum dots	[510]
Microsoft	USA	Topological	[511]
Rigetti	USA	Superconducting	[512]

4.3.5. QUANTUM COMMUNICATION

Quantum communication technologically ranges from point-to-point quantum key distribution to fully quantum networks [513, 514]. Quantum communication involves the generation and use of quantum states and resources for communication protocols and is inherently distributed in nature with separation between nodes ranging from micrometer to planetary scales. Its main applications are in provably secure communication, long-term secure storage, cloud computing and other cryptography-related tasks, as well as in the future, a secure "quantum web" distributing quantum resources like entanglement, nonlocality, randomness and connecting remote devices and systems. The main role of cryoelectronics in this fields is in the area of single photon detectors based on superconducting nanowires [515]. A cryogenic microwave-based quantum communication scheme has been proposed and is being researched in the EU [516].

Quantum key distribution, which is a quantum communication protocol for two parties, involves a sender (Alice) and a receiver (Bob), who share one-time pad material (a shared classical random bit string). The simplest implementation requires only the superposition state of a photonic qubit with no entanglement required at all. This advanced technology has reached the stage where successful field trials have been performed and left running for several years. Future applications will be determined by the distance at which secure keys can be established. Current QKD implementations have a limitation on both the distance and

rate at which shared keys can be established, for instance the best performance currently is ~ 1 Mbit/s over 50 km. As the communication distance increases further, the rate rapidly decreases, and a few hundred kilometers is considered the limit. To go farther and maintain the level of key security, the current QKD implementations require quantum repeaters to be added, which is also the key technology needed to distribute quantum entanglement over long distances. Technologies for quantum communication relevant to current quantum information technology developments include quantum key distribution, quantum interconnects, and quantum repeaters; each covered in following sub-sections.

4.3.5.1. QUANTUM KEY DISTRIBUTION

Quantum key distribution has moved from the research arena now to the product development phase where market alignment is highly essential. Further technology developments to higher generation rates over long distance are important and necessary. For long distance QKD systems, there are two directions currently being investigated: trusted relay optical-fiber-based networks and satellite communications which could be combined in the future. These technologies are in principle only based on the superposition of quantum states and do not rely on quantum entanglement. The challenge is to go beyond 10 Mbit/s for 50 km, and 1 kbit/s for satellite communications. To eliminate trusted nodes, which inherently severely compromise key security, the move to quantum repeater technology is needed.

Quantum key distribution utilizing quantum repeaters naturally allows extending the communication distance significantly without compromising key security. The challenge is to develop the key technology necessary in quantum repeaters. Limiting the use of quantum repeaters to only QKD allows elimination of several components including technologically difficult quantum memories with long storage times. Another possible quantum communication approach including QKD is a quantum sneakernet, a system based on physical movement of quantum memory [517]. This is a quantum-memory-based quantum communication system whereas quantum repeaters are communication-channel-based system. Quantum sneakernets require an extremely long-lived quantum memory with coherence time sufficient for a quantum signal to be physically delivered from the sender to the receiver. This necessitates either a fault-tolerant quantum error corrected qubit (composed of many physical qubits) or an exceptionally long coherence for the quantum memory (possibly weeks).

4.3.5.2. QUANTUM REPEATERS

Quantum repeaters are a core technology for quantum communication. Any direct quantum communication between two parties has a distance limitation as the success rate decreases exponentially with the communication distance. To overcome this fundamental limitation, waystations are required in the communication channel, similar to amplifiers in classical communication channels. However, unlike amplifiers used for classical signals, it is impossible to amplify a quantum signal due to the no-cloning theorem. Hence quantum repeaters work by generating and then swapping entanglement between waystations to extend the range of quantum correlations. Quantum repeaters allows the generation of entanglement over the entire communication network. The deterioration of the fidelity of entanglement can be recovered by distillation (purification) of the quantum state.

Quantum relays are a precursor technology to full quantum repeaters. They are in a sense quantum pre-repeaters or primitive quantum repeaters with limited functionality. It does not show the scalability that a true quantum repeater-based network would exhibit (polynomial resource usage with the quality of the entangled resource not scaling exponentially with overall communication distance) but it can scale polynomially if the quantum memory has an infinite coherence time. Typical technological requirements for the relays are single photon sources, single photon detectors, quantum memories, and an interface between the matter-based qubit and photon. The requirements include optical cavity developments, control of matter qubits with optical transitions as such as NV centers in diamond, and lossless fiber-cavity coupling. Quantum relays and quantum repeaters share many of the basic hardware technology components, though the architectures of the communication systems are vastly different.

Quantum repeaters need to have at most a polynomial scaling in terms of resources required while at the same time establishing entangled states whose quality does not scale down exponentially with the number of repeater nodes in the network. A quantum repeater system consists of three distinct operations: entanglement distribution, entanglement swapping, and entanglement distillation (purification) and error correction. Although quantum repeaters employ error correction, the implementation is much simpler than in quantum computation and fault tolerance is not necessary.

4.3.5.3. QUANTUM INTERCONNECTS

Quantum interconnects are components of quantum communications systems used to transport entanglement between quantum devices. They can be implemented on chip and between chips for short distances that do not require quantum repeaters. In particular, they can be used to fundamentally change the connectivity for quantum adiabatic computation, quantum annealing, and quantum simulation, providing significant benefits in this era of noisy intermediate-scale quantum (NISQ) computing [518]. More importantly, they allow in the longer term to perform distributed quantum computation.

The quantum internet is a network of quantum computers connected by quantum communication channels. On the quantum internet, quantum computers are connected coherently, and so one can distribute quantum correlations and consume them in a

global fashion. Such a network of coherently connected quantum computers would allow global distribution and consumption of quantum correlations.

4.3.6. QUANTUM SENSING

Quantum sensing is the use of a quantum system, quantum properties, or quantum phenomena to perform a measurement of a physical quantity [10]. Quantum sensors enable measuring a physical quantity to a precision beyond the quantum standard limit (shot noise limit) possible with classical technology. Intermediate sensing applications to exploit quantum effects are also possible.

Quantum-enabled sensing that cannot achieve sensitivities beyond the standard quantum limit (SQL) nonetheless can provide advantages in comparison to conventional sensing by manipulating a sensor's quantum nature. Examples include functional NMR and non-classical light spectroscopy and sensing. It is the most relevant approach for commercial development at the current stage.

Quantum sensing beyond the SQL requires the manipulation of quantum information on the probe state. Hence it requires control of quantum-phase information and the ability to read it out. One of the most advanced technologies utilizes quantum correlated light. Matter-based sensors are under development using NV centers in diamond and hybrid quantum systems.

Quantum imaging is based on similar technology; however, this focuses on a different aspect of sensing. Using quantum-mechanically correlated light, imaging is possible with limited probing of the object under consideration. Important applications are in medical and biological applications where avoiding damage caused by the sensing is regarded as a vital factor.

Quantum global sensing uses quantum coherence to measure large-scale global properties with high accuracy. Application examples include natural-resource searching and crustal-movement imaging. The core technologies required for global sensing are quantum sensors combined with quantum repeater networks.

4.4. BENCHMARKING AND METRICS FOR QIP

Quantum information processing is currently in an exploratory stage of engineering, and there is widespread consensus that the development of many different technologies remains necessary to meet the long-term expectation of fault-tolerant, universal quantum devices. Recent experimental demonstrations have passed significant milestones in the design, fabrication, and operation of small-scale quantum computing devices. These advances underscore the need to track technical progress in this field and to forecast future developments in quantum engineering research. Such insights are expected to be necessary to monitor the overall growth in sophistication of quantum engineering. A five-layer system to that end has been proposed in Germany [455].

Methods for tracking the development of quantum information processing are under development by the research community [519, 520, 521, 522, 523, 524]. Those methods seek to evaluate the salient features and behaviors of quantum information devices as well as the expected usage. Metrics for quantum information processing are intended to be representative of device growth and device performance, whereas benchmarks define the methods by which these metrics are evaluated. Notably, metrics for quantum information processing may be defined at different levels of abstraction including the physical, logical, and system levels, and these metrics represent conventional concerns for information processing as well as concerns that are unique to quantum information. The IEEE has engaged in several efforts to build a structured community for discussing these points and building scientific consensus [525].

Presently, the community is debating a framework for metrics and benchmarks designed around the expected use cases and technology layers for quantum computing devices. In this description, use cases represent a category that identifies a designed purpose for a quantum computing device or system. Common examples include noisy, intermediate-scale quantum devices, quantum annealers, and quantum simulators. The technology layers identify the levels of design complexity in a quantum computing device or system. These layers include the low-level physical registers storing quantum states, the integrated control systems expressing quantum operations, and the system-level performance concerns for specific applications.

Existing metrics for quantum devices characterize the noise in the physical register and the errors observed from low-level physical gate operations. The aggregate effects of these two sources of errors also has been proposed for evaluating device reliability but outstanding questions remain on how to connect these metrics to application performance. In the context of application performance, time-to-solution has been used as a device-agnostic method of comparison across solution methods. However, current devices are too small to enable broad ranges in problem evaluation and the comparison of quantum technologies against conventional devices is complicated by vastly different levels of technology maturity.

4.5. ACTIVE RESEARCH QUESTIONS FOR QIP

Superconducting quantum computing requires further development, lower error rates, and scale (number of qubits) to clearly demonstrate the improved performance of important applications. Integrated circuit technologies are required that are scalable

and address the special needs of quantum circuits [526]. More work is needed to explore potential applications for quantum algorithms and to develop suitable quantum processor architectures. As mentioned above, the integration of superconducting digital electronics with superconducting qubits for control and readout holds promise for scaling to significantly larger systems than is possible with present state-of-the-art approaches [491].

Table CEQIP-17 Difficult Challenges for QIP

Near-Term Challenges: 2018-2025	*Summary of Issues and Opportunities*
Physical qubits	Design and fabrication of qubit devices with enhanced qubit coherence times and gate fidelities
Logical qubits	Implementation of fully error-corrected logical qubits and protected gate operations
Readout of qubits	Development of scalable, cryogenic qubit readout hardware
Interconnects, cryogenic to room temperature	Development of low thermal conductance and high bandwidth interconnects between different temperature stages of cryogenic- and room-temperature electronics

5. CHALLENGES

The top near term challenges for superconductor electronics (SCE) and quantum information processing (QIP) are given in the table below. These are a very high-level summary of challenges that the industry needs to address for this IFT.

Table CEQIP-18 Difficult Challenges Summary

Near-Term Challenges: 2018-2025	*Summary of Issues and Opportunities*
SCE: Integrated circuit fabrication	Foundries for commercial production now process 200 mm or smaller wafers using equipment lacking state-of-the-art capability. Achieving the yield and throughput for large-scale applications will require process improvements and, possibly, a move to 300 mm wafers. Planarization and thickness control is challenging in stacks of multiple superconductor layers when the layer thicknesses remain the same, rather than increasing with layer number as in CMOS back-end processes.
SCE: Device variability	Variation in device parameters reduces the operating margins of circuits. Needed is better process control, better device designs, or circuit designs that tolerate or compensate for device variability.
SCE: High critical current density junctions (J_c > 100 μA/μm^2)	The AlO_x barrier in Josephson junctions with J_c = 100 μA/μm^2 is now approximately 1 nm thick. Thinner barriers increase J_c, allowing smaller and faster JJs. For J_c > 500 μA/μm^2 the sub-gap resistance can be sufficiently low to eliminate the need for shunt resistors. Uniformity control will be challenging as defects typically dominate conduction through thinner barrier layers and thickness control is also difficult. Materials and process development is needed to improve uniformity and control of devices with high J_c.
SCE: Electronic design automation (EDA) tools	EDA tools for CMOS are not adequate for SCE. Inductance is critical in superconducting circuits and connecting wires must have inductance values within a specified range. Circuit simulators and timing analysis must be modified for pulse-based logic. Flux trapping analysis—both for trapping probability and the coupling of trapped flux in moats to circuits—is required, while analysis of the coupling of bias current and ground plane return currents to circuit structures are also important and difficult at chip level.
SCE: Packaging	Operation at cryogenic temperatures requires different materials, packaging, testing, and cooling systems, much of which will require new development. State-of-the art systems package a few superconductor ICs in a commercial cryostat. Scaling up to systems with higher complexity chips and multi-chip modules will require further reduction of power consumption by all components. Josephson junctions are extremely sensitive to magnetic fields and require shielding, which becomes more challenging as system volumes grow.
QIP: Qubit, physical	Identify qubit technology with the best overall characteristics for use in quantum computing.
QIP: Qubit, logical	Demonstrate logical qubits and error correction sufficient for scaling to larger systems.

6. SUMMARY

This IRDS chapter surveys Cryogenic Electronics (sections 2 and 3), and Quantum Information Processing (section 4), which include alternatives to conventional CMOS technologies. Although novel functionalities and applications have been a primary objective of cryogenic electronics and quantum information processing, high performance at low-power consumption could become important as well.

- ***SUPERCONDUCTOR ELECTRONICS (SCE)***

Logic families continue to develop with very different characteristics. The number of Josephson junction switching elements in a circuit is approaching 1 million.

Cryogenic RAM with sufficient density and capacity continues to be the most important need for superconductor electronics. Memory based on logic-style Josephson junctions is most developed but has not yet achieved 1 Mibit capacity.

SCE technology is ready to begin roadmapping for digital computing applications.

- ***CRYOGENIC SEMICONDUCTOR ELECTRONICS (CRYO-SEMI)***

Monitoring of applications, drivers, and technologies will continue. No areas seem ready for roadmapping at this time.

- ***QUANTUM INFORMATION PROCESSING (QIP)***

Monitoring of applications, drivers, and technologies will continue. No areas seem ready for roadmapping at this time, although some are close.

7. ENDNOTES/REFERENCES

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