INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

2018 UPDATE

BEYOND CMOS

Table of Contents

List of Figures

List of Tables

Link to Beyond CMOS Tables File

ACKNOWLEDGMENTS

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Ferdinand Peper
Shriram Ramanathan
Mingyi Rao
Shashi Paul
Titash Rakshit
Arijit Raychowdhury
Horst Rogalla
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Shintaro Sato
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BEYOND CMOS

1. INTRODUCTION

1.1. SCOPE OF BEYOND-CMOS FOCUS TEAM

Dimensional and functional scaling[1] of CMOS is driving information processing[2] technology into a broadening spectrum of new applications. Scaling has enabled many of these applications through increased performance and complexity. As dimensional scaling of CMOS will eventually approach fundamental limits, several new information processing devices and microarchitectures for both existing and new functions are being explored to extend the historical integrated circuit scaling cadence. This is driving interest in new devices for information processing and memory, new technologies for heterogeneous integration of multiple functions, and new paradigms for system architecture. This chapter, therefore, provides an IRDS perspective on emerging research device technologies and serves as a bridge between conventional CMOS and the realm of nanoelectronics beyond the end of CMOS scaling. (Material challenges related to emerging research devices are addressed in a complementary 2017 chapter entitled *Emerging Research Materials*.)

An overarching goal of this chapter is to survey, assess, and catalog viable emerging devices and novel architectures for their long-range potential and technological maturity and to identify the scientific/technological challenges gating their acceptance by the semiconductor industry as having acceptable risk for further development. This chapter also surveys new applications of emerging technologies, e.g., hardware security, cryogenic electronics.

This goal is accomplished by addressing two technology-defining domains: 1) extending the functionality of the CMOS platform via heterogeneous integration of new technologies ("More Moore"), and 2) stimulating invention of new information processing paradigms ("Beyond CMOS"). The relationship between these domains is schematically illustrated in Figure BC1.1. Novel computing paradigms and application pulls (e.g., big data, IoT, artificial intelligence, autonomous systems, exascale computing) introduce higher performance and efficiency requirements, which is increasingly difficult for the saturating More Moore technologies to fulfill. Beyond-CMOS technologies may provide the required devices, processes, and architectures for the new era of computing.

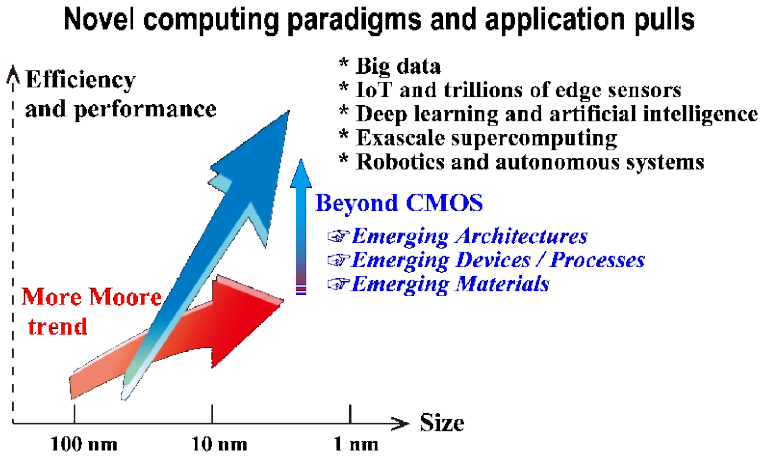


Figure BC1.1 Relationship of More Moore, Beyond CMOS, and Novel Computing Paradigms and Applications (Courtesy of Japan beyond-CMOS group)

The chapter is intended to provide an objective, informative resource for the constituent nanoelectronics communities pursuing: 1) research, 2) tool development, 3) funding support, and 4) investment. These communities include universities, research

[1] *Functional Scaling: Suppose that a system has been realized to execute a specific function in a given, currently available, technology. We say that system has been functionally scaled if the system is realized in an alternate technology such that it performs the identical function as the original system and offers improvements in at least one of size, power, speed, or cost, and does not degrade in any of the other metrics.*

[2] *Information processing refers to the input, transmission, storage, manipulation or processing, and output of data. The scope of the BC Chapter is restricted to data or information manipulation, transmission, and storage.*

institutes, and industrial research laboratories; tool suppliers; research funding agencies; and the semiconductor industry. The potential and maturity of each emerging research device and architecture technology are reviewed and assessed to identify the most important scientific and technological challenges that must be overcome for a candidate device or architecture to become a viable approach.

The chapter is divided into five sections: 1) memory devices, 2) information processing or logic devices, 3) emerging application areas, 4) emerging device-architecture interaction, and 5) assessment. Some detail is provided for each entry regarding operation principles, advantages, technical challenges, maturity, and current and projected performance. The chapter also discusses applications and architectural focus combining emerging research devices offering specialized, unique functions as heterogeneous core processors integrated with a CMOS platform technology. This represents the nearer term focus of the chapter, with the longer-term focus remaining on discovery of an alternate information processing technology beyond digital CMOS.

The technology entries in this chapter adopt the main entries of the International Technology Roadmap of Semiconductors (ITRS) Emerging Research Devices (ERD) chapter. The memory device section is expanded to include a new technology entry: “massive storage devices”. The previous “novel STTRAM devices” entry has been modified to “novel magnetic memory” to cover a broader range of devices. The “macromolecular (polymer) memory”, which was previously included in the category of ReRAM, is listed as a separate entry. “ReRAM” continues to be extensively tracked with simplified categorization. The logic device section categorizes technology entries as CMOS extension, charge-based beyond-CMOS devices, and non-charge-based beyond-CMOS devices.

1.2. Difficult Challenges

1.2.1. Introduction

The semiconductor industry is facing some difficult challenges related to extending integrated circuit technology to new applications and to beyond the end of CMOS dimensional scaling. One class relates to propelling CMOS beyond its ultimate density and functionality by integrating a new high-speed, high-density, and low-power memory technology onto the CMOS platform. Another class is to extend CMOS scaling with alternative channel materials. The third class is information processing technologies substantially beyond those attainable by CMOS using an innovative combination of new devices, interconnect, and architectural approaches for extending CMOS and eventually inventing a new information processing platform technology. The fourth class is to extend ultimately scaled CMOS as a platform technology into new domains of functionalities and application, also known as “more than Moore”. The fifth class is to bridge the gap between novel devices and unconventional architectures and computing paradigms. These difficult challenges are summarized in Table BC1.1.

1.2.2. Device Technologies

Difficult challenges gating development of beyond-CMOS devices include those related to memory technologies, information processing or logic devices, and heterogeneous integration of multi-functional components, a.k.a. More-than-Moore (MtM) or Functional Diversification.

One challenge is the need of a new memory technology that combines the best features of current memories in a fabrication technology compatible with CMOS process flow and that can be scaled beyond the present limits of SRAM and FLASH. This would provide a memory device fabrication technology required for both stand-alone and embedded memory applications. The ability of an MPU to execute programs is limited by interaction between the processor and the memory, and scaling does not automatically solve this problem. The current evolutionary solution is to increase MPU cache memory, thereby increasing the floor space that SRAM occupies on an MPU chip. This trend eventually leads to a decrease of the net information throughput. In addition to auxiliary circuitry to maintain stored data, volatility of semiconductor memory requires external storage media with slow access (e.g., magnetic hard drives, optical CD, etc.). Therefore, development of electrically accessible non-volatile memory with high speed and high density would initiate a revolution in computer architecture. This development would provide a significant increase in information throughput beyond the traditional benefits of scaling when fully realized for nanoscale CMOS devices.

Table BC1.1 Beyond CMOS Difficult Challenges

Difficult Challenges	*Summary of Issues and Opportunities*
Scale high-speed, dense, embeddable, volatile/non-volatile memory technologies to replace SRAM and FLASH in appropriate applications.	The scaling limits of SRAM and FLASH in 2D are driving the need for new memory technologies to replace SRAM and FLASH memories. Identify the most promising technical approach(es) to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and non-volatile memories. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified and addressed early in the technology development.
Extend CMOS scaling	Develop new materials to replace silicon (or III-V, Ge) as alternate channel and source/drain to increase the saturation velocity and to further reduce V_{dd} and power dissipation in MOSFETs while minimizing leakage currents Develop means to control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Accommodate the heterogeneous integration of dissimilar materials. The desired material/device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified and addressed early in this development.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS.	Invent and reduce to practice a new information processing technology to replace CMOS as the performance driver. Ensure that a new information processing technology has compatible memory technologies and interconnect solutions. A new information processing technology must be compatible with a system architecture that can fully utilize the new device. Non-binary data representations or non-Boolean logic may be required to employ a new device for information processing, which will drive the need for new system architectures. Bridge the gap that exists between materials behaviors and device functions. Accommodate the heterogeneous integration of dissimilar materials. Reliability issues should be identified and addressed early in the technology development.
Extend ultimately scaled CMOS as a platform technology into new domains of functionalities and application (“more than Moore, MtM”).	Discover and reduce to practice new device technologies and primitive-level architecture to provide special purpose optimized functional cores (e.g., accelerator functions) heterogeneously integrable with CMOS. Provide added value by incorporating functionalities that do not necessarily scale according to “Moore’s Law”. Heterogeneous integration of digital *and* non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields, such as communication, automotive, environmental control, healthcare, security, and entertainment.
Bridge the gap between novel devices and unconventional architectures and computing paradigms.	Identify suitable opportunities in unconventional architectures and computing paradigms that can utilize unique characteristics of novel devices. Identify emerging devices that can implement computing functions and architectures more efficiently than CMOS and Boolean logic.

A related challenge is to sustain scaling of CMOS logic technology. One approach to continuing performance gains as CMOS scaling matures in the next decade is to replace the strained silicon MOSFET channel (and the source/drain) with an alternate material offering a higher potential quasi-ballistic-carrier velocity and higher mobility than strained silicon. Candidate materials include strained Ge, SiGe, a variety of III-V compound semiconductors, and carbon materials. Introduction of non-silicon materials into the channel and source/drain regions of an otherwise silicon MOSFET (i.e., onto a silicon substrate) is fraught with several very difficult challenges. These challenges include heterogeneous fabrication of high-quality (i.e., defect free) channel and source/drain materials on non-lattice matched silicon, minimization of band-to-band tunneling in narrow bandgap channel materials, elimination of Fermi level pinning in the channel/gate dielectric interface, and fabrication of high-κ gate dielectrics on the passivated channel materials. Additional challenges are to sustain the required reduction in leakage currents and power dissipation in these ultimately scaled CMOS gates and to introduce these new materials into the MOSFET while simultaneously minimizing the increasing variations in critical dimensions and statistical fluctuations in the channel (source/drain) doping concentrations.

The industry is now addressing the increasing importance of a new trend of functional diversification, where added value to devices is provided by incorporating functionalities that do not necessarily scale according to "Moore's Law". In this chapter, an "Emerging Application Areas" section covers unconventional applications of existing and novel technologies. Two topics, emerging devices for hardware security and cryogenic electronics, are discussed in this section.

A longer-term challenge is invention and reduction to practice of a manufacturable information processing technology addressing "beyond CMOS" applications. For example, emerging research devices might be used to realize special purpose processor cores that could be integrated with multiple CMOS CPU cores to obtain performance advantages. These new special purpose cores may provide a particular system function much more efficiently than a digital CMOS block, or they may offer a uniquely new function not available in a CMOS-based approach. Solutions to this challenge beyond the end of CMOS scaling may also lead to new opportunities for such an emerging research device technology to eventually replace the CMOS gate as a new information processing primitive element. A new information processing technology must also be compatible with a system architecture that can fully utilize the new device. A non-binary data representation and non-Boolean logic may be required to employ a new device for information processing. These requirements will drive the need for new system architectures. The requirements and opportunities correlating emerging devices and architectures are discussed in the "Emerging Device-Architecture Interaction" section.

1.2.3. MATERIALS TECHNOLOGIES

The most difficult challenge for Beyond CMOS is to deliver materials with controlled properties that will enable operation of emerging research devices in high density at the nanometer scale. To improve control of material properties for high-density devices, research on materials synthesis must be integrated with work on new and improved metrology and modeling. These important objectives are addressed in the "2017 Emerging Research Materials" chapter.

1.3. NANO-INFORMATION PROCESSING TAXONOMY

Information processing systems to accomplish a specific function, in general, require several different interactive layers of technology. One comprehensive top-down list of these layers begins with the required application or system function, leading to system architecture, micro- or nano-architecture, circuits, devices, and materials. A different bottom-up representation of this hierarchy begins with the lowest physical layer represented by a computational state variable and ends with the highest layer represented by the architecture. In this representation focused on generic information processing at the device/circuit level, a fundamental unit of information (e.g., a bit) is represented by a computational state variable, for example, the position of a bead in the ancient abacus calculator or the charge (or voltage) state of a node capacitance in CMOS logic. The electronic charge as a binary computational state variable serves as the foundation for the von Neumann computational system architecture. A device provides the physical means of representing and manipulating a computational state variable among its two or more allowed discrete states. Eventually, device concepts may transition from simple binary switches to devices with more complex information processing functionality, perhaps with multiple fan-in and fan-out. The device is a physical structure resulting from the assemblage of a variety of materials possessing certain desired properties obtained through exercising a set of fabrication processes. An important layer, therefore, encompasses the various materials and processes necessary to fabricate the required device structure, which is a focus of the "Beyond CMOS (BC)" chapter. The data representation is how the computational state variable is encoded by the assemblage of devices to process the bits or data. Two of the most common examples of data representation are binary digital and continuous or analog signal. This layer is within the scope of the BC chapter. The architecture layer encompasses three subclasses of this taxonomy: 1) nano-architecture or the physical arrangement or assemblage of devices to form higher level functional primitives to represent and execute a computational model, 2) the computational model that describes the algorithm by which information is processed using the primitives, e.g., logic, arithmetic, memory, cellular nonlinear network (CNN), and 3) the system-level architecture that describes the conceptual structure and functional behavior of the system exercising the computational model.

2. EMERGING MEMORY DEVICES

The emerging research memory technologies tabulated in this section are a representative sample of published research efforts (circa 2015 – 2017) describing alternative approaches to established memory technologies.[3] The scope of this section also includes updated subsections addressing the "Select Device" required for a crossbar memory application and an updated treatment of "Storage Class Memory" (including Solid State Disks).

[3] *Including a particular approach in this section does not in any way constitute advocacy or endorsement. Conversely, not including a particular concept in this section does not in any way constitute rejection of that approach. This listing does point out that existing research efforts are exploring a variety of basic memory mechanisms.*

Figure BC2.1 is a taxonomy of the prototypical and emerging memory technologies. An overarching theme is the need to monolithically integrate each of these memory options onto a CMOS technology platform in a seamless manner. Fabrication technologies are sought that are modifications of or additions to established CMOS platform technologies. A goal is to provide the end user with a device that behaves similarly to the familiar silicon memory chip.

This memory portion of this section is organized around a set of eight technology entries shown in the column headers of Table BC2.1. These entries were selected using a systematic survey of the literature to determine areas of greatest worldwide research activity. Each technology entry listed has several sub-categories of devices that are grouped together to simplify the discussion. Key parameters associated with the technologies are listed in the table. For each parameter, two values for performance are given: 1) theoretically predicted performance values based on calculations and early experimental demonstrations, 2) up-to-date experimental values of these performance parameters reported in the cited technical references.

The tables have been extensively footnoted, and details may be found in the indicated references. The text associated with the table gives a brief summary of the operating principles of each device and significant scientific and technological issues, not captured in the table, but which must be resolved to demonstrate feasibility.

The purpose of many memory systems is to store massive amounts of data, and therefore memory capacity (or memory density) is one of the most important system parameters. In a typical memory system, the memory cells are connected to form a two-dimensional array, and it is essential to consider the performance of memory cells in the context of this array architecture. A memory cell in such an array can be viewed as being composed of two fundamental components: the 'storage node' and the 'select device', the latter of which allows a given memory cell in an array to be addressed for read or write. Both components impact scaling limits for memory. For several emerging resistance-based memories, the storage node can, in principle, be scaled down below 10 nm,[1] and the memory density will be limited by the select device. Thus, the select device represents a serious bottleneck for ReRAM scaling to 10 nm and beyond. Planar transistors (e.g. FET or BJT) are typically used as select devices. In a two-dimensional layout using in-plane select FETs the cell layout area is Acell=(6-8)F^2. In order to reach the highest possible 2-D memory density of $4F^2$, a vertical select transistor can be used. Table BC2.3 shows several examples of vertical transistor approaches currently being pursued for select devices. Another approach to obtaining a select device with a small footprint is a two-terminal nonlinear device, e.g. a diode, either as a separate device or a strong nonlinearity intrinsic to a resistive memory element. Table BC2.4 displays benchmark parameters required for a 2-terminal select device, and Table BC2.5 summarizes the operating parameters for several candidate 2-terminal select devices.

Storage-class memory (SCM) describes a device category that combines the benefits of solid-state memory, such as high performance and robustness, with the archival capabilities and low cost per bit of conventional hard-disk magnetic storage. Such a device requires a non-volatile memory technology that can be manufactured at a very low cost per bit. Table BC2.6 lists a representative set of target specifications for SCM devices and systems, which are compared against benchmark parameters offered by existing technologies (HDD, NAND Flash, and DRAM). Two columns are shown, one for the slower S-class Storage Class Memory, and one for fast M-class SCM, as described in Section 2.4. These numbers describe the performance characteristics that will likely be required from one or more emerging memory devices in order to enable the emerging application space of Storage Class Memory. Table BC2.7 illustrates the potential for storage-class memory applications of a number of prototypical memory technologies (Table BC2.1) and emerging research memory candidates (Table BC2.2). The table shows qualitative assessments across a variety of device characteristics, based on the target system parameters from Table BC2.6. These tables are discussed in more detail in Section 2.4.

Table BC2.1 Emerging Research Memory Devices—Demonstrated and Projected Parameters

Table BC2.2 Emerging Research Memory Devices—Redox RAM Demonstrated and Projected Parameters

2.1. MEMORY TAXONOMY

Figure BC2.1 provides a simple visual method of categorizing memory technologies. At the highest level, memory technologies are separated by the ability to retain data without power. Non-volatile memory offers essential use advantages, and the degree to which non-volatility exists is measured in terms of the length of time that data can be expected to be retained. Volatile memories also have a characteristic retention time that can vary from milliseconds to (for practical purposes) the length of time that power remains on. Non-volatile memory technologies are further categorized by their maturity. Flash memory is considered the baseline non-volatile memory because it is highly mature, well optimized, and has a significant commercial presence. Flash memory is the benchmark against which prototypical and emerging non-volatile memory technologies are measured. Prototypical memory technologies are at a point of maturity where they are commercially available (generally for niche applications), and have a large

scientific, technological, and systems knowledge base available in the literature. The focus of this section is Emerging Memory Technologies. These are the least mature memory technologies in Figure BC2.1, but they have been shown to offer significant potential benefits if various scientific and technological hurdles can be overcome. This section provides an overview of these emerging technologies, their potential benefits, and the key research challenges that will allow them to become viable commercial technologies.

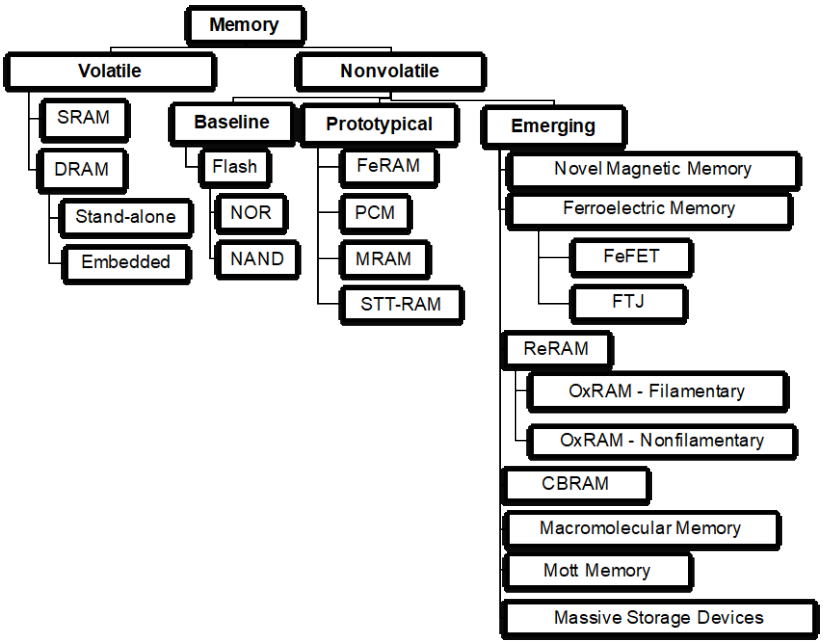


Figure BC2.1 Taxonomy of Emerging Memory Devices

2.2. EMERGING MEMORY DEVICES

2.2.1. NOVEL MAGNETIC MEMORY

Spin-transfer torque RAM (STT-RAM) is covered in the More Moore Chapter of IRDS since this memory had matured and become commercially available. However, there has been recent progress in emerging memory devices which utilize novel magnetic mechanisms, and in response a completely updated section covering this topic has been added to Beyond CMOS. There has been an evolution in thinking, as to what should be the target magneto-electric devices for CMOS 'plug-in' replacement logic and memory. The earliest magneto-electric devices were based on a magnetic tunnel junction structure[2,3] which consists of two ferromagnetic (FM) layers separated by a non-magnetic insulator where the device resistance is determined by the relative orientation of the magnetization of the two FM layers. The magnetization of the free layer is exchange coupled to the Cr_2O_3 (or other magneto-electric) interface magnetization. A bias voltage applied across a magneto-electric layer, like chromia Cr_2O_3, reverses the interface magnetization, which in turn switches the magnetization of the free layer[4, 5, 6]. A non-magnetic Hall bar on top of magneto-electric chromia has now been demonstrated as a readout mechanism for a memory state via the anomalous Hall effect.[7,8]

More recent attention[6,9,10,11,12] has shifted to the magneto-electric transistor (the ME-spinFET). Magneto-electric transistor schemes are based on polarization of the semiconductor channel, by the boundary polarization of the magneto-electric gate. The advantage to the magneto-electric field effect transistor is that such schemes avoid the complexity and detrimental switching energetics associated with exchange-coupled ferromagnets. Spintronic devices based solely on the switching of a magneto-electric transistor, will have a switching speed that will be limited only by the switching dynamics of that magneto-electric material and above all are voltage controlled spintronic devices. Moreover, these magneto-electric devices promise to provide a unique field effect spin transistor (spin-FET)-based interface for input/output of other novel computational devices. These devices offer spintronics without a ferromagnet, with faster write speeds (<20 ps/full adder), at a lower cost in energy (<20 aJ/full adder), greater temperature stability (operational to 400 K or more), and scalability, and require far fewer device elements (transistor equivalents) than CMOS.

Magneto-electric field effect transistor device concepts that emphasize the value of using a narrow channel conductor, with strong spin-orbit coupling (SOC), will have, however, enhanced ON/OFF ratios and even greater functionality. To some extent the device has been "proven" as the anomalous Hall effect [7,8] devices demonstrate feasibility.

2.2.1.1. THE ANTI-FERROMAGNET SPIN-ORBIT READ (AFSOR) DEVICE

The anti-ferromagnet spin-orbit read (AFSOR) device structure has interesting advantages: the potential for high and sharp voltage 'turn-on'; inherent non-volatility of magnetic state variables; absence of switching currents; large ON/OFF ratios; and multistate logic and memory applications. The design will provide reliable room-temperature operation with large ON/OFF ratios (>10^7) well beyond what can be achieved using magnetic tunnel junctions.[13,14] Again, the core idea is the use of the boundary polarization of the magneto-electric to spin polarize or partly spin polarize a very thin semiconductor, ideally a 2D material, with very large spin orbit coupling.

If the semiconductor channel retains large spin orbit coupling, then the spin current, mediated by the gate boundary polarization, may be enhanced and, to some extent, topologically protected. The latter implies that each spin current has a preferred direction.

2.2.1.2. THE MAGNETO-ELECTRIC SPIN-FET MULTIPLEXER

There is a variant where inversion symmetry is not as strictly broken, which leads to a non-volatile spintronics version of multiplexer logic (MUX). The magneto-electric spin-FET multiplexer also exploits the modulation of the spin-orbit splitting of the electronic bands of the semiconductor channel through a "proximity" magnetic field derived from a voltage-controlled magneto-electric material. By using semiconductor channels with large spin-orbit coupling, we expect to obtain a transverse spin Hall current, as well as a spin current overall. Depending on the magnitude of the effective magnetic field in the narrow channel, we anticipate two different operational regimes. Like the AFSOR magneto-electric spin FET, the magneto-electric spin-FET multiplexer uses spin-orbit coupling in the channel to modulate spin polarization and hence the conductance (by spin) of the device. There is a source-drain voltage and current difference between the two FM source contacts due to the spin-Hall effect when spin-orbit coupling is present. This output voltage can be modulated by the gate or gates, which influences the spin-orbit interaction in the channel especially when it is both top and bottom gated. The spin-Hall voltage in the device can be increased by using different FMs in the source and drain. To increase the spin fidelity of current injection at the source end, one could add a suitable tunnel junction layer (basically a 1nm oxide layer) between the magnetic source and the 2D semiconductor channel, though this latter modification would result in diminished source-drain currents.

The challenges in pushing forward these technologies extends not only to the fabrication and characterization of a new generation of non-volatile magneto-electric devices, but also to ascertaining the optimal implementation of CMOS plug in replacement circuits. That said, the magneto-electric transistor has far fewer challenges to implementation than the magneto-electric magnetic tunnel junction, so, not surprisingly, there is a shifting of development effort toward these and related devices for both memory and logic.

2.2.2. OXIDE-BASED RESISTIVE MEMORY (OXRAM)

The redox-based nanoionic memory operation is based on a *change in resistance* of a MIM structure caused by ion (cation or anion) migration combined with redox processes involving the electrode material or the insulator material, or both.[15,16,17] Three classes of electrically induced phenomena have been identified that involve chemical effects, i.e., effects which relate to redox processes in the MIM cell. In these three ReRAM classes, there is a competition between thermal and electrochemical driving forces involved in the switching mechanism. Two major types of ReRAM exist: i) those based on metal oxide (OxRAM), which involve oxygen vacancy motion, and ii) conducting bridge-based RAM (CBRAM), which involves metal cation motion. This section covers the three categories of OxRAM, and conducting bridge-based RAM (CBRAM) is covered in the following section. Beyond CMOS has sub-categorized oxide-based ReRAM (OxRAM) based on the electrical switching type (bipolar versus unipolar) and whether the device forms a filament. Most of the literature fits into the three categories: bipolar filamentary, unipolar filamentary, and nonfilamentary.[18]

In most cases, the conduction is of a filamentary nature, and hence a one-time formation process is required before the bi-stable switching can be started. If this effect can be controlled, memories based on this bi-stable switching process can be scaled to very small feature sizes. The switching speed is limited by the ion transport. If the active distance over which the anions or cations move is small (in the <10 nm regime) the switching time can be as low as a few nanoseconds. Many of the finer details of the ReRAM switching mechanisms are still unknown. Developing an understanding of the physical mechanisms governing switching of the redox memory is a key challenge for this technology. Nevertheless, recent experimental demonstrations of scalability,[19] retention,[20] and endurance[21] are encouraging.

2.2.2.1. BIPOLAR-FILAMENTARY OXRAM

Bipolar filamentary OxRAM is the most common form of oxide-based ReRAM. As the name suggests these devices are able to maintain their resistance after the application of an electrical stimulus. The mechanism of operation of these devices often involves valance change of the dielectrics (e.g. oxides) or redox reactions of the dielectrics between the electrodes.[22,23] The dielectrics are mostly comprised of one or a few layers of insulating materials[24] (e.g., oxide AlO_x, HfO_x, TaO_x, TiO_x, WO_x, ZrO_x, oxynitrides AlO_xN_y, or nitrides including AlN_x and CuN_x) sandwiched between two electrodes. During the time of fabrication or the electroforming process, the electrode with a relatively active metal interacts with the dielectric material to generate anion

vacancies (Oxygen or Nitrogen).[25] The counter electrode is typically inert to provide an electrical contact and form a relatively high electronic barrier at the interface (e.g. Schottky-like barrier)[26]. TaOx and HfOx are the leading candidates among the aforementioned dielectrics, due to their superior performance (e.g. endurance) and CMOS compatibility.

A one-time electroforming process is required for most OxRAM switches to create a conduction filament(s)/channel(s) across the dielectric layer linking the electrodes. All subsequent switching events which are operated at significantly smaller voltages are believed to rupture and recover a part of the filament in the vicinity of the inert metal electrodes. Electroforming is an electrochemical process where the reduction of the oxide and nitride dielectrics takes place [27]. The electroforming process can be avoided by employing a thinner dielectric layer with an anion scavenging layer, thereby leading to electroforming free devices.

Since the demonstration of a single crosspoint HfOx device with a 10 nm dimension in 2011[28], scaling to a smaller size had been achieved by employing a sidewall electrode in a 1×3 nm^2 cross-sectional HfO_x-based OxRAM device with reasonable performance in terms of both endurance and retention.[29] Regarding repeatability, up to 10^{12} cycles has been demonstrated with $Zr:SiO_x$ sandwiched by graphene oxide layers recently.[30] This is comparable to the previous endurance record demonstrated using a Ta_2O_{5-x}/TaO_{2-x} structure developed by Samsung in 2011.[31] The fastest OxRAM was demonstrated on a TaO_x device with a programing duration about 100 ps in 2011.[32] Recently, 85ps switching was demonstrated in nitride based devices.[33] Remarkable progress has been made on improvement of the OxRAM reliability, especially for TaO_x. Extrapolated retention at 85°C by stressing TaO_x in the temperature range from 300°C to 360°C is estimated to be years with an activation energy of 1.6 eV.[34] Reliable switching operations have been demonstrated at 340°C with devices based on 2D layered heterostructures (e.g., graphene/$MoS_{2-x}O_x$/graphene).[35]

Unconventional electrodes like graphene have been paired with HfO_x dielectrics and yield a low power consumption, a write/erase energy about 230 fJ per bit for a single programming transition.[36] Recently a Pt/BMO((Bi, Mn)O_x)/Pt structured OxRAM device was used to demonstrate an even lower write/erase energy per transition of the order of 3.8 pJ/bit for read and 20 pJ/bit for write operation.[37]

Large scale integration of OxRAM switching based on 1T1R schemes has been carried out by Toshiba, Panasonic and IMEC. In 2013, Toshiba announced the 32 Gb RRAM chip integrated with 24 nm CMOS.[38] In 2014, Panasonic and IMEC demonstrated the encapsulated cell structure with an $Ir/Ta_2O_5/TaO_x/TaN$ stack on a 2-Mbit chip with 40 nm node. In addition, passive integration of 1S1R scheme has been reported by Crossbar on a 4-Mbit chip, but the material stack of the OxRAM switch has not been revealed.[39]

A number of technical challenges remain despite the significant advancements made in the field of OxRAM. These technical challenges are hampering the commercialization of OxRAM. One of the main challenges is the fact that the switching currents for devices based on the currently most mature materials (e.g., HfO_x and TaO_x) are still too high (above tens of μA) for large arrays. Apart from that, the filament formation and rupture processes are stochastic in nature, which leads to variation in switching parameters like the voltage and resistance distribution of the switching. This is especially detrimental to certain applications such as multilevel cell memory. Passive arrays of OxRAM switches will require either select devices (selectors) or intrinsic IV nonlinearity. However, an external select device that meets all the requirements, including great endurance, large selectivity (ON/OFF ratio), good scalability, fast speed, low variability, suitable operation current and voltage, remains to be demonstrated.

2.2.2.2. Bipolar Non-Filamentary OxRAM

The *Bipolar Non-Filamentary* OxRAM is a non-volatile bipolar resistive switching device composed of one or more oxide layers. One layer is a conductive metal oxide (CMO), which is usually a perovskite such as PrCaMnO3 or $Nb:SrTiO_3$.[40] In contrast to *Unipolar* and *Bipolar Filamentary* OxRAM devices – typically based on binary oxides such as TiO_x, NiO_x, HfO_x, TaO_x or combinations thereof—the resistance change effect of the *Bipolar Non-Filamentary* OxRAM is *uniform*. Depending on the materials choice and structure the current is conducted across the entire electrode area, or at least across the majority of this area. A forming step to create a conductive filament is *not* needed. Non-volatile memory functionality is achieved by the field-driven redistribution of oxygen vacancies close to the contact resulting in a change of the electronic transport properties of the interface (e.g. by modifying the Schottky barrier height). Oxygen can be exchanged between layers due to the exponential increase in ion mobility at high fields. Low current densities, uniform conduction, and bipolar switching imply that substantial self-heating is not involved. Typical R_{OFF} to R_{ON} ratios are on the order of 10.

One class of the Bipolar Non-Filamentary OxRAM includes a deposited ion conductive tunnel layer (Tunnel ReRAM), e.g. ZrO_2. Here, a redistribution of oxygen vacancies causes a change of the electronic transport properties of the tunnel barrier. Low current densities and area scaling of device currents enable ultra-high-density memory applications. Set, reset, and read currents scale with device area. In addition, set, reset, and write currents are controlled by the tunnel oxide and hence, can be adjusted by changing the tunnel barrier thickness. Both set and reset IV characteristics are highly nonlinear enabling true 1R cross-point architectures *without* the need for an additional selector device for asymmetric arrays up to 512×4096 bit. No external circuitry

is needed for current control during set operation. A continuous transition between on and off states allow straightforward multi-level programming without the need for precise current control.

The typical thickness of the CMO is greater than 5 nm and the tunnel barrier is typically 2–3 nm. If a tunnel barrier is present, the adjacent electrode needs to be an inert metal such as Pt to prevent oxidation during operation. For the case of PCMO cell, low deposition temperatures less than 425°C of all layers enables back end integration schemes.

Currently the technology is in the research and development stage. Depending on material system and structure cycling endurance over 10,000 cycles and up to a billion cycles as well as data retention from days to months at 70°C has been achieved on single devices.[41, 42, 43] Within the Bipolar Non-Filamentary OxRAM device family the Tunnel OxRAM is probably the furthest developed technology. Single device functionality is demonstrated down to 30 nm. Set, reset, and read currents scale with area and tunnel oxide thickness facilitating sub µA switching currents with read currents in the order of a few nA to a few 100 nA. BEOL integration schemes and CMOS/OxRAM functionality are verified for 200 nm devices on 200 mm CMOS wafers. True cross-point array (1R) functionality utilizing the self-selecting non-linear device IV characteristics and transistor-less array operation is demonstrated on fully decoded 4kb true cross-point arrays (1R) build on top of CMOS base wafers. SLC and MLC operations are demonstrated within 4kb arrays.

Major challenges to be resolved towards the commercialization of Bipolar Non-filamentary OxRAM are, in order of priority, a) improvement of data retention, b) the integration of conductive metal oxide layer (perosvkites) via ALD or the replacement of CMO by more process friendly materials, and c) the replacement of Pt electrodes by a non-reactive, more process-friendly electrode material.

The most important issue is the improvement of retention and the "voltage-time dilemma." This dilemma hypothesizes physical reasons as to why it is difficult in a particular device and material system to simultaneously obtain a long retention, with short low read voltages, and fast switching at moderate write voltages.[44] Even though the exact mechanism is still under investigation there is a common agreement that oxygen vacancies are moved by the external electric field resulting in different resistance states of the memory cell. Vacancy drift at room temperature is possible due to a field dependent mobility, which increases exponentially with field at fields of 1 MV/cm and larger. However, current models based on a field dependent mobility underestimate the experimentally observed ratio between set/reset times and data retention indicating that the mechanism is only partly understood. More theoretical work is needed to understand the kinetics of programming and retention mechanisms. Once understood, materials need to be chosen to maximize the ratio between set/reset and retention times. The goal is to set/reset devices at low temperatures and meet retention requirement of 10 years at 70°C, 85°C, and 125°C, depending on the application. A multi-layer ReRAM structure (HfO_2/A_2O_3) was shown to improve retention by suppressing tail bit failure due to decreased oxygen ion diffusivity.[45]

Memory cells using conductive perovskite material as an electrode have proven to show excellent device-to-device and wafer-to-wafer reproducibility with yields close to 100%. One of the reasons might be that perovskites display high oxygen vacancy mobilities and tolerate large variations in the oxygen content while maintaining its crystal structure. From an integration perspective, ALD is the method of choice for advanced technology nodes and future 3D integration schemes. Key issues are the control of the metals ratio (perovskites are ternary or quaternary oxides), the control of the oxygen stoichiometry in the cell, oxygen loss in the presence of reducing atmospheres like H_2, as well as high temperatures required for crystallization. Eventually a migration to binary oxides with comparable properties might be required to resolve the integration challenges.

Platinum or other noble electrodes display superior device performance over fab friendly electrodes like TiN. On the one hand it was observed that the oxidation resistance of TiN is not sufficient to prevent oxidation and the formation of TiO_2 during operation. On the other hand, inert electrodes such as Pt or Pt-like metals are difficult to integrate. New oxidation resistant electrodes and Pt alternatives are required to reduce integration challenges and enable 3D integration schemes.

2.2.2.3. UNIPOLAR FILAMENTARY OXRAM

Note that unipolar filamentary OxRAM has been removed from the memory tracking tables, due to lack of research over the period covered by this Beyond CMOS chapter. However, this text section has been maintained to provide background on earlier unipolar OxRAM work, due to the close relationship and key differences with bipolar OxRAM.

Unipolar OxRAM is another resistive switching device, also referred to in the literature as thermochemical memory (TCM)[15] due to its primary switching mechanism. The device structure consists of a top electrode metal/insulator/bottom electrode metal (MIM) structure. Typical insulator materials are metal-oxides such as NiO_x, HfO_x, etc., and common metal electrodes include TiN, Pt, Ni, and W. In general, the device can be asymmetric (i.e. top electrode material differs from bottom electrode material), but unlike other types of ReRAM, asymmetry is not required.

The first reported resistive switching in these MIM structures after 2000 was unipolar in nature (see reference[46] for the first integrated device work that put metal oxide ReRAM in the spotlight). Unipolar is defined as switching where the same polarity

of voltage needs to be applied for changing the resistance from high to low (SET) or from low to high (RESET). Note that in the general case, polarity is still important (e.g. repeatable SET/RESET switching only occurs for one polarity of voltage with respect to one of the electrodes[47]). Only in symmetric structures (e.g. Pt/HfO_2/Pt), nonpolar behavior can be obtained, where SET and RESET are occurring irrespective of voltage polarity.[48]

The switching process is generally understood as being filamentary, where conduction is caused by a filamentary arrangement of defects (e.g. oxygen vacancies) throughout the thickness of the insulator film. As with other filamentary OxRAM devices, an initial high voltage "electroforming" step is required to form the conduction filament, while subsequent RESET/SET switching is thought to occur through local breaking/restoration of this conduction path.

The unipolar character of the switching indicates that drift (of charged defects) in an electric field plays a less important role (than it does in bipolar switching resistive memory), but that thermal effects probably dominate.[49,50] On the other hand, polarity effects indicate anodic oxidation (e.g. at Ni or Pt electrodes) is responsible for RESET.[47] These findings suggest a thermo-chemical "fuse" model for describing this unipolar switching. It has been shown for different MIM structures that both unipolar and bipolar switching mechanisms can be induced, depending on the operation conditions.[51,52,53,54] An interesting work reporting on the Scaling Effect on Unipolar and Bipolar Resistive Switching of Metal Oxides was published.[55]

A unipolar switching device is seen as advantageous for making scaled memory arrays, as it only requires a selector device as simple as a diode that can be stacked vertically with the memory device in a dense crossbar array.[46] In addition, the use of a single program voltage polarity greatly simplifies the circuitry.

On the other hand, as has been exemplified in mixed mode (unipolar/bipolar) operation of memory cells, there are important trade-offs between the unipolar and bipolar switching modes. On the positive side, unipolar switching mode typically shows a higher ON/OFF resistance ratio. On the negative side, unipolar switching is typically obtained at higher switching power (higher currents) than the bipolar mode, and also endurance is much more limited. As a result, major research and development work on resistive memories has shifted towards bipolar switching mechanisms. Yet, some interesting recent development work has been reported.[56,57,58,59,60,61] One paper[56] shows an endurance of over 10^6 cycles with a resistive window of over 5 orders of magnitude (and a reset current ~1mA). Others[57,58,59] demonstrate how unipolar RRAM elements can be integrated in a very simple way in an existing CMOS process (known as Contact ReRAM technology). This may provide a very inexpensive embedded ReRAM technology. Recently, integration unipolar ReRAM with a 29 nm CMOS process was reported.[59] The key attributes were a small cell size (0.03 μm^2), switching voltage of less than 3V, RESET current of less than 60 µA, endurance > 10^6 cycles, and short SET and RESET times of 500 ns and 100 µs, respectively. One paper[60] shows 4Mb array data using this same Contact-RRAM technology, fabricated using a 65 nm CMOS process. To accommodate for the low logic VDD process, on-chip charge pump was applied. Set and reset voltages are less than 2V. Another paper[61] reports on a novel approach using thermal assisted switching to lower the switching current.

As stated above, large OFF to ON resistance ratio is an attribute of unipolar switching. The low resistance window and large intrinsic variability of bipolar switching OxRAM may require complex and time-consuming switching operation schemes (e.g. the so-called verify scheme). Further study of the stability and control of the large resistance window (at low current levels), are required to determine if unipolar OxRAM variability can be improved, potentially even allowing for multi-level cell operation.

Major challenges to be resolved are the high switching current that seems inherent to the unipolar operation mode. Reset currents less than 100 µA are achieved but need further reduction to less than 10 µA.[57,58,59] Recently, a possible solution incorporating thermally assisted switching has been presented.[61]

2.2.3. CONDUCTING BRIDGE MEMORY

Conductive Bridge RAM (CBRAM), also referred to as, Programmable Metallization Cell (PMC), and electrochemical metallization cells, is a device which utilizes electrochemical control of nano-scale quantities of metal in thin dielectric films or solid electrolytes to perform the resistive switching operation.[62] The basic CBRAM cell is a metal–ion conductor–metal (MIM) system consisting of an electrode made of an electrochemically active material such as Ag, Cu or Ni, an electrochemically inert electrode such as W, Ta, or Pt, and a thin film of solid electrolyte sandwiched between both electrodes.[63] Large, non-volatile resistance changes are caused by the oxidation and reduction of the metal ions by the application of low bias voltages. Key attributes are low voltage, low current, rapid write and erase, good retention and endurance, and the ability for the storage cells to be physically scaled to a few tens of nm. The material class for the dielectric film or the solid electrolyte is comprised of oxides, higher chalcogenides (including glasses), semiconductors, as well as organic compounds including polymers.

CBRAM is a strong emerging memory candidate primarily due to scalability (~10 nm),[64] ultra-low energy operations due to fast read, write and erase times, and low voltage requirements.[65] Maturity of the CBRAM technology development can be assessed by the fact that many companies are either shipping products based on CBRAM or are in advanced stages of commercialization. Recent publications show CBRAM technology application in various markets including SSDs,[66] embedded NVM,[67] and serial interface non-volatile memory replacement.[68] In 2012, a CBRAM-based serial NVM replacement product became commercially

available.[69] In 2014, a 16 GB CBRAM array based on a CuTe CBRAM cell was demonstrated.[70,71] Such efforts are critical to identify core technology challenges[72] and fundamental materials and mechanisms.[73] Novel applications such as reconfigurable switch[74] and synaptic elements in Neuromorphic systems[75] based on CBRAM are also gaining prominence and are expected to expand the application base for this technology.

As with other filamentary ReRAM technologies, CBRAM is challenged by bit level variability,[72] the random nature of reliability failure such as retention or endurance, and random telegraph noise potentially contributing to read disturbs.[76] Such issues require large populations of bits to be studied, which suggests collaboration between universities and industry may be beneficial. Focus on fundamental understanding and simultaneously addressing some mitigation path such as error correction schemes, redundancy and algorithm development would enable closing the technology gap.

Engineering hurdles include the availability and integration of new materials used in CBRAM at advanced process nodes especially when there could be issues with compatibility of thermal budgets and process tooling. The availability of integrated array level information suggests that some of these challenges are being resolved in the recent years.[68,74] Active participation from semiconductor equipment vendors and material suppliers would assist in overcoming manufacturing hurdles rapidly.

2.2.4. MACROMOLECULAR (POLYMER) MEMORY

Macromolecular memory is a category of memory which focuses structures incorporating a layer of polymer, and the polymer may contain nano-particles, small molecules and nanoparticles that are sandwiched between two metal electrodes. This structure allows two different stable electrical states controllable through an external electrical voltage. These two stable electrical states, which are often called ON and OFF states (or 0 and 1), exhibit resistive, ferroelectric or capacitive natures according to the physical properties of the sandwich. The first fully-organic memory devices, based on nano-composite (a blend of poly-vinyl-phenol (PVP) and Bucky-ball (C60)) was presented in Materials Research Society.[77] Around the same time, memory devices using gold nano-particles and 8-hydroxyquinoline, dispersed in a polystyrene matrix, were also demonstrated.[78] Since then, the interest to use an admixture of nano-particles, small molecules and polymers in the manufacture of electronic memory devices, is on the rise. Non-volatile memory effects with a non-destructive read have been reported for a surprisingly large variety of polymeric/organic materials and blends of polymers with nanoparticles and molecules. Unlike the other four categories, this category is based on the material used in the switching layer(s) of the cell, but the mechanism in not specified. Both bipolar and unipolar (all pulses of the same polarity) switching have been demonstrated. Macromolecular ReRAM may have a mechanism placing it in one of the four main ReRAM categories listed above. However, the other mechanisms behind the electrical bistability, such as capacitive and ferroelectric, have also been reported.

Depending on the structure of the polymer, a variety of mechanisms can be operative. For polymers supporting transport of inorganic ions, formation of metallic filaments is reported. In semiconducting polymers supporting ion transport, dynamic doping due to migration of inorganic ions occurs. Ferroelectric polymers in blends with semiconducting material give rise to a memory effect-based modification of charge injection barriers by the ferroelectric polarization. However, for many polymeric materials, the origin of the resistive switching is not well understood. To date no specific design criteria for the polymer are known, although clear correlations between memory effect and electronic properties of the polymer have been demonstrated.

Stability of the memory states at high temperatures (85°C, 2×10^4 s) has been demonstrated.[79,80] Programming at very low power (70 nW) has been realized.[80] Assuming a 15 ns switching time determined for the same system, one might achieve a write energy of 6×10^{-15} J/bit. Furthermore, low programming voltages have been realized: +1.4 and -1.3 V for the two states with good retention time (>10^4 s).[81] Downscaling of polymer resistive memory cell to the 100 nm length scale has been reported.[82] At this length scale, integration of memory cells into an 8×8 array could be shown. Polymer memory cells on a flexible substrate have been shown.[83] For amorphous carbon, downscaling to nanometer sized cells has been published (1×10^3 nm^2).[84] Using carbon nanotubes as macromolecular electrodes and aluminum oxide as interlayer, isolated, non-volatile, rewriteable memory cells with an active area of essentially 36 nm^2 have been achieved, requiring a switching power less than 100 nW, with estimated switching energies below 10 fJ per bit.[85] With regards to the mechanism of operation, extensive work on the class of polyimide polymers has shown clear correlations between electronic structure of the polymer and memory effects, although a comprehensive picture for the operation has not yet emerged. A number of studies have indicated an active role of the interface between macromolecular material and (native) oxide layers in the operation of the memory involving charge trapping.[86,87] The recent and past studies show resistive,[88] capacitive (charge storage, based on electric dipole formation)[89,90] and ferroelectric behavior[91] of such devices. Thus, there is a need to open up a further discussion on the right pathway to realize such memory.

In macromolecular memory, a large variety of operation mechanisms can be operative. A key research question concerns distinguishing different mechanisms and evaluating the potential and possibilities of each mechanism. A second subsequent step would be to identify model systems for each mechanism. Having such a model system then provides a possibility to benchmark the operation of the macromolecular materials. These research steps would be crucial for establishing and securing the collaboration of the chemical industry; for design, synthesis and development of the next generation macromolecular materials

for memory applications, clear guidelines on the required structural and electronic properties of the macromolecular material are needed. For instance, memory effect originating for metallization and formation of metallic filaments requires macromolecular materials that support transport of ions and have appropriate internal free volume for ion conduction. Here the field could benefit from interaction with the field of polymer batteries. Ferroelectric polymers have been shown to give rise to resistive memory[92] and could benefit enormously from development of new macromolecular polymeric materials with combined ferroelectric switching and semiconducting structural units. Finally, a number of macromolecular memories involve oxide layers. Here mutually beneficial interaction with the (research) community on metal oxide ReRAM switching could spring, because at the macromolecular / oxide interface trap states can be engineered by tuning the electron levels of the macromolecular material.

In a nutshell, this area certainly needs an attention from theoretical physicists, materials scientists, chemists and device engineers. There are a number of issues that need to be addressed before we can embark on extending these devices to the real world. Such issues involve understanding of the electrical bistability mechanism in nano-composite (there are a number of contradicting theories), maintaining the difference between low and high conduction states for a longer period time by ensuring the stability of the high and low states, selecting environmentally friendly materials required for fabrication of nano-composite/polymer materials, and developing a cost-effective methodology for the fabrication of devices.

It is not possible to replace silicon-based memory devices in the foreseeable future. However, there are a number of other applications where "cheap" electronic memory devices can play a vital role. For example, nano-composite based memory devices can be directly printed on medicine bottles/packages and the information about the patient and schedule of taking medicine can be stored on the printed device.

2.2.5. FERROELECTRIC MEMORY

Coding digital memory states by the electrically alterable polarization direction of ferroelectrics has been successfully implemented and commercialized in capacitor-based Ferroelectric Random Access Memory (covered in Table BC2.1). However, in this technology the identification of the memory state requires a destructive read operation and largely depends on the total polarization charge on a ferroelectric capacitor, which in terms of lateral dimensions is expected to shrink with every new technology node. In contrast to that, alternative device concepts, such as the ferroelectric field effect transistor (FeFET) and the ferroelectric tunnel junction (FTJ), allow for a non-destructive detection of the memory state and promise improved scalability of the memory cell. The current status of and key challenges for these emerging ferroelectric memories will be assessed within this section.

2.2.5.1. FERROELECTRIC FET

The FeFET is best described as a conventional MISFET that contains a ferroelectric oxide in addition to or instead of the commonly utilized SiO_x, SiON or HfO_2 insulators. The former case requires the direct and preferably epitaxial contact of the ferroelectric to the semiconductor channel (metal-ferroelectric-semiconductor-FET, MFSFET), whereas the latter and commonly applied case maintains a buffer layer between the channel material and the ferroelectric (metal-ferroelectric-insulator-semiconductor-FET, MFISFET). When additionally introducing a floating gate in-between the buffer layer and the ferroelectric, a metal-ferroelectric-metal-insulator-semiconductor structure (MFMISFET) may be obtained that shares its equivalent circuit representation with the MFISFET approach. By applying a sufficiently high voltage pulse to the gate of the FeFET (i.e. voltage drop across the ferroelectric layer larger than its coercive voltage V_c), the polarization direction of the ferroelectric can be set to either assist in the inversion of the channel or to enhance its accumulation state. This results in a polarization dependent shift of the threshold voltage V_T, which allows for a non-destructive read operation and a 1T memory operation comparable to that of FLASH devices.

In order to assess the material and device requirements for a reliable and scalable FeFET technology the following two intrinsic relations in a ferroelectric gate stack need to be considered. First it is important to note that the extent of the aforementioned V_T-shift (memory window) in FeFET devices is primarily determined by the V_C of the implemented ferroelectric rather than by its remnant polarization P_r.[93] This results in a scaling versus memory window trade-off as V_c is proportional to the coercive field E_c and thickness d_{FE} of the ferroelectric. The inability of the commonly utilized perovskite-based FeFETs to laterally scale beyond the 180 nm node is therewith not solely based on the insufficient thickness scaling of perovskite ferroelectrics,[94,95] but rather due to their low E_c (SBT: 10-100 kV/cm, PZT: ~50 kV/cm, summarized in[96]) that in order to maintain a reasonable memory window requires compensation by a large d_{FE}. A solution to this scaling retardation is provided by the high coercive field (1-2 MV/cm) and thickness scalable FE-HfO_2.[97] This CMOS-compatible material innovation enabled the demonstration of a FeFET technology scaled to the 28 nm node utilizing a conventional HKMG technology and is already used in high volume production.[98] The close resemblance of the HKMG transistor and the FE-HfO_2-based memory transistor proves especially useful for the realization of an embedded memory solution with greatly reduced mask counts as compared to embedded FLASH.

The second noteworthy and important characteristic of the FeFET gate stack is related to its intrinsic capacitive voltage divider, which causes a significant gate voltage drop and buildup of electric field not only across the ferroelectric, but also across the non-

ferroelectric insulator in the gate stack. When additionally considering the incapability of the linear insulator to fully compensate the polarization charge of the ferroelectric layer, it becomes apparent that even in the case of no external biasing the capacitive voltage divider leads to a buildup of a permanent electric field. The so-called depolarization field building up in the ferroelectric is opposed to the polarization direction of the ferroelectric and to the electric field induced in the insulator[99]. The capacitive voltage divider is therefore directly responsible for the retention loss during stand-by as well as for the gate voltage distribution and the corresponding charge injection during write operations. This retention and endurance critical distribution of the electric field within the gate stack may be optimized by choosing the insulator capacitance as high as possible and the ferroelectric capacitance as low as possible. In the perovskite-based FeFET this is achieved by utilizing high-k buffer layers and is additionally fostered by the unavoidably large physical thickness of the perovskite ferroelectrics.[4, 100]. In the case of the aggressively scaled FE-HfO_2-based FeFET, the small thickness of the ferroelectric is compensated by the comparably low permittivity of HfO_2, the possibility to use ultra-thin interfacial layers, and by the depolarization resilience of the high E_c.[96,101] This leads to the situation that despite the markedly different stack dimensions and materials used, the electrically obtained characteristics are quite similar. Fast switching speed (≤100 ns), switching voltages in the range of 4-6 V, and 10-year data retention and endurance in the range of 10^{12} switching cycles have been demonstrated for FE-HfO_2-[97,98,102,103] as well as for perovskite-based FeFETs.[93,104,105] In the case of cycling endurance, however, the high E_c of FE-HfO_2 and the correspondingly large electric field in the insulator facilitates charge trapping during write operation, which was identified as the root cause for the limited endurance of 10^5 cycles observed in FE-HfO_2-based FeFETs with ultra-thin interfacial layer enabling excellent data retention.[106] Nevertheless, in an alternative approach utilizing a thicker insulator and sub-loop operation it was demonstrated that at the cost of retention a cycling endurance $>10^{12}$ may still be obtained.[102] In the current stage of development this endurance versus retention trade-off may be tailored, spanning the application range from embedded NOR-FLASH replacement with high retention requirements to low refresh rate 1T DRAM requiring high cycling endurance.

Entirely overcoming this endurance versus retention trade-off will require an improved stack design that may include a tailored polarization hysteresis (low P_r and high P_r/P_s ratio)[93], a reduced trap density at the interfaces,[106] an optimized capacitive voltage divider by area scaling in the MFMISFET approach[107] or the realization of a MFSFET device by implementing recent breakthroughs in the epitaxial growth of FE-HfO_2.[108] Despite promising results obtained for perovskite-based FeFET devices implemented into 64Kb NAND-Arrays at a feature size of 5 µm[105], little is known about the variability and array characteristics of FeFET devices scaled to technology nodes approaching the grain or domain size of the implemented ferroelectrics. Initial investigations on phase and grain distribution in doped HfO_2 based ferroelectric thin films and the effects of such granularity on device level characteristics of scaled FeFETs (such as on the statistical nature of switching) have recently been reported in Refs. [109,110,111]. Recently, 64 kb and 32 Mb FeFET arrays were demonstrated in the 28 nm[112] and the 22 nm FD-SOI CMOS platform,[113] respectively—in each case, a clear low and high V_T separation at the array level was demonstrated. Nevertheless, in order to fully judge the variability of ferroelectric phase stability at the nanoscale and to guide material optimization and fundamental understanding of the phenomenon, larger array statistics in the kB to Mb range and high-resolution PFM data will be required. Besides, recent demonstration of non-volatile memory operation based on antiferroelectricity—a phenomenon closely related to ferroelectricity—in work-function engineered ZrO_2 thin film capacitors may allude to new way of addressing and potentially solving some of these challenges in FeFETs.[114]

2.2.5.2. FERROELECTRIC TUNNEL JUNCTION

The ferroelectric tunnel junction, a ferroelectric ultra-thin film commonly sandwiched by asymmetric electrodes and/or interfaces, exhibits ferroelectric polarization induced resistive switching by a non-volatile modulation of barrier height. With the tunneling current depending exponentially on the barrier height, the ferroelectric dipole orientation either codes for a high or a low resistance state in the FTJ, which can be read out non-destructively. The resulting tunneling electroresistance (TER) effect of FTJs, the ratio between HRS and LRS, is usually in the range of 10 to 100 ([115] and references therein). However, giant TER of > 10^4 has most recently been reported in a super-tetragonal $BiFeO_3$ based FTJ by Yamada et al.[116] A similarly high TER was demonstrated by Wen and co-workers[117] for a $BaTiO_3$ tunnel barrier by replacing one metal electrode of the FTJ with a semiconducting electrode. With this new junction design, the modulation of tunneling current does not only rely on barrier height, but due to a variable space charge region in the semiconductor, also on a barrier width modification. With these most recent findings, two strategies to achieve giant TER have been identified: either use a ferroelectric barrier with a large polarization such as $BiFeO_3$ or use a semiconductor as electrode material to modulate the barrier width by field-induced carrier depletion.

The MFM-based structure of FTJs may be able to enable a retention time (> 10 years) and very high cycling endurance (> 10^{14}) properties of conventional FRAM. Nonetheless, in order to have a significant tunneling current, ferroelectric films in FTJs usually have a thickness ranging from several unit cells to ~5 nm, which is much thinner than in commercialized 1T-1C FRAM (> 50 nm). Due to larger interface contributions and increased leakage currents at reduced thickness, experimental data of these material systems might strongly deviate from their thick film behavior and need to be assessed separately.[118] However, even though only limited data are available up to this point, promising single cell characteristics have already been demonstrated, such as the most recent demonstration of $4x10^6$ endurance cycles and extrapolated data retention of 10 years at room temperature for a $BiFeO_3$-

based FTJ.[119] In the context of retention, it should be noted that despite improved TER, the newly proposed MFS-FTJ structure will give rise to a depolarization field, which will most likely degrade memory retention in a similar manner as described for the FeFET in Section 2.2.5.1. The highly energy efficient electric field switching, common to all ferroelectric memories, enables fast (10 ns[120]) and low voltage (1.4 V[119]) switching in FTJ devices and results in a minimal power consumption during write operation (1.4 fJ/bit, calculation based on the device characteristics given[121]). Due to the availability of non-destructive read-out and the further reduced ferroelectric thickness in FTJ devices as compared to conventional FRAM, improved voltage scaling and total energy consumption may be expected from this technology.

Similar to most other two-terminal resistor-based memories with insufficient self-rectification, the elimination of sneak currents in large crossbar arrays is most efficiently suppressed utilizing 1T-1R or 1D-1R cell architecture. In terms of scaling, this two-element memory cell, as well as the scalability of the selector device itself, has to be considered.[122] Simply based on the lateral dimensions of the FTJ element (assuming unlimited scalability of the selector), scaling below 50 nm^2,[121]based on PFM data,[123] most likely appears possible. However, with further scaling a simultaneous enhancement of the LRS current density is required to maintain readability in massively parallel memory architectures. A recent breakthrough of $1.4x10^5$ A/cm^2 current density at 300 nm feature size has been achieved by Bruno et al.[124] utilizing low resistivity nickelate electrodes. Based on these results maintaining 10 µA read current for feature sizes <100 nm appears possible. New FTJ concepts are also emerging; for example, engineered domain walls within the ferroelectric layer in an FTJ structure can lead to exotic quantum phenomenon such as resonant electron tunneling and quantum oscillations in the electrical conductance albeit at low temperatures.[125]

FTJ based memories are currently at a very early development stage, and most of the research activity is focused on perovskite-based ferroelectrics. Further investigations reaching beyond single device characterization will be needed to fully judge the scalability of FTJ as well as its MLC capability suggested in Ref. [126]. So far, no conclusions can be drawn on retention and statistical distribution of the polarization induced resistance states in large arrays. However, when considering the collective phenomenon of ferroelectricity with multiple dipoles contributing to a resistance change as opposed to filament-type resistive switching, advanced scalability may be expected. First results have shown that the FTJ is very similar to ReRAM in terms of electrical behavior and memory design, albeit distinct physical mechanisms. It should be noted that current prototypes could actually have both FTJ and ReRAM traits, as resistive switching is common among oxides including ferroelectric perovskites ([127] and references therein). For future development, the ferroelectric film in an ideal FTJ should be as thin as possible to allow scalability (while maintaining sufficient read current) and much less defective than that in ReRAM (e.g., with less oxygen vacancies), so that the mechanism of ferroelectric switching can dominate electrical behavior with little influences from mechanisms related to conducting filaments. The manufacturability of the rather complex electrode-perovskite ferroelectric-system of the FTJ concept will largely rely on the availability of high throughput and CMOS-compatible epitaxial growth techniques for large substrates or alternatively on the unrestricted feasibility demonstration of a polycrystalline FTJ. In this context it is worth noting that the CMOS-compatibility and advanced thickness scalability of ferroelectrics based on HfO_2 and its doped variant[103] as well as recent breakthroughs in its epitaxial growth[108] might yield great potential for the manufacturability of competitive FTJs. Experimental demonstrations of FTJs based on doped variant of HfO_2 were recently reported in Refs. [128,129,130].

2.2.6. MASSIVE STORAGE DEVICES

Device scaling has become a matter of strategic importance for modern and future information storage technologies, which motivates an exploration of unconventional materials with competitive performance attributes. By 2040 the conservative estimate of the worldwide amount of stored data is 10^24 bits, and the high estimate is ~10^29 bits[131] (these estimates are based on research by Hilbert and Lopez[132]). In nature, much of the data about the structure and operation of a living cell is stored in the molecule of deoxyribonucleic acid (DNA) and using nucleic acids molecules, such as DNA, for memory storage has been proposed. DNA has an information storage density that is several orders of magnitude higher than any other known storage technology: 1 kg of DNA stores 10^24 bits, for which $>10^9$ kg of silicon Flash memory would be needed.[131] Thus, a few tens of kilograms of DNA could meet all of the world's storage needs for centuries to come.

A number of recent studies have shown that DNA can support scalable, random-access and error-free information storage.[133,134,135] A state-of-the-art operating system developed by at the University of Washington with an industry partner is a DNA-based archival storage framework that supports random access from a DNA key-value store.[136] The DNA-stored files are compatible with mainstream digital format, and large-scale DNA storage up to 200 MB has been demonstrated.[137] There are still many unknowns regarding both DNA operations in cell and with regard to the potential of DNA technology for massive storage applications. DNA volumetric memory density far exceeds (10^3–10^7×) projected ultimate electronic memory densities. Also, in the living cell, the memory read/write operations occur at high speed (<100 µs/bit) and require very low energy of ~10^{-17} J/bit or 10^{-11} W/GB.[138] DNA can store information stably at room temperature for hundreds of years with zero power requirements, making it an excellent candidate for large-scale archival storage.[138] Also, DNA is an extremely abundant and totally recyclable material. Recently, a method for efficient encoding of information—including a full computer operating system—into DNA was presented, which approaches the theoretical maximum for information stored per nucleotide.[139] One of the goals for research

efforts is to demonstrate miniaturized, on-chip integrated DNA storage. New methods for DNA synthesis and sequencing are key components for these developments.

Two major categories of technical challenges remain:

- Physical Media: Improving scale, speed, cost of synthesis and sequencing technologies.
- Operating System: Creating scalable indexing, random access and search capabilities.

The key technological and scientific challenges are in improving performances beyond the life sciences industry. In the life science industry applications require perfect synthesis and perfect sequencing, while scale, throughput and cost are secondary considerations. For data storage, high read and write error rates can be tolerated, and information encoding schemes can be used. In this application, scale and throughput and cost are primary considerations. Current DNA storage workflows can take several days to write and then read data, due to reliance on life sciences technologies that were not designed for use in the same system. The demonstrated DNA write-read cycle is too slow and costly to support exascale archival data storage. Solving this problem will require: 1) Substantial reductions in the cost of DNA synthesis and sequencing, and 2) Deployment of these technologies in a fully automated end-to-end workflow.

2.2.7. MOTT MEMORY

Mott memory is a metal/insulator/metal capacitor structure consisting of a correlated electron insulator (or Mott insulator). Correlated electron insulators often show the electronic phase transition accompanied by a drastic change in their resistivity under external stimuli such as temperature, magnetic field, electric field, and light. Mott memory exploits this electronic phase transition (called Mott metal-to-insulator transition or Mott transition[140]) induced by an electric field. A mechanism of the Mott memory has been theoretically proposed in terms of the interfacial Mott transition induced by the carrier accumulation at a Schottky-like interface between a metal electrode and a correlated electron insulator.[141] The theory also predicted that the resistive switching due to the interfacial Mott transition has a non-volatile-memory functionality, because the Mott transition is a first-order phase transition due to its nature.[140] In addition, Mott memory based on the Mott transition involving a large number of carriers (more than 10^{22} cm^{-3}) has in principle an advantage in device scaling, because there are a sufficient number of carries for the Mott transition even in a nanoscale device. In an ideal Mott transition, the electrons localized due to the strong electron-electron correlation come to be itinerant, via the stimuli, such as application of an electric field, and so forth. It needs no dopants, and the mechanism withstands the miniaturization of the (silicon) devices.

The Mott transition induced by an electric field or carrier injection has been experimentally demonstrated in a correlated electron material of $Pr_{1-x}Ca_xMnO_3$.[142] After this demonstration, two-terminal devices such as switches and memories have been intensively studied using such correlated electron oxides as $Pr_{1-x}Ca_xMnO_3$,[143,144] VO_2,[145,146,147] $SmNiO_3$,[148] NiO,[149,150] Ca_2RuO_4,[151] and NbO_2,[152,153] and using Mott-insulator chalcogenides of AM_4X_8 (A=Ga, Ge; M=V, Nb, Ta; X=S, Se).[154,155,156,157] In addition to these inorganic materials, recently, reversible and non-volatile resistive switching based on the electronic phase change between charge-crystalline state and quenched charge glass has been demonstrated in the organic correlated materials of θ-(BEDT-TTF)$_2X$ (where X denotes an anion).[158]

$SmNiO_3$ exhibits a colossal (8 orders in magnitude) resistance jump by hydrogenation. The $SmNiO_3$ channel with the solid state proton gate has demonstrated the electric base gated large ON/OFF switching.[148] The trigger for switching is based on the proton intercalation by electric field, and the DFT calculation explains the large gap opening by additional electron doping via protonation and is the origin for colossal resistance jump phenomena.[159] These results indicate that the device using the metal – insulator (Mott) transition driven by the strong electron-electron correlation is powerful as well as appropriate for the switching devices.

Scalability has been demonstrated down 110 × 110 nm^2 in Mott memristors consisting of NbO_2 that shows the temperature-driven Mott transition from a low-temperature insulator phase to a high-temperature metal phase. The switching speed, energies, and endurance of the NbO_2-Mott memristors have been evaluated to be less than 2.3 ns, of the order of 100 fJ, and $>10^9$, respectively.[152,153] The programing and read voltages reported so far are <2 V and <0.2 V, respectively.[150] The non-volatile resistive switching of AM_4X_8 single crystals was induced by the electric field of less than 10 kV/cm.[154,155,156,157] This suggests that if the device consisting of a 10-nm-thick AM_4X_8 film is fabricated, the switching voltage will be less than 0.01 V.

Although non-volatile switching has been reported in the devices based on AM_4X_8 and θ-(BEDT-TTF)$_2X$, their retention characteristics are not elucidated in detail.[154,155,156,157,158] In addition, the NbO_2-Mott memristors and VO_2-based devices are volatile switch.[145,146,147,152,153] The retention is thus a major concern of Mott memory. In principle, the Mott transition can be driven even by a small amount of carrier doping to the integer-filling or half-filling valence states of the transition element.[140] However, because of disorders, defects, and spatial variation of chemical composition, a rather large amount of carriers of more than 10^{22} cm^{-3} are required to drive the Mott transition in actual correlated electron materials, resulting in a relatively large switching voltage required in the Mott memory. Therefore, one of the key challenges is the control of crystallinity and chemical

composition in the thin films of correlated electron materials, including the integration of the correlated electron materials onto Si platform. There are some theoretical mechanisms proposed for Mott memories such as the interfacial Mott transition[141] and the formation of conductive filament generated by local Mott transition.[154,156,157] However, a thorough understanding of the mechanism has not been achieved yet. Therefore, the elucidation of detailed mechanism is also a major research challenge.

2.3. MEMORY SELECT DEVICE

The *capacity* (or *density*) is one of the most important parameters for memory systems. In a typical memory system, memory devices (cells) are connected to form an array. A memory cell in an array can be viewed as being composed of two components: the '*storage node'*, which is usually characterized by an element with switchable states, and the '*selector'*, which allows the storage node to be selectively addressed for read and write. Both components impact scaling limits of memory. It should be noted that for several advanced concepts of resistance-based memories, the storage node could in principle be scaled down below 10 nm,[160] and the memory density is often limited by the selector devices. Thus, the selector device represents a serious bottleneck for emerging memory scaling to 10 nm and beyond.

The most commonly used memory selector devices are transistors (e.g., FET or BJT), as in DRAM, FRAM, *etc*. Flash memory is an example of a storage node (floating gate) and a selector (transistor) combined in one device. Planar transistors typically have the footprint around (6-8)F^2. In order to reach the highest possible 2D memory density of $4F^2$, a vertical transistor selector needs to be used. However, transistors as selector devices are generally unsuitable for 3D memory architectures. Two-terminal memory selector devices are preferred for scalability and can be used in crossbar memory arrays to achieve $4F^2$ footprint.[161,162] The function of selector devices is essentially to minimize leakage through unselected paths ("sneak paths"). Two-terminal selector devices can achieve this through asymmetry (e.g., rectifying diodes) or nonlinearity (e.g., nonlinear devices).[163] Volatile switches can also be used as selector devices. Figure BC2.2 shows a taxonomy of memory selector devices. In addition to external selector devices, some storage elements may have inherent self-selecting properties (e.g., intrinsic nonlinearity or self-rectification), which may enable functional crossbar arrays without external selectors.

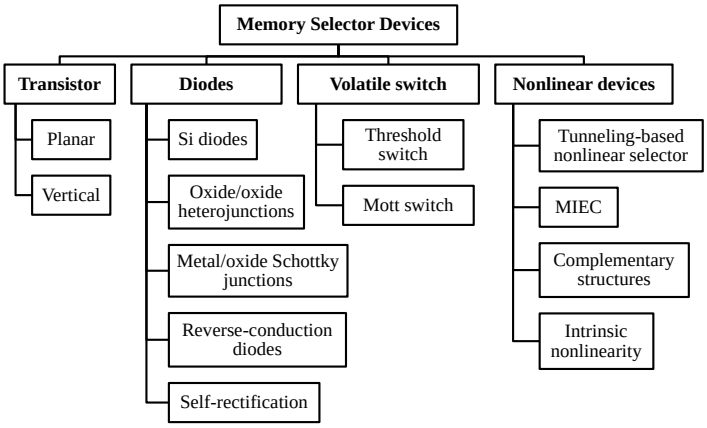


Figure BC2.2. Taxonomy of Memory Select Devices

2.3.1. VERTICAL TRANSISTORS

Several examples of experimental demonstrations of vertical transistors used as selectors in memory arrays are presented in Table BC2.3. While a vertical transistor selector allows for the highest planar array density ($4F^2$), it is challenging to integrate a transistor selector into stacked 3D memory. For example, to avoid thermal stress on the memory elements on the existing layers, the processing temperature of the vertical transistor in 3D stacks must be low. Also, making contact to the third terminal (gate) of vertical transistors constitutes an additional integration challenge, which usually results in cells size larger than ($4F^2$);[164] although true $4F^2$ arrays can, in principle, be implemented with 3-terminal selector devices.[165]

Table BC2.3 Experimental Demonstrations of Vertical Transistors in Memory Arrays

2.3.2. DIODE SELECTOR DEVICES

General requirements for two-terminal selector devices are sufficient ON currents at proper bias to support read and write operations and sufficient ON/OFF ratio to enable selection. The minimum ON current required for fast read operation is ~1 μA (Table BC2.4). The required ON/OFF ratio depends on the size of the memory block, $m \times m$: for example using a standard scheme

of array biasing the required ON/OFF ratio should be in the range of 10^7–10^8 for m=10^3–10^4, in order to minimize the 'sneak' currents.[166] These specifications are quite challenging, and the experimentally demonstrated selector devices can rarely meet them. Thus, selector devices are becoming a critical challenge of emerging memory. It should be noted that different application targets of resistance-based memories also impact selector device requirements.

Table BC2.4 Benchmark Select Device Parameters

The simplest realization of diode selectors uses semiconductor diodes, such as a *pn*-junction diode, Schottky diode, or heterojunction diode. Such devices are suitable for a unipolar memory cell. For bipolar memory cells, selectors with bi-directional switching are needed. Proposed examples include Zener diodes,[167] BARITT diodes,[168] and reverse breakdown Schottky diodes.[169]

2.3.2.1. Si diode Selector Devices

Both single-crystal Si[170] and poly-Si[171,172,173] diodes have been developed as selector devices for PCM arrays. To provide high ON current, the contact resistivity needs to be reduced to $<10^{-7}$ Ω cm^2, which was achieved by engineering the metal electrodes and electrode-Si interface.[171] A short-time annealing technique helps to reduce the OFF current and enlarge the ON/OFF ratio. Poly-Si technology can achieve ON current density of 10^7 A/cm^2 (at ~ 1.8V) and an ON/OFF ratio of 10^8. It is believed that Si diodes can be scaled beyond 20 nm or 10 nm. Poly-Si diode selector devices have been integrated in PCM crossbar arrays, 3D vertical chain-cell type PCM,[172] and a 1 Gb PCM test chip.[173] A major challenge of Si diodes is the high processing temperature (above 1000°C) required to crystallize Si to reduce contact resistivity and OFF current.

2.3.2.2. Oxide Diode Selector Devices

Oxide-based heterojunction[174,175,176,177] or Schottky junction[180,181,182,183] diodes may be fabricated at lower temperatures and used as selector devices. They are particularly suitable for oxide-based RRAM devices. A p-NiO_x/n-TiO_x diode has demonstrated a rectification ratio of 10^5 at ±3V and ON current density of 5×10^3 A/cm^2 (at ~ 2.5V)[174]. A p-CuO_x/n-$InZnO_x$ diode achieved higher ON current density of 10^4 A/cm^2 (at ~ 1.3V) and was integrated with NiO_x RRAM in a 2-layer 8×8 crossbar array[175,176] and with Al_2O_3 antifuse in a one-time-programmable (OTP) memory.[177] Si substrates can be used as a part of heterojunction diodes as demonstrated in n-ZnO/p-Si[178] and n-Ge-nanowire/p-Si diodes.[179] In TiO_x-based diodes with Pt electrodes, temperature-dependent current-voltage (I-V) characteristics confirm a Schottky barrier of ~0.55 eV at the TiO_x/Pt interface.[180] The rectification ratio is ~ 1.6×10^4 at ±1V but ON current density is low (~ 13A/cm^2) due to large size. A Pt/TiO_2/Ti diode with Pt as the Schottky contact and Ti the ohmic contact achieved higher rectification ratio of 10^7 – 10^9 at ±1V.[181] Another demonstration of Pt/TiO_2/Ti Schottky diodes improved ON current density to ~ 3×10^5 A/cm^2 at 2 V on a 4 μm^2 area.[182] Measurement showed that current is not uniform across the diode area, probably due to edge leakage. Therefore, current density is higher at smaller diode size. An Ag/n-ZnO Schottky diode with non-alloyed Ti/Au ohmic contact demonstrated a rectification ratio of 10^5 and forward current density over 10^4 A/cm^2 at 2 V.[183] In addition to oxide Schottky diodes, Si Schottky diodes are also utilized as selector devices, e.g., Al/p-Si.[184] The ON current of oxide-based heterojunction diodes is often limited by both contact resistance and density of states of the oxide materials.

2.3.3. Volatile Switch as Selector Devices

Volatile resistive switching devices can also be utilized as selector devices. They provide access to a selected memory element in their ON state and block sneak paths in OFF state. The device structure and physics of operation of these devices are sometimes similar to those of the storage nodes. The main difference is that nonvolatility is required for the storage node, while for select devices volatile switching characteristics allow them to be switched quickly between ON and OFF states.

2.3.3.1. Mott Switch

This device is based on metal-insulator transition (i.e., Mott transition) and exhibits a low resistance above a critical electric field (threshold voltage, V_{th}). It recovers to a high-resistance state if the voltage is below a hold voltage (V_{hold}). If the electronic conditions that triggered Mott transition can relax within the memory device operation time scale, the Mott transition device is essentially a volatile resistive switch and can be utilized as a selector device. A VO_2-based device has been demonstrated as a selector device for NiO_x RRAM element.[185] However, the feasibility of Mott-transition switches as selector devices still needs further research. It should be noted that VO_2 undergoes a phase transition to the metallic state at temperature around 68°C, which restricts its operation temperatures and limits practical applications of a VO_2 selector as current specifications require operational temperature of 85°C. Suitable Mott materials with higher transition temperatures need to be investigated. Metal insulator transitions at ~ 130°C, and electrically driven switching were observed in thin films of $SmNiO_3$ [186].

2.3.3.2. THRESHOLD SWITCH

This type of device is based on the threshold-switching effect observed in thin-film MIM structures caused by electronic charge injection. Significant resistance reduction occurs at V_{th}, and this low-resistance state quickly recovers to the original high-resistance state when the applied voltage falls below V_{hold}. It was reported that chalcogenide-based threshold switches could be used as access devices in PCM arrays.[187] Niobium oxide is found to possess both memory switching and threshold switching properties at different compositions, based on which hybrid memory (W/bi-layer-NbO_x/Pt) was demonstrated in a 1kb array.[188] NbO_x-based selectors have also been integrated with TiO_x/TaO_x based RRAM in crossbar arrays at 5xnm node.[189] In Si-As-Te ternary alloy, the composition (controlled by the sputtering power during deposition) determines the emergence of threshold switching.[190] Both V_{th} and V_{hold} vary with composition, which may provide a method to optimize the selector device operation window. Another threshold switch device based on chalcogenide AsTeGeSiN was shown to be scalable to 30nm with current density exceeding 10MA/cm^2 and endurance over 10^8 cycles.[191,192] It was integrated with TaO_x-based RRAM devices. An unavoidable finite delay time was found in this selector device due to intrinsic properties of the chalcogenide material, which may limit the selector speed. Another doped-chalcogenide (material undisclosed) based selector demonstrates low V_{hold} (0.2 V), large ON/OFF ratio (>10^7), fast speed (<10 ns), long endurance (>10^9 cycles) and good thermal stability (180°C).[193] A so-called "FAST" (Field Assisted Superliner Threshold) selector was recently reported, with abrupt switching (<5 mV/dec), high ON/OFF ratio (10^7), and long endurance (10^8 cycles).[194] Unlike other threshold switch selectors, this device does not exhibit recovery to OFF-state at certain V_{hold}, which appears more like a nonlinear selector. A 4Mb 1S1R crossbar RRAM array has been demonstrated based on this selector.

2.3.4. NONLINEAR SELECTOR DEVICES

Similar to volatile switches, nonlinear selector devices can be used with bipolar memory elements, which is an advantage over rectifying diode selectors.

2.3.4.1. NONLINEAR SELECTOR DEVICES

Nonlinearity in device characteristics can be introduced with non-ohmic transport mechanisms, e.g., tunneling. A Ni/TiO_2/Ni nonlinear selector device is integrated with HfO_2-RRAM to demonstrate a 1S1R memory structure.[195] Another selector device with Pt/TiO_2/TiN structure is combined with a bi-layer Pt/TiO_{2-x}/TiO_2/W RRAM for a functional memory device.[196] A so-called "varistor" selector device is based on a sandwiched TaO_x/TiO_2/TaO_x structure.[197] It was found that the substitution of Ti^{4+} in TiO_2 by Ta^{5+} ions increases the conductivity of the initially insulating TiO_2 layer. The ON-current of nonlinear selector devices can be modulated by oxide thickness and oxidation conditions. Another multi-oxide stack (Ta_2O_5/TaO_x/TiO_x) based selector also leverages various interface engineering techniques to obtain high ON-current density (>10^7 A/cm^2), high nonlinearity ratio (~10^4), and low OFF-current (<100 nA).[198] It is integrated with CBRAM in a 1 kb crossbar array. A back-to-back diode structure, $n^+/p/n^+$ poly-Si, is also suggested as a selector device, where the middle p-layer is fully depleted and a drain induced barrier lowering (DIBL) effect causes exponential current increase with applied voltage.[199]

2.3.4.2. MIEC SWITCH

The device is made from Cu-containing "mixed ionic and electronic conduction" (MIEC) materials sandwiched between an inert top electrode (TE) (e.g., TiN, W) and a bottom electrode (BE). Negative voltage applied on TE pulls Cu^+ in MIEC away from the BE and creates vacancies near the BE. The hole and vacancy concentrations depend exponentially on the applied voltage. Symmetrical diode-like I-V characteristics are achieved with two inert electrodes. Large fraction of mobile Cu^+ enables high current density (> tens of MA/cm^2).[200] Endurance above 10^8 cycles has been demonstrated on MIEC devices in small arrays.[201] The MIEC selector devices were also integrated with PCM in a 512 kb testing array using 180nm CMOS process.[202] The scalability of MIEC select devices was tested to below 30nm in diameter and below 12nm in thickness.[203]

2.3.4.3. COMPLEMENTARY RESISTIVE SWITCHES

A complementary resistive switch (CRS) provides a self-selecting memory by connecting two bipolar RRAM devices anti-serially.[204] It may be considered as "constructed nonlinearity". Both states "0" and "1" have high resistance in CRS, which helps to minimize leakage through sneak paths. In either state, one of the two RRAMs is in LRS and the other in HRS. When reading a "1" state, the HRS device is switched to LRS and both devices end up in LRS. When reading a "0" state, no switching occurs and CRS remains in HRS. Notice that the reading operation is destructive, although non-destructive readout method was also proposed.[205] CRS has been demonstrated in different resistive switching devices, e.g., Cu/SiO_2/Pt bipolar resistive switches,[206] amorphous carbon-based RRAM,[207] TaO_x–based RRAM,[208] multi-layer TiO_x device,[209] HfO_x RRAM,[210] ZrO_x/HfO_x bi-layer RRAM,[211] Cu/TaO_2 atomic switch,[212] Nb_2O_{5-x}/NbO_y RRAM,[213] *etc.*

Table BC2.5a summarizes experimentally demonstrated parameters of some two-terminal select devices, including diodes, volatile switches, and nonlinear devices. Table BC2.5b summarizes the parameters of some reported self-rectifying memories. It should be emphasized that these summary tables can only capture a snapshot of selector device characteristics; however, the functionality of these devices depends on their actual voltage in arrays with random data patterns and the balance between

selectors and storage elements. Therefore, these parameter tables should only be used for illustration purpose, not for rigorous benchmark or assessment.

It remains a great challenge for the demonstrated selector devices to meet all the requirements in Table BC2.4. For scaled two-terminal select devices, two fundamental challenges are *contact resistance*[171] and *lateral depletion effects.*[214,215] Very high doping concentration is needed to minimize both effects. However, high doping concentrations result in increased reverse bias currents in classical diode structures and therefore reduced I_{on}/I_{off} ratio. For switch-type selector devices the main challenges are identifying the right material and the switching mechanism to achieve the required drive current density, I_{on}/I_{off} ratio, and reliability.

Table BC2.5a Experimentally Demonstrated Two-terminal Memory Select Devices

Table BC2.5b Experimentally Demonstrated Self-selecting Memory Devices (self-rectifying)

2.4. STORAGE CLASS MEMORY

2.4.1. STORAGE CLASS MEMORY DEVICES

2.4.1.1. TRADITIONAL STORAGE: HDD AND FLASH SOLID-STATE DRIVES

Conventionally, magnetic hard-disk drives are used for non-volatile data storage. The cost of HDD storage in $/GB is extremely low and continues to decrease. Although the bandwidth with which contiguous data can be streamed is high, the poor random-access time of HDDs limits the maximum number of I/O requests per second (IOPs). In addition, HDDs have relatively high energy consumption, a large form factor, and are subject to mechanical reliability failures in ways that solid state technologies are not. Despite these issues, the sheer number and growth in HDD shipments per year (380,000 Petabytes in 2012, growing at 32% per year) means that magnetic disk storage is highly unlikely to be "replaced" by solid-state drives at any time in the foreseeable future.[216]

Non-volatile semiconductor memory in the form of NAND Flash has become a widely used alternative storage technology, offering faster access times, smaller size and lower energy consumption when compared to HDD. However, there are several serious limitations of NAND Flash for storage applications, such as poor endurance (10^3–10^5 erase cycles), only modest retention (typically 10 years on a new device, but only 1 year at the end of rated endurance lifetime), long erase time (~ms), and high operating voltage (~15 V). Another difficult challenge of NAND Flash SSD is posed by its page/block-based architecture. By not allowing for direct overwrite of data, sophisticated procedures for garbage collection, wear-leveling and bulk erase are required. This in turn requires additional computation – which reduces performance and increases cost and power because of the need for a local processor, RAM, and logic – as well as over-provisioning of the SSD which further increases cost per effective user-bit of data.[217]

Although Flash memory technology continues to project for further density scaling, inherent performance characteristics such as read, write and erase latencies have been nearly constant for more than a decade.[218] While the introduction of multi-level cell (MLC) Flash devices extended Flash memory capacities by a small integral factor (2–4), the combination of scaling and MLC have resulted in the degradation of both retention time and endurance, two parameters critical for storage applications. The migration of NAND Flash into the vertical dimension above the silicon has continued this trend of improving bit density (and thus cost-per-bit) while maintaining or in some cases, even slightly degrading the latency, retention, and endurance characteristics of present-day NAND Flash.

This outlook for existing technologies has opened interesting opportunities for prototypical and emerging research memory technologies to enter the non-volatile solid-state-memory space.

2.4.1.2. WHAT IS STORAGE CLASS MEMORY?

Storage-class memory (SCM) describes a device category that combines the benefits of solid-state memory, such as high performance and robustness, with the archival capabilities and low cost of conventional hard-disk magnetic storage.[219,220] Such a device requires a non-volatile memory (NVM) technology that could be manufactured at a very low cost per bit.

A number of suitable NVM candidate technologies have long received research attention, originally under the motivation of readying a "replacement" for NAND Flash, should that prove necessary. Yet the scaling roadmap for NAND Flash has progressed steadily so far, without needing any replacement by such technologies. So long as the established commodity continues to scale successfully, there would seem to be little need to gamble on implementing an unproven replacement technology instead.

However, while these NVM candidate technologies are still relatively unproven compared to Flash, there is a strong opportunity for one or more of them to find success in applications that do not involve simply "replacing" NAND Flash. Storage Class Memory can be thought of as the realization that many of these emerging alternative non-volatile memory technologies can potentially offer significantly *more* than Flash, in terms of higher endurance, significantly faster performance, and direct-byte access capabilities. In principle, Storage Class Memory could engender two entirely new and distinct levels within the memory and storage hierarchy. These levels would be differentiated from each other by access time, with both levels located within more than two orders of magnitude between the latencies of off-chip DRAM (~80 ns) and NAND Flash (20 µs).

2.4.1.2.1. STORAGE-TYPE SCM

The first new level, identified as S-type storage-class memory (S-SCM), serves as a high-performance solid-state drive, accessed by the system I/O controller much like an HDD. S-SCM must provide at least the same data retention as Flash, allowing S-SCM modules to be stored offline, while offering new direct overwrite and random-access capabilities (which can lead to improved performance and simpler systems) that NAND Flash devices cannot provide. However, because of the modest (perhaps 10x) advantage in read latency over NAND Flash, it is critical that the eventual cost-per-bit for S-SCM be no worse than 3-10x higher than NAND Flash. While such costs need not be realized immediately at first introduction, it would need to be very clear early on that costs could steadily approach such a level relative to Flash.

Note however that such system cost reduction can come from other sources than the raw cost of the device technology: a slightly-higher-cost NVM technology that enabled a simple, low-cost SSD by eliminating or simplifying costly and /or performance-degrading overhead components would achieve the same overall goal. If the cost per bit could be driven low enough through ultrahigh memory density, ultimately such an S-SCM device could potentially replace magnetic hard-disk drives in enterprise storage server systems as well as in mobile computers (subject to the same issues mentioned above in terms of needing numerous IC fabs to ship the many petabytes of HDD delivered to those markets[216]).

2.4.1.2.2. MEMORY-TYPE SCM

The second new level within the memory and storage hierarchy, termed M-type storage-class memory (M-SCM), should offer a read/write latency of less than ~200 ns. These specifications would allow it to remain synchronous with a memory system, allowing direct connection from a memory controller and bypassing the inefficiencies of access through the I/O controller. The role of M-SCM would be to augment a small amount of DRAM to provide the same overall system performance as a DRAM-only system, while providing moderate retention, lower power-per-GB and lower cost-per-GB than DRAM. Again, as with S-SCM, the cost target is critical. It would be desirable to have cross-use of the same technology in either embedded applications or as a standalone S-SCM, in order to spread out the development risk of an M-SCM technology. The retention requirements for M-SCM are less stringent, since the role of non-volatility might be primarily to provide full recovery from crashes or short-term power outages, requiring non-volatility over a period of perhaps 7–21 days.

Particularly critical for M-SCM will be device endurance, since the time available for wear-leveling, error-correction, and other similar techniques is limited. The volatile portion of the memory hierarchy will have effectively infinite endurance compared to any of the non-volatile memory candidates that could become an M-SCM. Even if device endurance can be pushed well over 10^9 cycles, it is quite likely that the role of M-SCM will need to be carefully engineered within a cascaded-cache or other Hybrid Memory approach.[221] That said, M-SCM offers a host of new opportunities to system designers, opening up the possibility of programming with truly persistent data, committing critical transactions to M-SCM rather than to HDD, and performing commit-in-place database operations.

2.4.1.3. TARGET SPECIFICATIONS FOR SCM

Since the density and cost requirements of SCM transcend the straightforward scaling application of Moore's Law, additional techniques will be needed to achieve the ultrahigh memory densities and extremely low cost demanded by SCM, such as 1) 3-D integration of multiple layers of memory, currently implemented commercially for write-once solid-state memory,[222] and/or 2) Multiple level cell (MLC) techniques.

Table BC2.6 lists a representative set of *target* specifications for SCM devices and systems compared with benchmark parameters of existing technologies (HDD and NAND Flash). As described above, SCM applications can be expected to naturally separate based on latency. Although S-class SCM is the slower of these two targeted specifications, read and write latencies should be in the 1–5 µsec regime in order to provide sufficient performance advantage over NAND Flash. Similarly, endurance of S-class SCM should offer at least 1 million program-erase cycles, offering a distinct advantage over NAND Flash. In order to support off-line storage, 10-year retention at 85°C should be available.

In order to make overall system power usage (as shown in Table BC2.6) competitive with NAND Flash and HDD, and since faster I/O interfaces can be expected to consume considerable power, the device-level power requirements must be extremely minimal. This is particularly important since low latency is necessary but not sufficient for enabling high bandwidth – high parallelism is also required. This in turn mandates a sufficiently low power per bit access, both in terms of peripheral circuitry

and device-level write and read power requirements. Finally, standby power should be made extremely low, offering opportunities for significant system power savings without loss of performance through rapid switching between active and standby states.

In order to achieve the desired cost target of within 3–10x of the cost of NAND Flash, the effective areal density will similarly need to be quite similar to 1X-node planar NAND Flash. This low cost structure would then need to be maintained by subsequent SCM generations, through some combination of further scaling in lateral dimension, by increasing the number of multiple layers, or by increasing the number of bits per cell.

Also shown in Table BC2.6 are the target specifications for M-type SCM devices. Given the faster latency target (which enables coherent access through a memory controller), the program-erase cycle endurance must be higher, so that the overall non-volatile memory system can offer a sufficiently large lifetime before needing replacement or upgrade. Although some studies have shown that a device endurance of 1e7 cycles is sufficient to enable device lifetimes on the order of 3–10 years,[223] we anticipate that the need for sufficient engineering margin would suggest a minimum cycle endurance of 1e9 cycles. While such endurance levels support the use of M-class SCM in memory support roles, significantly higher endurance values (e.g., 1e12 or 1e14 cycles) would allow M-class SCM to be used in more varied memory applications, where the total number of memory accesses may become very large.

Table BC2.6 Target Device and System Specifications for SCM

Table BC2.7 Potential of Current Prototypical and Emerging Research Memory Candidates for SCM Applications

2.4.1.4. First SCM Products Reach the Market

In July 2015, a new non-volatile memory technology called "3D-Xpoint" was announced. This technology is said to offer 1000x lower latency and 1000x higher endurance than NAND Flash, at a density that is 10x higher than DRAM.[224,225] (Note that it is most likely that the latency referred to here is write latency rather than read latency, since NAND write latency is much slower than its read latency.) 3D-Xpoint technology, said to have been implemented at the 128Gbit chip level, is based on a two-layer stacked crossbar array, with each intersection point containing a non-volatile memory device and a nonlinear access device.[226,227] The particular non-volatile memory device was not specified, other than that it depends on bulk changes of resistance,[228] nor was the nonlinear access device described. Speculation based on patent searches and job solicitations suggest that the technology may be a combination of some variant of phase change memory and an Ovonic Threshold Switching access device.[228]

While the details of the devices involved may still be uncertain, the projected array specifications and the target applications are, for all intents and purposes, indistinguishable from those described above for S-type Storage Class Memory. Thus we can consider 3D-Xpoint as the first commercial implementation of the Storage Class Memory concept first described in 2008.[219,220] Furthermore, in a later presentation, a second, "Performance-focused" form of 3D-Xpoint memory was described as being under active development.[229] Compared to the initial "Cost-focused" form of 3D-Xpoint memory, this variant is said to offer even faster latencies and higher endurance (Figure BC2.3). Thus, this second variant of 3D-Xpoint is somewhat similar to M-type SCM as described above, both in terms of its specifications and in terms of potential applications. The only major difference, as observed in Figure BC2.3, is the strong similarity between the expected volatility of Performance-focused 3D-Xpoint and the known volatility of DRAM. In contrast, one of the benefits of M-type SCM was supposed to be its non-volatility. Ideally, retention of data for perhaps 1-3 weeks would permit successful recovery of server data, even after a power outage due to a natural disaster or other major event.

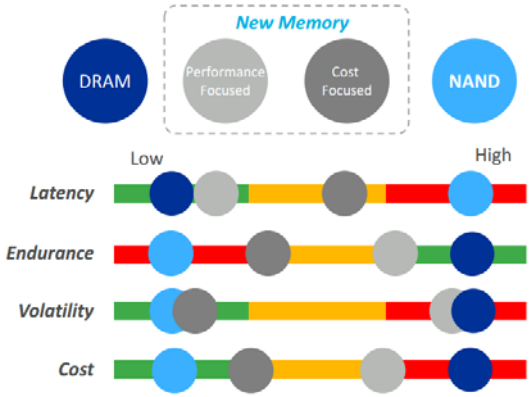


Figure BC2.3 Comparison of Performance of Different Memory Technologies

2.4.2. STORAGE CLASS MEMORY ARCHITECTURES

2.4.2.1. INTRODUCTION

In traditional computing, SRAM is used as a series of caches, which DRAM tries to refill as fast as possible. The entire system image is stored in a non-volatile medium, traditionally a hard drive, which is then swapped to and from memory as needed. However, this situation has been changing rapidly. Application needs are both scaling in size and evolving in scope, and have rapidly exhausted the capabilities of the traditional memory hierarchy.

By combining the reliability, fast access, and endurance of a solid-state memory together with the low-cost archival capabilities and vast capacity of a magnetic hard disk drive, Storage Class Memory (SCM) offers several interesting opportunities for creating new levels in the memory hierarchies that could help with these problems. SCM offers compact yet robust non-volatile memory systems with greatly improved cost/performance ratios relative to other technologies. S-class SCM represents ultra-fast long-term storage, similar to an SSD but with higher endurance, lower latencies, and byte-addressable access. M-class represents dense and low-power non-volatile memory at speeds close to DRAM.

In order to implement SCM, both the emerging memory technologies discussed in Section 2.4.1 as well as new interfaces and architectures will be needed, in order to fully use the potential and to compensate for the weaknesses of various new memory technologies. In this section, we explore the Emerging Research Architecture implications and challenges associated with Storage Class Memory.

2.4.2.2. CHALLENGES IN MEMORY SYSTEMS

Current memory systems range in size from Gigabytes (low-volume ASIC systems, FPGAs and mobile systems) through Terabytes (multicore systems that manage execution of many threads for personal or departmental computing), to Petabytes (for database, Big Data, cloud computing, and other data analytics applications), and up to Exabytes (next-generation, exascale scientific computing). In all cases, speed (both in terms of latency of data reads and writes as well as bandwidth), power consumption, and cost are absolutely critical. However, the importance of other system aspects can vary across these different application spaces.

Historically, roughly one-third of the power in a large computer system is consumed in the memory sub-system.[230] Some portion of this is refresh power, required by the volatile nature of DRAM. As a result, modern data servers consume considerable power even when operating at low utilization rates. For example, it has been reported that servers are typically operating at over 50% of their peak power consumption even at very low utilization rates.[231] The requirement for rapid transition to full operation precludes using a hibernate mode. As a result, a persistent memory that did not require constant refresh would be valuable.

Many computer systems are not running at peak load continuously. Such systems (including mobile or data analytics) become much more efficient if power can be turned off rapidly while maintaining persistent stored data, since power usage can then become proportional to the instantaneous computational load. This provides additional incentive for the non-volatile storage aspect of SCM.

Some applications such as data analytics and ASIC systems can benefit from having associative memories or content addressability, while other applications might gain little. Mobile systems can become even more compact if many different memory tiers can be combined on the same chip or package, including non-volatile M-class or even S-class Storage Class Memory.

Total cost of ownership is influenced by cost-to-purchase, cost-to-maintain, and system lifetime. Current cost-to-purchase trends are that Hard Disk Drives (HDD) cost roughly an order of magnitude less per bit than Flash memory, which in turn costs almost an order of magnitude less per bit than DRAM. However, cost-to-purchase is not the only consideration. It is anticipated that S-class SCM will consume considerably less power than HDD (both directly and in terms of required cooling), and will take up considerably less floorspace. One early projection what that by 2020, if the main storage system of a data center is still built solely from HDD, the target performance of 8.4 G-SIO/s could consume as much as 93 MW and require 98,568 square feet of floor space.[232] In contrast, the improved performance of emerging memories could supply this performance with only 4 kW and 12 square feet. Given the cost of energy, this differential can easily shift the total cost advantage to emerging memory, away from HDD, even if a cost per bit differential still exists.

These requirements have led to considerable early investigation into new memory architectures, exploiting emerging memory devices, often in conjunction with DRAM and HDDs in novel architectures. These new Storage Class Memories (SCM) are differentiated as whether they are intended to be close to the CPU (M-class) or to largely supplement the hard-drives and SSDs (S-class).

The emergence of SCM leads to the need to resolve issues beyond the device level, including software organization, wear leveling management, and error management. Because of the inherent speed in SCMs, software can easily limit the system performance. Some of these changes have already been initiated by the advent of SSDs. All types of IO software – from the filesystem, through the operating system and up to applications – had to be redesigned in order to best leverage both SSDs and then SCMs. The number of software interactions was reduced, and disk-centric features were removed. Inefficiencies buried deep within conventional software were accounting for anywhere from 70% to 94% of the total IO latency.[233] It is likely to be valuable to give application software direct access to the SCM interface, although this can then require additional considerations to protect the SCM device from malicious software. This direct access has not occurred for SSDs, with manufacturers applying numerous undocumented operations between the input data and the raw storage. (One example is the inversion of entire data blocks, based on the number of 0s or 1s to be stored.) However, this approach is not typically used in current operating systems that use some form of File Address Table as an intermediate index mechanism.

Access patterns in data-intensive computing can vary substantially. While some companies continue to use relational databases, others have switched to flat databases that must be separately indexed to create connections amongst entries. In general, database accesses tend to be fairly atomic (as small as a few bytes) and can be widely distributed across the entire database. This is true for both reads and writes, and since the relative ratio of reads and writes varies widely by application, the optimality of any one design can depend strongly on the particular workload.

A specific issue that arises with SCMs is wear leveling. While DRAMs and HDDs can support a large number of writes to the same location without failure, most of the emerging non-volatile memory device technologies cannot. Thus, there is a need for low-overhead mechanisms to "spread" the writes around uniformly, generally referred to as "wear leveling". An important issue in any file system is that certain data (such as metadata) is written to quite frequently. It is important to make sure that such storage locations are not subject to fast wearout, e.g. by using a more robust technology for such portions of the file system.

Error management is a broader problem than just wear leveling. While DRAM has traditionally benefited from simple methods such as ECC and EDCs, Flash with its large page sizes and slow accesses can afford more sophisticated algorithms such as LDPC. Unfortunately, SCM will need more error correction than DRAM but will need faster error correction than Flash, especially for M-class SCMs. This is an open area for research. Some possible options include exploring codes that exploit specifics of error patterns, such as Tensor codes, and the use of in-situ scrub,[234] where accumulated errors are periodically eliminated so that one or two-bit error correction can remain sufficient.

2.4.2.3. Emerging Memory Architectures for M-Class SCM

Storage Class Memory architectures that are intended to replace, merge with, or support DRAM, and be close to the CPU, are referred to as M-type or Memory-type SCM (M-SCM). The required properties of this memory have many similarities to DRAM, including its interfaces, architecture, endurance, and read and write speed. Since write endurance of an emerging research memory is likely to be inferior to DRAM, considerable scope exists for architectural innovation. It will be necessary to choose how to integrate multiple memory technologies to optimize performance and power while maximizing lifetime. In addition, advanced load leveling that preserves the word level interface and suitable error correction will be needed.

The interface is likely to be a word-addressable bus, treating the entire memory system as one flat address space. Since the cost of adapting to new memory interfaces is sizeable, an interface standard that could support multiple generations of M-SCM devices would be highly preferred. Many systems (such as in automobiles) might be deployed for a long time, so any new standard should be backward-compatible. Such a standard should compatible to DRAM interfaces (though with simpler control commands) and should reuse existing controllers and PHY (physical layers), as well as power supplies, as much as possible. It should be power efficient, e.g. supporting small page sizes, and should support future directions, such as 3D Master/slave configurations. The M-

SCM device should indicate when writes have been completed successfully. Finally, an M-SCM standard should support multiple data rates, such as a DDR-like speed for the DRAM and a slower rate for the NVRAM.[235]

While wear-leveling in a block-based architecture requires significant overhead to track the number of writes to each block, simple techniques such as "Start-Gap" Wear-Leveling are available for direct-byte-access memories such as PCM (Phase Change Memory).[236] In this technique, a pair of registers are used to identify the location of the start point and an empty gap within a region of memory. After some threshold number of write accesses, the gap register is moved through the region, with the start register incrementing each time the gap register passes through the entire region. Additional considerations can be added to defend against detrimental attacks intended to intentionally wear out the memory.

With such techniques, even an M-class SCM that is markedly slower than DRAM can offer improved performance by increasing available capacity and by reducing the occurrence of costly cache misses.[237] With proper caching, a carefully-designed M-SCM system could potentially even match DRAM performance despite its lower device latency.[238] The presence of a small DRAM cache helps keep the slower speed of the M-class SCM from affecting overall system performance in many common workloads. Even with an endurance of 1e7 cycles, the system lifetime has been shown to be on the order of 3 years. Techniques for reducing the write traffic back to the SCM device can help improve this by as much as a factor of 3 under realistic workloads.

Direct replacement of DRAM with a slightly slower M-class SCM has also been considered, for the particular example of STT-MRAM.[239] Since individual byte-level writes to STT-MRAM consume more power than in DRAM, a direct replacement is not competitive in terms of energy or performance. However, by re-architecting the interaction between the output buffer and the STT-MRAM, unnecessary writes back to the NVM can be eliminated, producing a sizeable energy improvement at almost no loss in performance. However, the use of write buffers means that the device must be able to complete all writes back to non-volatile memory in the event of power loss. Integrating PCM into the mobile environment, together with a redesigned memory management controller, is predicted to deliver a six times improvement in speed and also extends the memory lifetime six times.[240]

Caches are intended to ensure that frequently needed data is located near to the processor, in nearby, low-latency memory. In storage architectures, "hot" or frequently accessed data is identified and then moved to faster tiers of storage. However, as the number of tiers or caches increases, a significant amount of time and energy is being spent moving data. An alternative approach is to completely rethink the hardware/software interface. By organizing the computational system around the data, data is not brought to the processor but instead processing is performed in proximity to the stored data. One such emerging data-centric chip architectures termed "Nanostores"[241] was predicted to offer 10–60x improvements in energy efficiency.[242]

Given the slower than expected deployment of scaled emerging devices for M-class SCM, several projects have employed large amounts of DRAM as a surrogate for and M-class SCM. Though Bresniker et.al. describe a computer enabled by a large non-volatile "Universal memory,"[243] press reports indicate that early commercial machines will be built with large amounts of DRAM. They point out that an NVM version allows "occasionally-on computing" but could have the downside that new types of bugs might appear as OSs and programs effectively run indefinitely and cannot "re-create their memory state representations each time they start". New applications and algorithms might emerge as a result of keeping data in perpetuity, or at least for long periods of time.

2.4.2.4. Emerging Memory Architectures for S-Class SCM

S (Storage) type SCMs are intended to replace or supplement hard-disk drives as main storage, much like current Flash-based SSDs, but with even more IOPs (I/O operations per second). Their main advantage will be speed, avoiding the seek time penalty of main drives. However, to succeed, their total cost of ownership needs to approach that of HDDs. Research issues include whether the SCM serves as a disk cache or is directly managed, how load leveling is implemented while retaining a sufficiently fast and flexible interface, how error correction is implemented, and identifying the optimal mix of fast-yet-expensive and slow-yet-inexpensive storage technologies. The effective performance of Flash SSD, itself slower than S-SCM, has been strongly affected by interface performance. For instance, the SATA (Serial Advanced Technology Attachment) interface was originally designed for HDD, and was commonly used for early SSD devices despite not being optimized for Flash SSD.[244]

One possible introduction of these new memory devices to the market would be as *hybrid* solid-state discs, where the new memory technology complements the traditional Flash memory to boost the SSD performance. Experimental implementations of FeRAM/Flash[245]and PCRAM/Flash[246] have been explored. It was shown that the PCRAM/Flash hybrid improves SSD operations by decreasing the energy consumption and increasing the lifetime of Flash memory.

Additional open questions for S-SCM include storage management, interface, and architectural integration, such as whether such a system should be treated like a fast disk drive or as a managed extension of main memory. To date, disk-like systems built using non-volatile memories have had disk-like interfaces, with fixed-sized blocks and a translation layer used to obtain block addresses.

However, since the file system also performs a table lookup, some portion of SCM performance is sacrificed. In addition, non-NAND-Flash SCMs have randomly accessible bits and do not need to be organized as fixed-size blocks.[247]

While preserving this two-table structure means that no changes to the operating system are required to use or to switch between new S-SCM technologies, the full advantages of such fast storage devices cannot be realized. There are two alternative approaches to eliminate one of these lookup tables. In the Direct Access mode, the translation table is removed, so that the operating system must then understand how to address the SCM devices. However, any change in how table entries are calculated (such as improvements in garbage collection or wearleveling) would then require changes in the operating system.

In contrast, in an Object-Based access model, the file system is organized as a series of (key, value) objects. While this requires a one-time change to operating systems, all specific details of the SCM could be implemented at a low level. This model leads to greater efficiency in terms of both speed and effective "file" density and also offers the potential for enhanced reliability.

Another issue for SCM-based systems will be addressing the asymmetry between read and write in devices such as PCM or other emerging non-volatile memories.[248] Such asymmetry can affect the ordering and atomicity of writes and needs to considered in system or algorithm design.[249] Atomicity is critical for operations such as database transactions properties, so that either all of a series of related database operations occur, or none of them occur.

Longer write latencies, in technologies such as PCM, can be compensated by techniques such as data comparison writes,[250] partial writes,[251] or specialized algorithms/structures that trade writes for reads.[252,253] (These last set of techniques can also help reduce endurance problems.) Write ordering and atomicity problems can be finessed by hardware primitives. These can either be existing hardware primitives – cache modes (e.g., write-back, write-combining), memory barriers, cache line flush[254,255,256] – or newly-proposed hardware primitives, such as atomic 8-byte writes and epoch barriers.[257,258]

Even first-generation PCM chips, although implemented without a DRAM cache, compare favorably with state-of-the-art SSDs implemented with NAND Flash, particularly for small (<2 KB) writes and for reads of all sizes.[259] The CPU overhead per input-output operation is also greatly reduced. Another observation for even first-generation PCM chips is that while the average read latency is similar to NAND Flash, the worst-case latency outliers for NAND Flash can be many orders of magnitude slower than the worst-case PCM access. This is particularly important considering that such S-class SCM systems will typically be used to increase system performance by improving the delivery of urgently needed "hot" data.

Another new software consideration for both S- and M-class SCM is the increased importance of avoiding memory corruption, either through memory leaks, pointer errors, or other issues related to memory allocation and deallocation.[260] Since part of the memory system is now non-volatile, such issues are now pervasive and may be difficult to detect and remove without affecting stored user data.

General libraries and programming interfaces – such as NV-heaps,[261] Mnemosyne,[262] NVMalloc,[263] and recovery and durable structures[264] – have been proposed to expose SCM as a persistent heap and thus ease its adoption. Schemes for filesystem support have been developed to transparently utilize as byte-addressable persistent storage, including Intel's PMFS,[265] BPFS, FRASH,[266] ConquestFS,[267] and SCMFS.[268]

Table BC2.8. *Likely Desirable Properties of M (Memory) Type and S (Storage) Type Storage Class Memories*

3. EMERGING LOGIC AND ALTERNATIVE INFORMATION PROCESSING DEVICES

3.1. TAXONOMY

One of the central objectives of this chapter is to review recent research in devices beyond silicon transistors and to forecast the development of novel logic switches that might replace the silicon transistor as the device driving technological development within the semiconductor industry. Such a replacement is thought to be potentially viable if one or more of the following capabilities is afforded by a novel device: 1) an increase in device density (and corresponding decrease in cost) beyond that achievable by ultimately scaled CMOS; 2) an increase beyond CMOS in switching speed, *e.g.*, through improvements in the normalized drive current or reduction in switched capacitance; 3) a reduction beyond CMOS in switching energy, associated with a reduction in overall circuit energy consumption; or 4) the enabling of novel information processing functions that cannot be performed as efficiently using conventional CMOS.

With the evolution of the Roadmap from the ITRS to the IRDS, an expanded focus on systems requires also that one evaluate the applicability of these novel devices for new types of systems and architectures, above and beyond the hierarchical influence of devices via small core circuits or functional building blocks. Historically, this evaluation has been conducted in this section in terms of possible applications for alternative information processing devices (i.e., those very unlike CMOS transistors). Beginning with the 2017 Edition of the IRDS, the focus pivots further toward architectures and applications that depart significantly from the device→circuit→logic gate→functional block→system paradigm. Primarily, in this Edition, the focus for these departures is detailed in Sections 4 and 5 of this chapter. As future editions emerge, more details will be codified in this section to provide stronger linkages to alternative systems and architectures.

For 2017, the organization of this section is intended to reflect a progression of options that might enable an orderly transition from CMOS to devices that depart increasingly from CMOS in terms of structure, materials, or operation. That organization is depicted in Figure BC3.1.

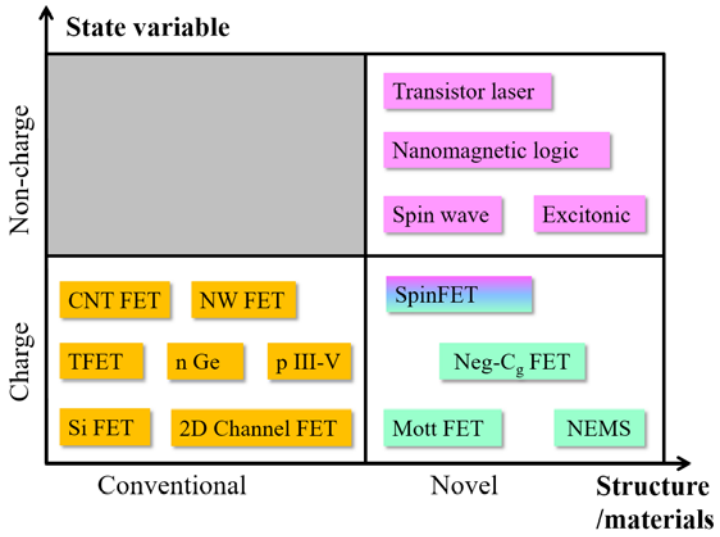


Figure BC3.1 Taxonomy of Options for Emerging Logic Devices

Note: The devices examined in this chapter are differentiated according to 1) whether the structure and/or materials are conventional or novel, and 2) whether the information carrier is electron charge or some non-charge entity. Since a conventional FET structure and material imply a charge-based device, this classification results in a three-part taxonomy.

The resulting taxonomy of emerging logic devices is conveyed in the three tables associated with this section. Table BC3.1a is titled "Extending MOSFETs to the End of the Roadmap" and tabulates characteristics of the devices in the lower-left quadrant of Figure BC3.1. These devices are reviewed below in Section 3.2. Table BC3.1b, titled "Charge-Based Beyond CMOS: Non-Conventional FETs and Other Charge-Based Information Carrier Devices," consists of those devices in the lower-right quadrant of the figure, which are reviewed in Section 3.3. Finally, Table BC3.1c details the "Alternative Information Processing Devices" that are listed in the upper-right quadrant of Figure BC3.1 and that are reviewed below in Section 3.4.

Table BC3.1a MOSFETS: Extending MOSFETs to End of Roadmap

Table BC3.1b Charge-based Beyond CMOS: Non-conventional FETs and Other Charge-based Information Carrier Devices

Table BC3.1c: Alternative Information Processing Devices

3.2. Devices for CMOS Extension

3.2.1. Carbon Nanotube FETs

For many researchers, the search for an ideal semiconductor to be used in FETs succeeded when single-walled carbon nanotubes (CNTs) were first shown to yield promising devices more than 15 years ago. Owing to their naturally ultrathin body (~1 nm diameter cylinders of hexagonally bonded carbon atoms), superb electron and hole transport properties, and reasonable energy

gap of ~0.6 – 0.8 eV, CNTs offer solutions in most of the areas that other semiconductors fundamentally fail when scaled to the sub-10 nm dimensional scale. CNT FETs operate as Schottky barrier transistors with nearly transparent barriers to carrier injection achieved for both n- and p-type transport. They are intrinsic semiconductors and cannot be doped in the traditional sense; hence, no inversion layers of charge form to allow current flow. Rather, the gate field lowers the energy barrier in the CNT channel to allow for carriers to be injected from the metal contacts. The most prominent advantages of CNT FETs over other options for aggressively scaled devices are the room temperature ballistic transport of charge carriers, the reasonable energy gap, the demonstrated potential to yield high performance at low operating voltage, and scalability to sub-10 nm dimensions with minimal short channel effects.

In the past several years, significant advances have been made in understanding and enhancing device performance in CNT FETs. These include 1) realizing end-bonded contacts having an effective contact length of 0 nm with reasonable performance,[269] 2) detailing the impact of contact scalability in CNT FETs,[270] 3) maintaining performance as the channel length is scaled down to 9 nm without observing short channel effects,[271] 4) fabricating complementary gate-all-around FETs,[272] 5) fabricating an FET with an intrinsic fT of 153 GHz,[273] 6) fabricating CMOS inverters and pass-transistor logic operating at 0.4 V with a non-doped CNT,[274] 7) fabricating a carbon nanotube computer composed of 178 FETs,[275] 8) progress towards reducing the variability in CNT FETs,[276] 9) understanding origins of hysteresis,[277] and (10) fabricating CNT FETs with ON-current of 0.5 mA/μm.[278]

In addition to improvements at the device level, continuous progress has been achieved toward overcoming the dominant material challenges,[279] including the need to achieve purified and sorted semiconducting CNTs with a relatively uniform diameter distribution and then position the CNTs into aligned, closely packed arrays with consistent pitch. With a target purity of 99.9999% semiconducting CNTs and placement density of >125 CNTs/μm (<8 nm pitch), much work still remains. However, it is important to note that progress continues to be steady and without fundamental obstacles barring these goals from being realized. There remains a need for further research toward improving other device-level aspects, including further reduction of contact effects at small contact lengths, demonstrated reduction in variability, improved control of gate dielectric interfaces and properties, and the experimental study of devices and circuits fabricated using the most scaled and relevant device structures and materials. In short, much work remains for CNT FETs, but they have some of the most substantial (and already demonstrated) potential in high-performance, low-voltage, sub-10 nm scaled transistor applications.

3.2.2. NANOWIRE FETS

Nanowire field-effect transistors are structures in which the conventional planar MOSFET channel is replaced with a semiconducting nanowire. Such nanowires have been demonstrated with diameters as small as 0.5 nm.[280] They may be composed of a wide variety of materials, including silicon, germanium, various III-V compound semiconductors (III-As, III-Sb, III-P, and III-N), II-VI materials (CdSe, ZnSe, CdS, ZnS), as well as semiconducting oxides (In_2O_3, ZnO, TiO_2), etc.[281] Importantly, at low diameters, these nanowires exhibit quantum confinement behavior, i.e., 1-D ballistic conduction,[282] and match well with the gate-all-around structure that permits the reduction of short channel effects and other limitations to the scaling of planar MOSFETs.

Important progress has been made in the fabrication of semiconducting nanowires for use as FET channels, for which there are two principal formation methods. The first method is top-down, by which semiconducting channels are formed through lithography and etch. The second approach is bottom-up growth including catalyzed vapor-liquid-solid (VLS) growth[283,284] and template-assisted selective epitaxy (TASE).[285] These mechanisms have been used to realize a variety of nanowire geometries, including core-shell and core-multishell heterostructures.[286,287] Although the top–down methods have been prevailing in the industrial manufacturing, the bottom–up methods have been developed to a point that is worth serious consideration for practical use, given their advantage in heterogeneous integration and convenience for in situ passivation through heterostructures. Nanowire gate-all-around geometry is of interest primarily due to its superb gate electrostatics that can allow further gate-length scaling.

Vertical nanowire transistors have been fabricated in this manner using Si,[288] InAs,[289,290] and ZnO.[291] Core-shell gate-all-around configurations display excellent gate control and few short channel effects. Circuit and system functionality of nanowire devices has been demonstrated, including vertical InAs MOSFETs with 103 GHz switching speed,[292] a down-conversion mixer based on vertical InAs transistors that showed cut-off frequency of 2 GHz,[293] and extended, programmable arrays (“tiles”) of non-volatile nanowire-based Flash memory that are used to build circuits such as full-adder, full-subtractor, multiplexer, demultiplexer, clocked D-latch and finite state machines.[294,295] Planar VLS III-As nanowires perfectly aligned in-plane have enabled multigate HEMTs to enhance high frequency performance.[296,297]

Despite the promising results that are mostly obtained from academic research labs, bottom-up nanowire transistors still face significant challenges before commercialization is feasible. There is an urgent need to improve device yield and uniformity, as well as position registry if the nanowires are to be transferred to a different substrate.[298] On the other hand, the potential of bottom-up nanowire transistors for monolithic core-shell architecture and the inherently relaxed lattice matching requirements for heterogeneous integration have not been completely exploited for low power and high speed applications.[299] For top-down

fabricated nanowires, with the demonstration of standalone transistors, CMOS integration, and a functional ring oscillator, vertically stacked planar Si nanowires hold enormous potential to succeed FinFETs in sub-5nm technology nodes.[300,301,302]

3.2.3. 2D MATERIAL CHANNEL FETS

Two-dimensional (2D) materials transition metal dichalcogenides (TMDCs), including graphene, are promising candidates for future channel materials in LSIs. Since they are layered materials, they can be as thin as one-layer (one-atom) thick without degrading their properties, which cannot be realized with conventional three-dimensional materials. Electrostatic control of such a thin channel is easier than a conventional bulk channel, suppressing "short channel effects" often encountered by scaled transistors. Carrier mobility of such 2D materials can be very high. Furthermore, novel devices based on principles different from that of CMOS can be realized using 2D materials, as discussed later.

Graphene has especially attracted attention as a channel material due to its extremely high mobility since the year of 2004, when a report on monolayer graphene prepared by exfoliation of graphite crystals was published.[303] The report showed that the field-effect mobility of graphene on SiO_2 was as high as ~10,000 cm^2/Vs. It was then predicted that the room-temperature mobility of graphene on SiO_2 would be limited to ~40,000 cm^2/Vs due to scattering by surface phonons of the SiO_2 substrate.[304] In fact, much higher field effect mobility was obtained using suspended graphene. Values as high as 120,000 cm^2/Vs and 1,000,000 cm^2/Vs at 240 K and liquid-helium temperature were obtained.[305,306] Recently, hexagonal boron nitride (hBN), an inert and flat material, has been used as a substrate for graphene-channel transistors, and it has been shown that the field effect mobility of such devices can exceed 100,000 cm^2/Vs at room temperature near the charge neutrality point.[307,308] Furthermore, a device in which graphene was sandwiched between two hBN flakes and edge-contacted with two metal electrodes exhibited mobility even higher than the above.[309] The results indicate that hBN can be excellent passivation film for graphene devices.

Graphene can also be obtained on SiC surface by annealing a SiC crystal at high temperatures (often called "epitaxial graphene"). The annealing temperatures range from 1200ºC to 2000ºC depending on the annealing environment.[310,311] Chemical vapor deposition of graphene on metal foil or film has also been demonstrated.[312,313,314,315] Typical growth temperatures are around 1000ºC. It has been shown that monolayer graphene is preferentially formed on Cu foil or film,[312,314,316] while multi-layer graphene can be formed on Ni, Co, and Fe catalyst.[313,315,317] The quality of epitaxial graphene and CVD graphene is now as good as that of exfoliated graphene.[318,319]

Efforts have been made to fabricate graphene-channel transistors, where fabrication processes such as doping and contacting to graphene channels have been developed.[320] However, since graphene does not have a bandgap, such transistors cannot have an ON/OFF ratio high enough for digital applications. Several approaches have been proposed to open a bandgap of graphene. One of the two major approaches is to apply an electric field perpendicular to AB-stacked bilayer graphene.[321,322,323,324,325] Experimentally, a transport gap of 130 meV was obtained at an electrical displacement of 2.2 V/nm, providing an ON/OFF ratio of ~100 at room temperature.[324] This ON/OFF ratio is probably the largest for this approach so far, which is, however, not high enough for logic applications. In fact, it has been pointed out that a small stacking fault of AB-stacked bilayer graphene can increase the off current,[326] which is a serious problem.

A promising approach to form a bandgap in graphene is to make it narrow, that is, to form a graphene nanoribbon (GNR).[327,328,329,330,331,332,333,334] In fact, simulations using a first-principles many-electron Green's function approach within the GW approximation have predicted that bandgaps can be as large as ~5 eV depending on their widths for armchair-edged GNRs (AGNRs).[334,335] Formation of GNRs was first attempted by using electron beam lithography and etching.[328] Carrier transport through such a GNR was also investigated. An energy gap of ~200 meV was obtained for a GNR with a width of 15 nm. Devices with multiple GNRs with a sub-10 nm half-pitch were fabricated using patterning with directed self-assembly of block copolymers.[336] The transport characteristics of such top-down GNRs were poor, however. This is mainly because the edges of such GNRs were not well controlled, probably with a lot of defects.[337,338] Recently, however, attempts to form GNRs with controlled edges have been made using bottom-up approaches. In fact, Cai et al. demonstrated the growth of armchair-edged GNRs (AGNRs) from 10,10'-dibromo-9,9'-bianthryl precursors.[339] In their approach, precursor molecules are deposited onto a clean Au(111) surface by vacuum evaporation in ultra-high vacuum. The substrate is then heated to 200ºC to remove Br from the precursors and to connect them with each other at the Br-removed points, forming polymers. By further heating the substrate to 400ºC, the polymers were cyclodehydrogenated to form AGNRs with a uniform width. The AGNR formed is referred to as 7AGNR, because it has seven dimer lines in the width direction. The band gap of 7AGNR is 3.7-3.8 eV according to the simulations above[334,335] and agrees with an experimentally obtained bandgap (~2.3 eV) considering image-charge corrections by Au substrate.[340] Now several types of GNRs have been formed using similar approaches with different precursors.[341] As for AGNRs with a smaller bandgap, 9AGRs with a theoretical bandgap of about 2.2-2.3 eV have been obtained.[305] Formation of 13AGNRs with a theoretical bandgap of about 2.3-2.5 eV was also demonstrated although the GNRs were rather short, typically less than 10 nm in this case. The successful formation of atomically precise AGNRs paves a way for their application to transistor channels.

Performance of GNR-channel transistors have been predicted by numerical simulations.[342,343,344] It was shown that a transistor with multiple-GNR channels (width: 1.47 nm, pitch: 3.47 nm) with a channel length of 15 nm exhibited an on-current exceeding 1 mA/μm with ON/OFF ratio larger than 10^5 and a subthreshold swing of 64 mV at a drain voltage of 0.1 V[40]. Transistors using 7AGNRs as channels were fabricated and evaluated experimentally. The performance of transistors was, however, poor with a very low on-current and an ON/OFF ratio of 3.6 x 10^3 at a drain voltage of 1V.[345] The small on-current was attributed to large Schottky barriers at the source and drain contacts caused by the large bandgap of 7AGNR. Use of 9AGNRs and 13AGNRs with smaller bandgaps actually improved the transistor performance. In fact, transistors using 9GNRs as channel exhibited ON/OFF ratios as high as 105 and on-current of 1 μA at a drain voltage of 1V, although the number of GNRs in each transistor is unclear.[346] The performance is not yet as good as a counterpart using carbon nanotubes (CNTs)[347] but expected to improve further by, for example, covering GNRs with hBN and realizing better contacts between GNRs and source/drain electrodes.

New principle devices using GNRs have also been proposed. One is a tunneling field-effect transistor (TFET). A higher on-current than that of Si TFET has been predicted.[348] Use of strained graphene as a channel can also realize tunneling-like transport, according to simulations.[349] A Klein-tunneling-based device has also been proposed.[350] Graphene can offer possibilities for employing novel switching mechanism for future electronics.

Transition metal dichalcogenides (TMDCs) are another 2D material attracting attention. TMDCs have the chemical formula of MX_2, where M is a transition metal element and X is a chalcogen. They can be metallic, half-metallic, semiconducting, or superconducting depending on their compositions. Molybdenum disulfide, MoS_2, is probably the most popular semiconducting TMDC, whose single layer was isolated for electrical measurements in 2005.[351] Electrical properties of semiconducting TMDCs depend on the number of layers due to quantum confinement effects and changes in symmetry. For example, single-layer MoS_2 has a direct band gap of 1.9 eV, while bulk MoS_2 has an indirect bandgap of 1.2 eV.[352] The bandgaps also vary with the compositions. For example, first principles calculations performed using the Heyd-Scuseria-Ernzerhof (HSE06) hybrid functional show that MoS_2, $MoSe_2$, $MoTe_2$, WS_2, WSe_2, and WTe_2 have bandgaps of 2.02 eV, 1,72 eV, 1.28 eV, 1.98 eV, 1.63 eV, and 1.03 eV, respectively.[353]

Transistors with TMDCs as a channel material have been demonstrated. Kis et al. fabricated a top-gate MoS_2-channel transistor, demonstrating a large ON/OFF ratio (~10^8) and good subthreshold swing (74 mV/decade).[354] Exfoliated single-layer MoS_2 was used in this experiment. However, field-effect mobility was relatively low (60-70 cm2/Vs).[355] In fact, transport in single-layer TMDC is severely affected by the environment, often degrading its electrical property. It has actually been demonstrated that mobility of TMDC increases with thickness.[356,357] This is because influences of charged impurities in substrate decrease as the thickness increases. As for MoS_2, field-effect mobility as high as 480 cm^2/Vs was obtained for a 47-nm thick MoS_2 channel.[358] MoS_2 is naturally electron-doped, which is possibly caused by chalcogen vacancies, while WSe2 is hole-doped.[359] It is actually still difficult to control doping level of TMDCs, which is a major challenge to realize TMDC-based electronics. Incidentally, Desai et al. fabricated MoS_2-channel transistor with 1-nm gate lengths by using a CNT as a gate.[360] The ON/OFF ratio and subthreshold swing were ~10^6 and 65 mV/decade, respectively. This is probably the shortest channel transistor ever made.

New principles devices using TMDCs have also been demonstrated. Sarkar et al. fabricated a tunneling FET (TFET) by placing n-type MoS_2 on top of p-type Ge, forming a p-n junction.[361] The TFET was gated by using a solid polymer electrolyte. The subthreshold swing had an average of 31.1mV/decade for four decades of drain current at room temperature. Britnell et al. prepared stacking structures consisting of graphene/MoS_2/graphene and graphene/hBN/graphene, demonstrating a switching device based on tunneling phenomena.[362] Although the tunneling devices introduced here can offer steep-slope switching properties, on-current is relatively low, which is an important issue to address for real-world applications. Fabrication of a lateral heterojunction of TMDCs, such as $MoSe_2$ and WSe_2, have also been demonstrated,[363,364] and a p-n junction by such a heterojunction has been made.[365,366] Valleytronics based on carriers located in two inequivalent valleys in the wave number space also attract attention.[367,368] New principles devices using TMDCs, as introduced here, may have good opportunities in future electronics.

Growth technology of TMDCs is also in progress. In fact, the synthesis of TMDC film dates back to the 1980's, when the growth was performed with van der Waals epitaxy.[369] More recently, Lee et al. demonstrated CVD growth of MoS_2 using MoO_3 and S powder as precursors.[370,371] The growth temperature was 650˚C. Single-crystal monolayer MoS_2 flakes were successfully obtained. This method was further improved and single-crystal MoS_2 flakes as large as 120 μm in lateral size were obtained.[372] There have been a quite a few reports using similar methods for synthesizing TMDCs, including $MoSe_2$,[373] WS_2,[370,374] and WSe_2.[375] However, uniform growth over a large area is not easy using this powder-based CVD technique. In 2015, Kang et al. succeeded in large area growth of MoS_2 by MOCVD using $Mo(CO)_6$ and $(C_2H_5)_2S$ as precursors.[376] The electron mobility of MoS_2 in this case was 30 cm^2/Vs at room temperature. In general, mobility of CVD MoS_2 is lower than that of exfoliated MoS_2, which is still an important issue to address. Furthermore, MoS_2 deposition by using sputtering is also in progress.[377,378,379] The sputtering method is scalable, but it is still difficult to obtain film with a quality as high as that by MOCVD.

3.2.4. P-TYPE III-V CHANNEL REPLACEMENT DEVICES

III-V compound semiconductors as replacements for n-type channel materials have attracted considerable attention because of their excellent bulk electron mobilities.[380] To create high performance CMOS circuits, high mobility p-channel materials are also required. Among III-V compound semiconductors, Sb-based semiconductors exhibit high hole mobilities when used as bulk materials; for example, InSb and GaSb show mobilities of 850 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 800 $cm^2 \cdot V^{-1} \cdot s^{-1}$, respectively,[381] which are significantly greater than the bulk Si hole mobility of 500 $cm^2 \cdot V^{-1} \cdot s^{-1}$. Moreover, hole mobility can be further increased by introducing biaxial compressive strain. This can be accomplished using pseudomorphic growth on a material with a smaller lattice constant.[381, 382, 383, 384] Another method of improving hole mobility is the application of uniaxial strain[383, 385,] which can be used in a similar manner as used in Si MOSFETs. The piezoresistance coefficient of p-InGaSb is 1.5 times greater than that of Si when uniaxial strain is applied.[386] Another advantage of InGaSb is its superior characteristics when used as an n-channel material. InGaSb has an electron mobility of over 4000 $cm^2 \cdot V^{-1} \cdot s^{-1}$. Thus, CMOS circuits can be fabricated using a single channel material system.[387]

The highest hole mobilities when using compressive strain were found in GaSb/AlAsSb heterostructures; they exhibit a mobility[384] of 1500 $cm^2 \cdot V^{-1} \cdot s^{-1}$. In the case of an InGaSb/AlGaSb system, 1500 $cm^2 \cdot V^{-1} \cdot s^{-1}$ was also observed[382]. In InSb, the highest mobility[386] is 1230 $cm^2 \cdot V^{-1} \cdot s^{-1}$. However, the thickness of the quantum well was 5 nm; a wider well might provide higher mobility.[384] Regarding device performance, compressively strained InSb quantum well pFETs with a gate length of 40 nm have an f_T value of 140 GHz, a g_m of 510 mS/mm, and an I_{on} of 150 mA/mm at a power supply voltage of 0.5 V. When the gate length was 125 nm, the sub-threshold slope[386] was 90 mV/dec.

A device on a Si substrate is essential as a replacement material for Si channels in MOSFETs. To realize III-V p-FETs on a Si substrate, some methods are reported. The first method is transfer of nano-ribbon,[388], nanowire[389] or film.[390] In the case of nano-ribbon, the peak effective mobility of the device is 820 $cm^2 \cdot V^{-1} \cdot s^{-1}$, achieved using an InAs cladding layer for surface passivation and hole confinement. By employing high-κ materials (10-nm-thick ZrO_2), the obtained sub-threshold slope was 130 mV/dec, even at an interface surface density of 1.4×10^{13} $cm^{-2} \cdot eV^{-1}$. In combination with an InAs channel using the same technique, CMOS gates were fabricated and the logic operations of NOT and NAND were demonstrated.[391] In the case of this trial, the peak mobility was reduced to 370 $cm^2 \cdot V^{-1} \cdot s^{-1}$ because of the thin well (5 nm) in the enhancement mode. The obtained sub-threshold slope was 156 mV/dec. In the case of nanowire, the inverter circuit was fabricated from single nanowire with InAs and GaSb.[389] As another possibility of InAs/GaSb nanowire, it can apply tunnel FET.[392] Rapid melt growth (RMG) method[393] can also supply GaSb thin film on Si, and transistor operation by RMG was reported.[394]

To realize a p-FET using an Sb-based channel, one notable problem is the interface property of metal-insulator-semiconductor structures. At present, the best I-V properties have been reported for compressively strained InSb quantum well p-FETs (with a gate length of 40 nm) using an HEMT structure to create a Schottky gate;[386] a MOS structure is a preferred choice to achieve low gate leakage currents. In MOSFETs, the lowest sub-threshold slope is limited to 120 mV/dec when the gate length is 5 mm.[395] Although the interface state density is approximately 3×10^{11} $cm^{-2} \cdot eV^{-1}$ in the mid-bandgap region, it rises to 1×10^{13} $cm^{-2} \cdot eV^{-1}$ near the conduction band edge. Moreover, the insulator thickness (Al_2O_3) in this trial was limited to 10 nm. Thus, improvements to the method of obtaining a low interface state density using a thinner insulator are required because the interface state density strongly depends on the fabrication process.[396] The requirement of having a high on-current is another problem. For a 5-mm-long MOSFET, an on-current of 70 mA/mm was reported;[395] however, shorter gate lengths were not studied in this report. The shortest reported gate length in a p-MOSFET is 750 nm,[396] and the channel dependence shows an inverse relationship between the gate length and the on-current. In the 750 nm-long device, the highest on-current was 70 mA/mm. Moreover, the estimated on-current in the InGaSb HEMT structure was 200 mA/mm, even when the gate length was 20 nm.[397] Taking both the significant degradation of mobility at a high sheet carrier concentration and carrier starvation due to insufficient carrier concentration due to poor ion implantation in a III-V semiconductor into account, the feasibility of high on currents must be verified.

3.2.5. N-TYPE GE CHANNEL REPLACEMENT DEVICES

High electron mobility in bulk Ge and (111)-inversion layer, which are 2.4 times and 3.1 times the counterpart of Si, respectively,[398] is considered a fundamental advantage of Ge-nMOSFETs. In addition, comparable or even higher ballistic current has been estimated for (111)Ge-nMOSFETs than for GaAs, InAs and InSb nMOSFETs due to the higher density of states,[399] although the electron mobility of Ge is less than those of III-V compound semiconductors. Not only the performance but also the lower cost of forming CMOS circuits may be another advantage of introducing Ge-nMOSFETs than forming III-V nFET/Ge pFET dual-channel CMOS configuration. Sub-100-nm FinFET-type Ge-nMOSFETs have already been demonstrated[400,401] for the counterpart of Ge-pMOSFETs in 7-nm technology node and beyond. Strain technologies to enhance the electron mobility using source-drain stressors[402] and stress liners[403] have been demonstrated and simulated, respectively. Simple CMOS circuits such as invertors and ring oscillators composed of Ge p- and nMOSFETs have been demonstrated on Ge-on-insulator substrates[404] and on poly-Ge layers on SiO_2/Si substrates.[405] A circuit simulation based on TCAD results for p- and n-channel Ge-on-insulator (GOI) MOSFETs predicted that the GOI-CMOS outperforms Si-on-insulator CMOS in various elemental circuits and

conditions.[406] As a new material, GeSn semiconductor alloy, in which direct band gap was predicted for a Sn fraction over ~10%, has been examined for CMOS and Si-photonics devices.[407,408] Theoretical calculations for a lattice-relaxed GeSn-nMOSFET with a Sn fraction around 10% predicted slightly higher carrier injection velocity than in a Ge-nMOSFET thanks to the higher electron population to the G valley with a lower effective mass.

The best reported inversion electron mobility at a high inversion electron density (N_s) is 429 cm^2/Vs at $N_s=1\times10^{13}$ cm^{-2} or 488 cm^2/Vs at $N_s=8\times10^{12}$ cm^{-2}.[409,410] It is significant that these high-mobility values were observed for devices with low EOT values of around 1 nm in terms of implementing Ge-nMOSFETs in scaled CMOS-LSIs. The scaling of gate-length and EOT has been demonstrated independently down to 35 nm and 0.39 nm, respectively.[400,411] The sub-threshold swing and off-state leakage current of Ge-nMOSFETs are getting better but still slightly worse than those of Ge-pMOSFETs[412], suggesting that the interface state density near the conduction-band edge should be improved. The drain current for scaled Ge nMOSFETs has been greatly improved during the latest 2 years and has reached ~250 mA/mm for $L_g=40$ nm device at $V_{dd}=1V$.[400] However, the current drivability is still lower than that of state-of-the-art Si-nMOSFETs of the similar gate-lengths. Reducing the high parasitic resistance in the Ge-nMOSFETs is a key technology to obtain acceptable current drivability as a counterpart of high-performance Ge-pMOSFETs. One of the major problems is the low activation of n-type dopants in Ge, which is usually saturated up to around 1×10^{19} cm^{-3} by means of conventional ion-implantation and RTA techniques. Theoretical calculation predicted the specific contact resistivity required in the ITRS ($<1\times10^{-8}$ ohm.cm^2) can be satisfied for a metal/0.7-nm-ZnO/n^+-Ge contact if an electron density of over 1×10^{20} cm^{-3} is attained in the Ge layer.[411] Experimentally, enhancing the activation of n-type dopants up to over 2×10^{20} cm^{-3} by Sb ion implantation and laser annealing processes has been achieved.[413] Reduction in a specific contact resistivity (r_c) down to ~3×10^{-8} ohm.cm^2 for NiGe/n^+-Ge contact has been also reported by the 2-step ion-implantation technique.[414]

The most significant issue for the implementation of Ge-nMOSFETs in future high-performance CMOS technologies is the demonstration of competing short-channel performances with conventional Si-nMOSFETs. Integration of the contact formation processes to reduce parasitic resistance with the gate-stack formation processes to realize sub-nm-EOT with low interface state density is a key technology. These should be consistent with integration processes for technology generations of 7-nm node and beyond. A common gate stack process for p- and n-MOSFETs is also desirable in terms of the cost merit against III-V/Ge dual channel devices.

3.2.6. TUNNEL FETS

Tunneling Field Effect Transistors (TFETs) have the potential to achieve a low operating voltage by overcoming the thermally limited subthreshold swing voltage of 60 mV/decade by utilizing tunneling as a switching mechanism.[415,416,417] In its simplest form, a TFET is a gated, reverse-biased p-i-n diode with a gate controlled intrinsic channel. There are two mechanisms that can be used to achieve a low voltage turn on. The gate voltage can be used to modulate the thickness of the tunneling barrier at the source channel junction and thus modulate the tunneling probability.[418,419,420,421] The thickness of the tunneling barrier is controlled by changing the electric field in the tunneling junction. Alternatively, it is possible use energy filtering or density of states switching. If the conduction and valence band do not overlap at the tunneling junction, no current can flow. Once they do overlap, current can flow. Simulations have predicted arbitrarily steep subthreshold swings when relying on density of states switching as the current is abruptly cutoff when the conduction band and valence band no longer overlap.[417] If phonons or short channel lengths are accounted for, simulated subthreshold swings on the order of 20–30 mV/decade are typical.[422] It is possible to use the tunneling switching mechanisms in series with the standard MOSFET thermal switching mechanism to get an overall subthreshold swing that is steeper than 60 mV/decade when no individual mechanism is steeper than 60 mV/decade.[423] The best experimental results to date have relied on a combination of thermal switching and density of states switching.[424].So far, the experimental results are far worse than simulated device characteristics. The review by Lu and Seabaugh[415] shows a comprehensive benchmarking of published experimental results prior to 2014. The benchmarking shows two problems with TFETs as a MOSFET replacement: 1) Devices are unable to achieve SS <60 mV/decade over a large range or at useful current levels and 2) The on-state current is too low for reasonable performance.

The review shows 14 reports of subthreshold swings below 60 mV/decade, and a few additional results have been published since. Most of the results are for group-IV materials such as Si,[420,425,426,427,428,429] strained SiGe,[430] Si/Ge,[431] and strained Ge.[432] Nanowire III-V TFETs have shown even steeper swings. A InP/GaAs heterojunction[433] has shown 30 mV/decade at 1 pA/μm. The steepest result ever reported is in a Si/InAs heterojunction[434] of approximately 20 mV/decade at 0.1 pA/μm. However, there are only a few data points defining this result. Even for low power applications, at least 1–10 μA/μm is needed.[435] Recently, a promising InAs/GaAsSb/GaSb nanowire heterostructure TFET with a 48 mV/decade SS at 67 nA/μm and an I_{60} (current at 60 mV/decade) of 0.31 μA/μm was demonstrated.[424].

Researchers attempting to achieve higher on-current TFETs have traditionally relied on reducing the effective mass by using III-V's and reducing effective bandgap by using a heterostructure. While this has increased the current, the subthreshold swings and off currents have gotten worse. The increase in off-state current and subthreshold swing needs to be decoupled from the increase

in on-state current. Unfortunately, this is a fundamental tradeoff when modulating the thickness of the tunneling barrier:[416] barrier thickness modulation only gives a step subthreshold swing at low current densities.

An ideal density of states (DOS) switch would switch abruptly from zero-conductance to the desired on-conductance thus displaying zero subthreshold swing voltage.[436] Practically, the band edges are not perfectly sharp, so there is a finite density of states extending into the band gap. Optical measurements of intrinsic GaAs imply a band edge steepness of 17 meV/decade.[437] However, the electrically measured joint DOS in diodes has generally indicated a steepness >90 mV/decade.[438] This broadening is likely due to the spatial inhomogeneity and on heavy doping that appears in real devices. Effectively, there are many distinct channel thresholds in a macroscopic device, leading to threshold broadening. Fortunately, it's been experimentally demonstrated that a band edge worse than 60 mV/decade can be combined with a thermal switching mechanism to give an overall subthreshold swing better than 60 mV/decade.[423]

TFETs are reverse-biased diodes hence are subject to generation in the depletion region. These generation events include but are not limited to bulk and interface trap-assisted Shockley-Read-Hall (SRH)[439,440,441] and spontaneous and Auger generation.[442] Calculations based upon these mechanisms show that these significantly degrade the subthreshold swing and increase the leakage currents but do not prevent TFETs from achieving sub-60 mV/decade subthreshold swing. Material defects and gate interface traps make these effects worse and result in worse band edges.

To overcome these challenges, better material perfection than ever before is needed. Every defect or dangling bond can create a trap that ruins the band edge or creates a parallel conduction path. The defects due to doping can be eliminated by electrostatically inducing carriers. Proof of concept devices can be made by making the device a few nanometers large so that there is a low probability of having a trap within the device. 2D transition metal dichalcogenides (TMD) heterostructures potentially have better electrostatic control and lower defects as there are ideally no dangling bonds at the semiconductor oxide interface.

3.3. Beyond-CMOS devices: Charge-Based

3.3.1. Spin FET and Spin MOSFET Transistors

Spin-transistors are classified as "non-conventional charge-based extended CMOS devices,"[443] and can be further divided into two categories: the spin-FETs proposed by Datta and Das[444] and spin-MOSFETs proposed by Sugahara and Tanaka.[445] The structures of both types of spin transistors consist of a ferromagnetic source and a ferromagnetic drain which act as a spin injector and a detector, respectively. Although the devices have similar structures, they have quite different operating principles.[443,446] In spin-MOSFETs, the gate has the same current switching function as in ordinary transistors, whereas in the spin-FETs, the gate acts to control the spin direction by utilizing the Rashba spin-orbit interaction. Both types of devices behave as a transistor and function as a magnetoresistive device. The important features of spin transistors are that they allow a variable current to be controlled by the magnetization configuration of the ferromagnetic electrodes (spin-MOSFETs) or the spin direction of the carriers (spin-FETs), and they offer the capability for non-volatile information storage using the magnetization configurations. These features are very useful for energy-efficient, low-power circuit architectures that cannot be achieved by ordinary CMOS circuits. Non-volatile logic and reconfigurable logic circuits have been proposed using the spin-MOSFET and the pseudo-spin-MOSFETs, which are suitable for power-gating systems with low static energy.[446,447,448,449,450,451,452]

The read and write operations of spin-FETs[446,453] and spin-MOSFETs[446,454,455,456,457] have not yet been fully experimentally verified. However, there has been important progress in the underlying technologies. Spin injection, detection and manipulation are essential [455] for realizing fully functional spin transistors. One key development has been half-metallic ferromagnetic materials for highly efficient spin injector/detectors. Theories[458,459,460,461] also predict that the insertion of a tunnel barrier between the ferromagnet (FM) and semiconductor (SC) in order to optimize the interface resistance between FM, and SC is a promising method for producing highly efficient spin injection and detection.

Spin injection and detection in Si have been achieved using hot-electron transport[462] and spin-polarized tunneling.[463,464,465,466,467,468,469,470] The electrical creation and detection of spin accumulation in n-type and p-type Si were demonstrated using FM/tunnel contacts[463,464,466,467,468,469,470] and FM/Schottky-tunnel-barrier contacts[471] up to room temperature (RT). Electrical spin injection into Si channels has also been demonstrated up to 500 K[465] by using a spin relaxation measurement method (Hanle measurement). A relatively long spin lifetime has been observed in heavily doped Si at RT.[464,467,468,470] Spin transport in SC has been studied intensively in various kinds of tunnel and channel materials. Observation of spin signals in heavily doped Ge[472,473,474] and GaAs[475,476] at RT has also been reported. Another study[477, 478] reported low-resistance spin injection and detection into Si using graphene and boron nitride tunnel barriers. Local magnetoresistance signal up to RT have been observed in long channel devices with FM/MgO tunnel barrier/Si lateral spin valve structures.[479,480] Recently, a basic read operation was demonstrated[457] at room temperature by using spin-MOSFETs with a back-gated structure and an interface technology in which the local magnetoresistance signal is observed at RT.

Since the reported[457] difference in the drain current between parallel and antiparallel spin configurations is very small at room temperature, the development of half-metallic ferromagnetic materials on SC is expected to be very important. Half-metallic Heusler alloys[481,482,483,484,485] are one of the most promising half-metallic ferromagnetic materials, because they are relatively easy to prepare. In addition to the progresses shown in the 2013 edition of the ITRS and references, spin injection and detection has been reported that is more efficient in SCs using a Heusler compound than in the ordinal CoFe electrodes.[486,487,488,489] More efforts to improve the qualities of Heusler compounds and FM/SC interfaces are required in order to observe large differences in drain current between parallel and antiparallel spin configurations. It should be noted that half-metallic materials are a required technique for spin-FETs because the current switching function needs to be controlled by spin precession induced by the action of the gate voltage. In spin-MOSFETs, however, since the relative magnetization configurations of the source and drain are used to modify the output current, half-metallic materials might not be required for spin-MOSFET.

Alternative approaches for realizing spin-MOSFETs have been proposed.[446,451,454,490, 491] Pseudo-spin-MOSFETs are circuits that reproduce the functions of spin-MOSFETs using an ordinary MOSFET and a magnetic tunnel junction (*MTJ*) which is connected to the MOSFET in a negative feedback configuration. Although pseudo-spin-MOSFETs offer the same functionality as spin transistors, such as the ability to drive variable current, pseudo-spin-MOSFETs have larger resistance than spin-FETs or spin-MOSFETs.

In terms of spin manipulation, spin precession of polarized carriers in the channel controlled by a gate voltage has been observed experimentally at low temperature.[492] This result confirms that spin-orbit interaction can be controlled by gate voltage. Materials with a strong spin-orbit interaction, such as InGaAs, InAs and InSb, are required[446] in order for the channel to sufficiently induce the Rashba spin-orbit interaction. However, materials with a strong spin-orbit interaction decrease spin lifetime. The use of a narrow wire channel structure[493,494,495] and the so-called persistent spin helix condition[496,497,498,499,500] has been proposed in order to increase spin lifetime. The experimental proof of spin injection, detection and manipulation at RT is needed in order to create spin-FETs with a channel material having strong spin-orbit interaction. Spin-MOSFET[454,455] and the pseudo-spin-MOSFET[446,450,491] use spin-transfer-torque (*STT*) switching, similar to the *STT*-MRAM that was commercialized at the end of 2012.[501]

To date, long channel devices with center-to-center spacing between the FM source/drain electrodes larger than $l_{FM\text{-}FM}$ >1000 nm have been investigated. To realize full read and write operations in spin-MOSFETs and spin-FETs at RT, experimental studies using short channel devices with $l_{FM\text{-}FMl}$ <100 nm are needed.

3.3.2. NEGATIVE GATE CAPACITANCE FET

Salahuddin and Datta originally proposed[502] that, based upon the energy landscape of ferroelectric capacitors, it should be possible to implement a step-up voltage transformer that will amplify the gate voltage of a MOSFET. This would be accomplished by replacing the standard insulator in the gate stack with a ferroelectric insulator of appropriate thickness. The resulting device is called a negative gate capacitance FET or NCFET. The gate operation in this device would lead to subthreshold swing (STS) lower than 60 mV/decade and might enable low voltage/low power operation. The main advantage of such a device[503] is that it is a relatively straightforward replacement of conventional FETs. Thus, high I_{on} levels similar to advanced CMOS would be achievable with lower voltages. An early experimental attempt to demonstrate a low-STS NCFET, based on a P(VDF-TrFE)/SiO_2 organic ferroelectric gate stack, was reported[504] in 2008, and subsequently[505] in a more controlled structure in 2010. These experiments established the proof of concept of sub-60 mV/decade operation using the principle of negative capacitance.

In addition to these experiments using polymer-based ferroelectrics, negative differential capacitance was demonstrated in a crystalline capacitor stack.[506] Essentially, it was demonstrated that in a bi-layer of dielectric Strontium Titanate ($SrTiO_3$: STO) and Lead Zirconate Titanate ($Pb_xZr_{1-x}TiO_3$: PZT), the total capacitance is larger than what it would be for just the STO of the same thickness as used in the bi-layer. This necessarily demonstrates the stabilization of PZT at a state of negative differential capacitance. More recently, in a single PZT capacitor, a direct measurement of negative capacitance was demonstrated.[507] That work determined that when a ferroelectric capacitor is pulsed with an input voltage, it shows an 'inductance-like' discharging in addition to a capacitive charging.

As a recent significant result, it is now possible to grow ferroelectric materials using the atomic layer deposition process (ALD) by doping the frequently used gate dielectric HfO_2 by constituents such as Zr, Al or Si.[508] Using this doped Hf based ALD ferroelectric, a number of experiments have demonstrated the negative capacitance effect.[509,510,511] For example, by using $HfZrO_2$ as a gate dielectric, sub-60 mV/decade STS was demonstrated[511] in finFETs with L_g=30 nm for both nFET and pFET structures. In the last two years, multiple papers have reported this effect for various material systems and channel lengths. Significant among them is the demonstration by GlobalFoundries of NCFETs in their 14 nm finFET technology, with improved subthreshold swing, lower OFF current and lower active power and ring oscillators running at GHz speed.[512]

3.3.3. NEMS SWITCH

Nano-Electro-Mechanical (NEM) switches are devices that employ electrostatic force to actuate a movable structure to make or break physical contact between two conductive electrodes. Mechanical switches feature two fundamental properties which are unattainable in MOSFETs: *zero off-state leakage* and *zero subthreshold swing*.[513] The first property provides for zero standby power dissipation, while the second property suggests the potential to operate at very low voltages for low dynamic power dissipation as well. Another advantage is that a mechanical switch can be operated with either positive or negative voltage polarity due to the ambipolar nature of the electrostatic force, so that an electrostatically actuated relay can be configured as a pull-down or pull-up device, respectively.[514] Additional advantages of mechanical devices include robust operation across a wide temperature range,[515] immunity to ionizing radiation, and compatibility with inexpensive substrates such as glass or even plastic. Since NEM switches comprise only conductive electrodes and air gaps, they can be fabricated at relatively low process temperatures in a modular fashion over CMOS circuitry. Indeed, since the most advanced CMOS technology in production today incorporates air-gapped interconnects,[516] it is conceivable for NEM switches to be implemented using multiple interconnect layers in an advanced back-end-of-line (BEOL) process.[517] Potential applications for mechanical switches in a hybrid NEMS-CMOS technology include CMOS power gating,[518] configuration of CMOS FPGAs,[519] non-volatile storage of information in SRAM and CAM cells,517 and energy-efficient, fast and reconfigurable look-up tables.[520]

NEM switches can be fabricated using conventional planar processing techniques (thin-film deposition, lithography and etch steps), with a final release step in which a sacrificial material such as silicon dioxide, photoresist, polyimide or silicon is selectively removed to form the actuation and contact air-gaps. (The gap in the contact region(s) can be made smaller than the actuation gap to reduce the switching delay and energy as well as the contact velocity for reduced wear and contact bounce.) The smallest actuation and contact gap demonstrated to date for a functional NEM structure fabricated using a top-down approach is 4 nm.[521] This device is a vertically actuated switch featuring a 30 nm-thick, 300 nm-wide, 1.4 μm-long doubly clamped TiW beam with a pull-in voltage of approximately 0.4 V. As expected, the off-state current is immeasurably low and the sub-threshold swing is practically zero. However, it is a 2-terminal device, not suitable for logic switch application.

In a digital logic circuit, it is necessary to connect multiple switches in series to implement various logic functions. To avoid having the state of a switch depend undesirably on the state of other switches in the series stack, a reference electrode is needed, such that the voltage applied between the control ("gate") electrode and the reference ("body") electrode determines the state of the switch, *i.e.* whether current can flow between the output ("source" and "drain") electrodes.[522] By biasing the reference electrode, the operating voltage of a relay can be minimized. Similarly, as for MOSFETs, a constant-field scaling methodology can be applied to scale NEM switches for improved device density, switching delay and switching energy.[523] The ultimate device density achievable may be comparable to that for MOSFETs, in principle. However, the switching delay of a mechanical logic switch (relay) is much longer than that of a MOSFET because it is dominated by the mechanical (motional) delay, ~1 ns,[513] rather than the electrical (charging/discharging) delay. Because of the large ratio between the mechanical and electrical delays of a relay, an optimized IC design should arrange for all mechanical movement to happen simultaneously, *i.e.* relay-based digital logic circuits should be comprised of single-stage complex gates so that the delay per operation is essentially one mechanical delay.[514] This generally results in significantly lower device counts as compared to the optimal CMOS implementations, especially since a relay can pass both low and high logic levels, and the body electrode can also be connected to a logic signal. By incorporating multiple pairs of source and drain electrodes into each gated structure[524] and/or by partitioning the gate electrode into multiple input electrodes,[525] the device count and hence the area required can be further reduced. A variety of relay-based computational and memory building blocks have been experimentally demonstrated to date.[526,527]

Since an optimized relay-based logic circuit has a topology that is very different from that of an optimized CMOS logic circuit, an assessment of the prospective benefits of NEM switch technology must be made at the level of complete circuit blocks. Such circuit-level assessments (*e.g.* of full adder and multiplier circuits) indicate that relays can provide for more than 10x reduction in energy per operation as compared with MOSFETs, and can reach clock speeds in the GHz regime.[528] Thus, a major potential advantage of NEM switch technology is *improved energy efficiency*. Moreover, by engineering the contact adhesive force and structural stiffness, bi-stable operation can be achieved, making scaled mechanical switches attractive for embedded non-volatile memory applications.[529]

Reliable operation is necessary for practical application of M/NEM switches in electronic circuits. Due to their extremely small mass (less than 1 ng), mechanical vibration/shock is not an issue. Structural fatigue is easily avoided by designing the movable electrode such that the maximum induced strain is well below the yield strength. Mechanical wear and Joule heating at the contacting points lead to increased real contact area and eventually stiction-induced device failure. This issue can be mitigated by using a refractory material to minimize wear and material transfer and by reducing the device operating voltage. (It should be noted that the higher associated contact resistance would not significantly compromise performance since the speed of an optimally designed relay-based logic circuit is limited by the mechanical delay rather than the electrical delay. The on-state resistance of a logic relay can be as high as ~10 kΩ.[514]) NEM switches with tungsten contacts have been demonstrated to have endurance up to 1 billion on/off cycles at 2.5 Volts for a relatively large load capacitance of 300 pF (*i.e.* exaggerated electrical

delay).[530] Endurance exceeding 10^{16} on/off cycles is projected for an operating voltage below 1 Volt and load capacitance below 1 pF. A gradual increase in contact resistance caused by surface oxidation or the formation of friction polymers during the course of device operation can lead to circuit failure and is the primary reliability challenge for M/NEM logic switches today. Stable conductive oxide contact materials and/or hermetic packaging are potential solutions to this issue.

Contact adhesive force sets the minimum spring restoring force of the movable electrode (to ensure that the switch turns off), which in turn sets a lower limit on the electrostatic actuation force (to ensure that the switch turns on) and hence the switching energy. For ultimately scaled contacts, the surface adhesion energy will be set either by metallic bonding or by van der Waals force (for oxidized contacting surfaces). The minimum switching energy for a nanoscale relay is anticipated to be on the order of 10 aJ, which compares well against the switching energy for an ultimately scaled MOSFET.[531,532]

In conclusion, NEM switches are intriguing candidates for ultra-low-power applications because they have negligible off-state leakage currents and abrupt switching behavior which, in principle, enables a very low operating voltage. Practical challenges remain to be solved, to achieve stable on-state resistance ((R_{ON}) and to minimize contact adhesive force within R_{ON} limits. A circuit-level assessment of energy *vs.* delay performance indicates that nanoscale relays should provide for more than 10× improvement in energy efficiency as compared with CMOS transistors, for applications requiring clock speeds below 100 MHz. Thus, they are poised to lead a resurgence in mechanical computing for the Internet of Things.

3.3.4. MOTT FET

Mott field-effect transistor (Mott FET) utilizes a phase change in a correlated electron system induced by a gate as the fundamental switching paradigm.[533,534] Mott FETs could have a similar structure as conventional semiconductor FET, with the semiconductor channel materials being replaced by correlated electron materials. Correlated electron materials can undergo Mott insulator-to-metal phase transitions under an applied electric field due to electrostatically doped carriers.[535,536] Besides electric field excitation, the Mott phase transition can also be triggered by photo- and thermal-excitations for optical and thermal switches. Defects created by environmental exposure to chemicals or electrochemical reactions can also induce Mott transition via carrier doping. The critical threshold for inducing phase change can be tuned via stress.

Mott FET structure has been explored with different oxide channel materials.[534] Among several correlated materials that could be explored as channel materials for Mott FET, vanadium dioxide (VO_2) has attracted much attention due the sharp metal-insulator transition near room temperature (nearly five orders in single crystals).[537] The phase transition time constant in VO_2 materials is in sub-picosecond range determined by optical pump-probe methods.[538] Device modeling indicates that the VO_2-channel-based Mott FET lower bound switching time is of the order of 0.5 ps at a power dissipation of 0.1 μW.[539] VO_2 Mott channels have been experimentally studied with thin film devices and the field effect has been demonstrated in preliminary device structures.[540, 541, 542] Recently, prototypes of VO_2 transistors using ionic liquid gating have shown larger ON/OFF ratio at room temperature than with solid gate dielectrics like hafnia.[543, 544] The conductance modulation happens at a slow speed, however, due to the large charging time constants.[545] The possibility of electrochemical reactions must also be carefully examined in these proof-of-principle devices due to the instability of the liquid-oxide interfaces and the ease of cations in such complex oxides to change valence state.[545, 546, 547] On the other hand, unlike traditional CMOS that is volatile and digital, electrochemically gated transistors exhibit non-volatile and analog behaviors, which can be utilized to demonstrate synaptic transistors[548] and circuits[549] that mimic neural activities in the animal brains. Voltage induced phase transitions in two-terminal Mott switches have also been implemented to realize neuron-like devices[550] and steep-slope transistors.[551] As a Mott device with purely electrostatic modulation in the solid-state base, the VO_2-FET with a high-k oxide/organic hybrid dielectric gate has been proposed.[552,553] Their reversible as well as quick resistance switching upon an application of gate bias and the maximum resistance modulation at the Metal-Insulator transition temperature indicate the possibility of purely electrostatic field-induced metal-insulator (Mott) transition.

Experimental challenges with correlated electron oxide Mott FETs include fundamental understanding of gate oxide-functional oxide interfaces and local band structure changes in the presence of electric fields. Methods to extract quantitative properties (such as defect density) of the interfaces are an important topic that have not been explored much to date. The relatively large intrinsic carrier density in many of the Mott insulators requires the growth of ultra-thin channel materials and smooth gate oxide-functional oxide interfaces for optimized device performance. It is also important to understand the origin of low room-temperature carrier mobility in these materials.[535] Theoretical studies on the channel/dielectric interfacial electronic band structure are needed for the modeling of subthreshold behaviors of Mott FETs. Understanding the electronic transition mechanisms while de-coupling from structural Peierls (lattice) distortions is also of interest and important in the context of energy dissipation for switching.

While the electric field-induced transitions are typically explored with Mott FET, nanoscale thermal switches with Mott materials could also be of substantial interest. Recent simulation studies of "ON and "OFF" times for nanoscale two-terminal VO_2 switches indicate the possibility of sub-ns switching speeds in ultra-thin device elements in the vicinity of room temperature.[554,555] Such devices could also be of interest to Mott memory.[556] One can, in a broader sense, visualize such correlated electron systems as

'threshold materials' wherein the conducting state can be rapidly switched by a slight external perturbation, and hence lead to applications in electron devices. Electronically driven transitions in perovksite-structured oxides such as rare-earth nickelates[557,558] or cobaltates[559] with minimal lattice distortions would also be relevant in this regard. Three-terminal devices are being investigated using these materials and will likely be an area of growth.[560,561,562, 563,564] $SmNiO_3$, with its metal-insulator transition temperature near 130ºC and nearly hysteresis-free transition, is particular interesting due to the possibility of direct integration onto CMOS platforms. Floating gate transistors have recently been demonstrated on silicon.[565] It has been found that non-thermal electron doping in $SmNiO_3$ can lead to a colossal increase in its resistivity, which has been utilized to demonstrate a solid-state proton-gated transistor with large ON/OFF ratio.[566] Clearly, these preliminary results suggest the promise of correlated oxide semiconductors for logic devices, while the doping process indicates slower dynamics than possible with purely electrostatic carrier density modulation. The non-volatile nature of the Mott transition in 3-terminal devices suggest combining memory operations into a single device and could be explored further. Architectural innovations that can create new computing modalities with slower switches but at lower power consumption can benefit in the near term with results to date while in the longer term transistor gate stacks need to be studied further for these classes of emerging semiconductors.

3.4. Beyond-CMOS devices: Alternative Information Processing

3.4.1. Spin Wave Device

A Spin Wave Device (SWD) is a type of magnetic logic device exploiting collective spin oscillation (spin waves) for information transmission and processing.[567,568,569,570] The basic elements of the SWD include: 1) magneto-electric cells (e.g. multiferroic elements) aimed to convert voltage pulses into the spin waves and vice versa;[571,572] 2) magnetic waveguides – spin wave buses for spin wave signal propagation between the magneto-electric cells,[573] 3) magnetic junctions to couple two or several waveguides, and 4) phase shifters to control the phase of the propagating spin waves. A SWD converts input voltage signals into the spin waves, computes with spin waves, and converts the output spin waves into the voltage signals. Computing with spin waves utilizes spin wave interference, which enables functional nanometer scale logic devices. Since the first proposal on spin wave logic,[567] the SWD concept has evolved in different ways encompassing volatile[574] and non-volatile,[575] Boolean[575,576] and non-Boolean,[577] single-frequency and multi-frequency circuits.[578] The primary expected advantage of SWD over Si CMOS are the following: 1) the ability to utilize phase in addition to amplitude for building logic devices with a fewer number of elements than required for transistor-based approach, 2) power consumption minimization by exploiting built-in non-volatile magnetic memory, and 3) parallel data processing on multiple frequencies in a single core structure by exploiting each frequency as a distinct information channel.

Micrometer scale SWD MAJ gate has been experimentally demonstrated.[579] It is based on $Ni_{81}Fe_{19}$ structure, operates within 1–3 GHz frequency range, and exhibits signal-to-noise ratio of approximately 10 at room temperature.[579] The internal delay of SWD is defined by the spin wave group velocity (e.g. 3×10^6 cm/s in $Ni_{81}Fe_{19}$ waveguides). Power dissipation in SWD is mainly defined by the efficiency of the spin wave excitation. Recent experiments with synthetic multiferroics comprising piezoelectric (lead magnesium niobate-lead titanate PMN-PT) and magnetostrictive (Ni) materials have demonstrated spin wave generation by relatively low electric field (e.g. 0.6 MV/m for PMN-PT/Ni).[580] The later translates in ultra-low power consumption (e.g. 1aJ per multiferroic switching). Recent experimental demonstration[572] of parametric spin wave excitation by voltage-controlled magnetic anisotropy (VCMA) is another promising route towards energy-efficient generation of spin waves.

Recently, a new type of SWD magnonic holographic memory (MHM), was proposed.[577] The principle of operation of MHM is similar to optical holographic memory, while spin waves are utilized instead of light waves. The first 2-bit MHM prototype based on yttrium iron garnet structure has been demonstrated.[581] MHM also possesses unique capabilities for pattern recognition by exploiting correlation between the phases of the input waves and the output interference pattern. Pattern recognition using MHM has been recently demonstrated.[582] The potential advantage of spin wave utilization includes the possibility of on-chip integration with the conventional electronic devices via multiferroic elements. In addition, magnonic holograms can show very high information density (about $1Tb/cm^2$) due to the nanometer scale wavelength of spin waves. According to estimates, the functional throughput of magnonic holographic devices may exceed 10^{18} $bits/s/cm^2$.[577]

There are several important milestones to be achieved for further SWD development: 1) nanomagnet switching by spin waves (e.g. by the combined effect of the voltage-assisted anisotropy change and a magnetic field produced by the incoming spin wave), and2) integration of several magneto-electric cells on a single spin wave bus. In order to have an advantage over CMOS in functional throughput, the operational wavelength of SWDs should be scaled down below 100 nm.[575] The success of the SWD will also depend on the ability to restore/amplify spin waves (e.g. by multiferroic elements or spin torque oscillators).

3.4.2. Nanomagnetic Logic

Nanomagnetic Logic (NML) uses fringing field interactions between magnetic islands to perform Boolean[583] and non-Boolean[584,585,586] logic operations. Binary information is represented via magnetization state. Most work with NML has focused on devices that couple in-plane (iNML). Recent work has also employed devices with out-of-plane, perpendicular magnetic

anisotropy (PMA). Perpendicular magnetic logic (pNML) devices typically switch through nucleation and domain wall propagation.[587,588] This reversal behavior is markedly different from in-plane permalloy nanomagnets, which remain nearly single-domain during switching and rotate coherently. That said, Bhowmick *et al.*[589] report using the spin Hall effect (SHE) to clock devices with PMA. With this approach, devices are placed in an in-plane, metastable state.

In all implementations of NML, externally supplied switching energy is generally needed to re-evaluate (i.e., "clock") a magnet ensemble with new inputs.[590] A clock modulates the energy barriers between magnetization states of the devices that comprise an NML circuit. With iNML, subgroups of devices are usually placed in a metastable state when clocked, and an input signal at one end can propagate through a part of said subgroup.[591] The other "end" of the subgroup is held in a metastable state to prevent back propagation of data. While pNML devices could be clocked in a similar manner (e.g., via the SHE[589]), it is also possible to globally clock a large ensemble of pNML devices (e.g., with an oscillating, out-of-plane magnetic field[586]). With either approach fine grain pipelining (and consequently improved throughput) could be achieved. (Subgroup size in iNML circuits will likely be limited by the granularity of the clock structure.)

Notably, either NML implementation can retain state without power and could be radiation hard. Moreover, it is possible that NML devices would dissipate less than 40 *kT* per switching event for a gate operation.[583] When clock overhead is considered, projections suggest that NML ensembles could still best low power CMOS equivalents in terms of metrics such as energy delay product, etc. Finally, NML appears to be scalable to ultimate limits using individual atomic spins.[592]

Present status for iNML: Fanout structures,[593] a 1-bit full adder,[594] etc. have been experimentally demonstrated and successfully re-evaluated with new inputs. Both field-coupled[595,596] and spin transfer torque (STT)[597,598,599] electrical inputs have been realized. For electrical output, multiple NML-magnetic tunnel junction hybrids[600] have been proposed and simulated. *Non-Boolean* hardware based on nanomagnetic discs has also been studied.[601] This work exploits the ability of nanomagnet systems to settle into energy minima to solve quadratic optimization problems (i.e., for computer vision applications).

Field based, CMOS compatible line clock structures have been used to simultaneously switch the states of multiple magnetic islands,[602] as well as to re-evaluate NML lines and gates with new inputs.[603] Additionally, recent experiments have considered materials-based solutions to further reduce field/energy requirements for line clock structures. Notably, results from Li *et al.*[604,605] suggest that component energy metrics could be further reduced by as much as 16X.

Voltage controlled clocking – e.g., multiferroics[606] and magnetostriction[607] – have also been proposed as potential clocking mechanisms for iNML. With respect to magnetostriction, this work suggests that stress-based clocking would lead to clock energy dissipation of just ~200 kT per device. Other recent work[608] has demonstrated strain-induced, 180-degree switching in anti-ferromagnetically coupled, single-domain magnets and short inverter chains. The SHE could be employed as a path to reduced energy clocking (i.e., 10-100X).[609]

Present status for pNML: Experimental results suggest that appropriately irradiated pNML structures[610] (to define dataflow directionality) can be controlled by a uniform, homogeneous, oscillating, global clock field.[611] Majority gates,[612] AF-lines,[611] multi-plane signal crossings,[613] and full adders[586,614] have all been experimentally demonstrated with this approach. Notably, Irina *et al.*[615] report the experimental demonstration of a three-dimensional majority gate (where input magnets reside in different planes). Each input combination was tested 50 times at room temperature. In each instance – and given the same clock window – the gate produced the correct output value. This could enable other compact and robust circuits (such as the five-magnet full adder discussed by Perricone *et al.*[616]). When considering I/O and clocking, field coupled electrical inputs have been demonstrated.[617] Also, large arrays of pNML devices could be controlled with on-chip inductor structures[618] that could be coupled with a capacitance in an LC oscillator – which opens the door to adiabatic energy recycling. Devices with PMA are also amenable to voltage-controlled clocking.[619]

Indeed, as noted above, small lines of pNML devices have been clocked via the SHE.[589] If 100 ps pulses are achievable, that work reports that the energy-delay product (EDP) of a pNML-based 32-bit adder would best that of low power CMOS. Individual pNML devices have also been clocked with on-chip inductor structures at 10 MHz. Simulation-based studies[620] suggest that a NAND/NOR operation would require just 2.8 aJ (assuming 200 nm × 200 nm devices and 50 MHz frequency and 10 functional layers of devices). Monolithic 3D NML co-processors have also been proposed.[621]

Active research on reliable switching work from 2008 suggests that in a soliton operating mode, dipole-to-dipole coupling could be insufficient to prevent thermal noise from inducing premature/random switching.[622] In that work, at the device-level, magnetocrystalline biaxial anisotropy could further promote hard axis stability of an iNML ensemble. Alternatively, adiabatic switching[623] and/or field gradients could potentially mitigate the effects of premature switching. Simulations suggest that NML circuits could tolerate some field misalignment.[624] Whether or not a circuit ultimately exhibits reliable and deterministic switching is very much a function of how it is clocked and requires additional study. More recently, nanomagnetic structures with spatially uniform clock fields,[625] leveraging shorter range exchange coupling between adjacent nanomagnets[626] (i.e., when compared to larger range parasitics that may be associated with dipole coupling), and nanoscale magnetic ratchets[627] (i.e., where specially

shaped magnets and strain are employed to achieve deterministic, 180-degree rotations) have all been explored and could potentially help to achieve more reliable magnetic switching.

Active research on fault tolerant architectures should be explored. As one example, stochastic computing (SC) could be an effective architectural strategy. Here, serial bit streams or parallel "bundles" of wires are used to encode probability values to represent and process information.[628] While bit streams/wire bundles are digital, information is conveyed through the statistical distribution of the logical values. With physical uncertainty, the fractional numbers correspond to the probability of occurrence of a logical one versus a logical zero. Computations in the deterministic Boolean domain are transformed into probabilistic computations in the real domain. Complex functions with simple logic are possible.

Bit flips afflict all the bits in the stream with equal probability. The result of bit flips is a mere fluctuation in the statistics of the stream, not a catastrophic error. Thus, SC enables meaningful computation even with high device error rates.[628] Furthermore, the SC architecture is pipelineable by nature. As the length of the stochastic bit stream increases, the precision of the value represented by it also increases. This allows a system to tradeoff precision with computation time. Thus, higher error rates that NML might experience can be tolerated by SC architectures. Pipelined SC architectures are a natural fit for inherently pipelined NML. Venkatesan *et al.*[629] and Perricone *et al.*[630] report examples of initial circuit design and benchmarking efforts in this area.

Active research on energy-efficient clocking including voltage controlled clocking should continue to be pursued – not only for benefits with respect to energy (e.g., as articulated by Nikonov and Young[631]), but also with respect to the fine-grained control it provides for an NML ensemble (which is useful in reducing error rates[632] as well as architecturally[618]). Domain-wall based switching could be another viable alternative for clocking.[633]

3.4.3. EXCITONIC DEVICES

Excitonic devices are based on excitons as computational state variables. Excitonic devices are suited to the development of an advanced energy-efficient alternative to electronics due to the specific properties of excitons: 1) Excitons are bosons and can form a coherent condensate with vanishing resistance for exciton currents and low switching voltage for excitonic transistors. This allows creating energy-efficient computation with power consumption per switch significantly smaller than in electronic circuits. 2) Excitonic signal processing can be directly coupled to optical communication in exciton optical interconnects. 3) The sizes of excitonic devices are scaled by the exciton radius and de Broglie wavelength that are much smaller than the photon wavelength. Furthermore, excitons can be efficiently controlled by voltage. This gives the opportunity to realize excitonic circuits at scales much smaller than for photonic devices.

The advantages listed above are realized using specially designed indirect excitons, IXs. An IX is a bound pair of an electron and a hole in separated layers. The properties of IXs make them different from conventional excitons and suitable for the development of energy-efficient computing: 1) IXs have oriented electrical dipole moments. As a result, the IX energy and IX currents are controlled by voltage allowing the realization of a field effect transistor operating with IXs in place of electrons. 2) The IX emission rate can be tuned over many orders of magnitude. Turning the emission off allows the realization of multi-element IX circuits with suppressed losses while turning it on allows fast write and readout. 3) The low overlaps between electrons and holes in IXs allow the realization of a coherent condensate with the suppressed thermal tails and dissipationless IX currents enabling energy-efficient computation.

Experimental proof-of-principle for excitonic devices including IX transistors,[634] diodes,[635] and CCD[636] was demonstrated. IX condensate and coherent IX currents[637] and, recently, long range coherent IX spin currents[638] were observed at low temperatures. New heterostructures based on single-atomic-layers of transition-metal dichalcogenide (TMD) for room-temperature IX circuits were proposed.[639] Recent progress includes the realization of IXs at room temperature in TMD heterostructures,[640] discovery of IX coherent spin currents in GaAs heterostructures[641], development of first split-gate device for IXs, the basic mesoscopic device[642], development of advanced platform for high-mobility excitonic devices[643], development of TMD heterostructures with small IX linewidth and finding charged IXs, indirect trions. At present, the studies are focused on the development of basic concepts of excitonic devices at low temperatures using GaAs heterostructures and development of room-temperature excitonic devices using TMD heterostructures.

3.4.4. TRANSISTOR LASER

The Light-Emitting Transistor (LET)[644] and Transistor Laser (TL)[645,646] utilize a fundamental characteristic of bipolar transistors - that electron-hole recombination in the base is an essential feature of the transistor and that the resulting photon signal in a direct-bandgap base is correlated to the electrical signal driving and being driven by the device. The TL can be thought of as a 5 terminal heterojunction bipolar transistor (HBT) with 3 conventional electrical terminals (emitter, base, and collector) and 2 optical terminals (input-generation and output-recombination).[647] Very-high-speed transmission and processing are enabled by the projected capability to achieve over 200 GHz bandwidths in the GaAs- or InP-based devices.[648] An advantage of the TL is that a single epitaxial layer structure can be used for devices that generate photons, detect photons, and perform electronic functions. The layer structure of the TL resembles a heterojunction bipolar transistor with features added to enhance base

recombination and control base transit time.[646,649] When used to realize conventional logic architectures, for example NOR gates,[650] the key advantage is speed. With processing-intensive operations and using the energy-delay product as a metric for comparison, a 30–100 times improvement is expected over conventional CMOS, leading to both faster processing and improved energy efficiency. An even greater benefit might be achieved through the use of architectures that perform electronic-photonic processing in the analog domain.

The first demonstration of lasing in the TL occurred in 2004. Since that time, progress has been made on understanding the device physics and on using the TL for discrete optical interconnects. A key initial objective has been examining factors affecting device bandwidth. Edge-emitting TLs with large active regions (200 μm × 1 μm) have been modulated to 22 Gbps and have shown a measured bandwidth of 10.4 GHz.[651] Relative intensity noise (RIN) as low as -151 dB/Hz has also been demonstrated, showing an approximately 28 dB improvement over diode lasers.[652] To improve speed and enable integration, reducing the size of the active region is critical. For that reason, Vertical-Cavity Transistor Lasers (VCTL) have been examined and demonstrated.[653] Initial VCTLs had limited temperature range due to misalignment of the cavity reflectivity and gain peaks. More recently, work has been underway to show that electronic-photonic logic can be made using the transistor laser. The initial target is a TL-based NOR gate.

The ultimate performance in both power and speed will be achieved as the device is size is scaled, as projected performance to bandwidths in excess of 100 GHz has a sound rationale but has yet to be realized. The use of vertical-cavity structures to reduce the device footprint has been a first step in the scaling process but further work is needed on microcavity vertical-cavity transistor lasers (VCTLs). Scaling beyond micron-scale devices such as this is possible, but the key will be the design of optical structures such as photonic crystal cavities that will enable small numbers of photons to be captured and directed to act on other TL structures. As scaling advances, further examination of device physics to reduce the effective minority carrier radiative lifetime will be key, along with the examination of effects that might impact the modulation response. Further work is also needed on InP-based devices (1310 and 1550 nm emission) to facilitate the use of silicon waveguides for optical signal routing. Additional questions at the architecture level involve the best way to use the TL in computer systems. What is enabled by having very high speed optical links? What architectures make sense for electronic-photonic NOR gates? Are other approaches to computation enabled, such as analog methods?

3.4.5. MAGNETOELECTRIC LOGIC

The earliest magneto-electric device concepts were based on a magnetic tunnel junction structure [1,2], which consists of two ferromagnetic (FM) layers separated by a non-magnetic insulator where the device resistance is determined by the relative orientation of the magnetization of the two FM layers. The magnetization of the free layer is exchange coupled to the Cr2O3 (or other magneto-electric) interface magnetization. A bias voltage applied across a magneto-electric layer, like chromia Cr2O3, layer reverses the interface magnetization, which in turn switches the magnetization of the free layer [3-5]. A lot of thought has been given to how this might be implements as logic elements [6-12], and to some extent benchmarked against CMOS [8,9,13]. The disadvantage is that while much faster than many spintronics device, there is long delay time in device operation, due to the slow speed of switching a ferromagnet.

Other magneto-electric devices, like the composite–input magnetoelectric–based logic technology (CoMET) [14] are limited by the switching speed of the ferroelectric and domain wall motion. The basis of these devices is an input switches a ferroelectric material, in contact with a ferromagnet with in-plane magnetic anisotropy placed on top of an intra-gate ferromagnet interconnect with perpendicular magnetic anisotropy. The input voltage nucleates a domain wall while a current is used to drive the domain wall to the output end of the device. A similar magneto-electric device structure, but now using spin-orbit coupling, has also been proposed [15]. Again, both devices will have long delay times, due to the slow switching speed of the ferromagnetic layer, and in the case of the CoMET device, the slow speed of domain wall propagation - where using higher currents to drive the domain wall at faster velocities comes at an energy cost. Also using spin orbit coupling, but now explicity also using a magneto-electric layer for electrical control of exchange bias of a laterally scaled spin valve is the nonvolatile magneto-electric spin-orbit (MESO) logic [16], but the delay time is limited again by the switching speed of the ferromagnetic layer.

More recently attention [5,17-23] has shifted to the magneto-electric spin field effect transistor (the ME-spinFET), where the most basic structure is outlined in Figure 1. Magneto-electric transistor schemes are based on polarization of the semiconductor channel, by the boundary polarization of the magneto-electric gate. The advantage to the magneto-electric field effect transistor is that such schemes avoid the complexity and detrimental switching energetics associated with magneto-electric exchange-coupled ferromagnetic devices. Spintronic devices based solely on the switching of a magneto-electric, will have a switching speed will be limited only by the switching dynamics of that magneto-electric material and above all are voltage controlled spintronic devices. Moreover, these magneto-electric devices promise to provide a unique field effect spin transistor (spin-FET)-based interface for input/output of other novel computational devices. This is spintronics without a ferromagnet, with faster write speeds (<20 ps/full adder), at a lower cost in energy (<20 aJ/full adder) [23], greater temperature stability

(operational to 400 K or more), and scalability, requiring far fewer device elements (transistor equivalents) than CMOS. These do differ from the conventional field transistor in that the ME-FET must be both top and bottom gated, son the result is that this is a 4, not 3 terminal transistor [17-22].

The anti-ferromagnet spin-orbit read (AFSOR) logic device structure (Figure 2) has interesting advantages: the potential for high and sharp voltage 'turn-on'; inherent non-volatility of magnetic state variables; absence of switching currents; large on/off ratios; and multistate logic and memory applications. The design will provide reliable room-temperature operation with large on/off ratios (>107) well beyond what can be achieved using magnetic tunnel junctions [21,22]. Again, the core idea is the use of the boundary polarization of the magneto-electric to spin polarize or partly spin polarize a very thin semiconductor, ideally a 2D material, with very large spin orbit coupling.

If the semiconductor channel retains large spin orbit coupling, then the spin current, mediated by the gate boundary polarization, may be enhanced and, to some extent, topologically protected. The latter implies that each spin current has a preferred direction, as indicated in Figure 2.

The silicon CMOS majority gate (left) requires 13 components. The ME-spinFET majority gate requires, including clocking, of 6 components. This represents an area improvement of over 50%, assuming similar size transistors. This is equivalent to greater than one process node. If we split the magnetoelectric side of the gate, so that the channel can independently be spin polarized up or down, this results in a component reduction from the previous best for the MEFET of six, down to four components, a further 50% reduction over the standard MEFET circuit, and a reduction to less than 30% in area compared to CMOS [24].

There is a variant of Figure 3, where inversion symmetry is not as strictly broken, that leads to a nonvolatile spintronics version of multiplexer logic (MUX). The magneto-electric spin-FET multiplexer (Figure 3) also exploits the modulation of the spin-orbit splitting of the electronic bands of the semiconductor channel through a "proximity" magnetic field derived from a voltage-controlled magneto-electric material. Here, by using semiconductor channels with large spin-orbit coupling, we expect to obtain a transverse spin Hall current, as well as a spin current overall. Depending on the magnitude of the effective magnetic field in the narrow channel, we anticipate two different operational regimes. Like the AFSOR magneto-electric spin FET, the magneto-electric spin-FET multiplexer in Figure 3 uses spin-orbit coupling in the channel to modulate spin polarization and hence the conductance (by spin) of the device. There is a source-drain voltage and current difference, between the two FM source contacts, due to the spin-Hall effect when spin-orbit coupling is present. This output voltage can be modulated by the gate or gates, which influences the spin-orbit interaction in the channel especially when it is both top and bottom gated especially. The spin-Hall voltage in the device can be increased by using different FMs in the source and drain. To increase the spin fidelity of current injection at the source end, one could add a suitable tunnel junction layer (basically a 1nm oxide layer) between the magnetic source and the 2D semiconductor channel. This latter modification would result in diminished source-drain currents though. Again, there is a reduction is delay time and energy cost because these devices are nonvolatile, there is no magnetization reversal of a ferromagnet involved and the implementation of this device concept would require only 5 components for a majority gate compared to the 13 components required of a silicon CMOS majority gate.

The challenges in pushing forward these technologies extends not only to the fabrication and characterization of a new generation of nonvolatile magneto-electric devices, but also to ascertaining the optimal implementation of CMOS plug in replacement circuits. Questions that need to be resolved include demonstration that the magneto-electric devices can be scaled to less than 10 nm, and this includes finding a suitable 2D channel material that can be polarized by exchange coupling with the boundary polarization of the magneto-electric and yet does not suffer from large scale edge scattering. Experimental demonstration of limits to the switching speeds of any antiferromagnetic magnetic electric remain absent. That said, the magneto-electric transistor has far fewer challenges to implementation than the magneto-electric magnetic tunnel junction, so, not surprisingly, there is a shifting of development effort toward those and related devices for both memory and logic.

4. Emerging Application Areas

4.1. Emerging Devices for Security Applications

4.1.1. Introduction

Like performance, power, and reliability, hardware security is becoming a critical design consideration. Hardware security threats in the IC supply chain, include 1) counterfeiting of semiconductor components, 2) side-channel attacks, 3) invasive/semi-invasive reverse engineering, and 4) IP piracy. A rapid growth in the "Internet of Things" (IoT) only exacerbates problems. While hardware security enhancements and circuit protection methods can mitigate security threats in protected components, they often incur a high cost with respect to performance, power and/or cost.

Advances in emerging, post-CMOS technologies may provide hardware security researchers with new opportunities to change the passive role that CMOS technology currently plays in security applications. While many emerging technologies aim to sustain

Moore's Law-based performance scaling and/or to improve energy efficiency,[654,655,656] emerging technologies also demonstrate unique features that could drastically simplify circuit structures for protection against hardware security threats. Security applications could not only benefit from the non-traditional I-V characteristics of some emerging devices, but also help shape research at the device level by raising security measures to the level of other design metrics.

At present, many emerging technologies being studied in the context of hardware security applications are related to designing physically unclonable functions (PUFs). Many post-CMOS devices[657,658,659] have been suggested as a pathway to a PUF design. (More detailed reviews are also available.[660]) With a PUF, challenge/response pairs are mapped (typically in a trusted environment). Responses are derived from natural/random variations and disorders in an integrated circuit that cannot be copied (or *cloned*) by an adversary. PUFs have been employed for tasks such as device authentication,[660] to securely extract software,[661] in trusted Field Programmable Gate Arrays (FPGAs),[662] and for encrypted storage.[661] Post-CMOS devices also find utility as random number generators (RNGs) that may be employed for secure communication channels (e.g., to generate session keys[660]). That said, while intriguing, PUFs and RNGs may only cover a small part of the hardware security landscape. (Furthermore, one must be careful that PUF designs based on emerging technologies do not depend on device characteristics that a designer would like to *eliminate* when considering utility for logic or memory.)

Given the many emerging devices being studied[654] and that few if any devices were proposed with hardware security as a "killer application," this document also reports initial efforts as to how the unique I-V characteristics of emerging transistors that are not found in traditional MOSFETs could benefit hardware security applications.

Below, we review the efforts described above, beginning with efforts to design PUFs and RNGs with emerging technologies. How device characteristics can enable novel circuits to achieve hardware security-centric ends such as IP protection, logic locking, and the prevention of side channel attacks are also discussed.

4.1.2. PHYSICALLY UNCLONABLE FUNCTIONS (PUFS) AND EMERGING TECHNOLOGIES

A variety of different emerging logic and memory technologies have been considered in the context of PUFs. As has been reviewed,[660] variations in the required write time in spin torque transfer random access memory (STT-RAM) was proposed to create a domain wall memory PUF.[657] Other structures based on magnetic tunnel junctions have also been proposed.[663,664] Variations in write times have also been exploited to produce unique responses in phase change memory (PCM) arrays.[665] The variability of ReRAM presents a natural opportunity for PUF implementation, and array demonstration has been reported.[666, 667] At the array-level, variations in diode resistivity have also been used to derive challenge/response pairs from crossbar structures.[668] PUFs based on graphene[669] and carbon nanotubes have also been proposed/considered.[670]

As a more representative case study, prior work[660] considers an array structure based on process variation in memristors[671,672] to create a PUF structure (referred to as *NanoPUF*[660]). NanoPUF is based on 1) a crossbar with memristors. 2) A challenge is applied to the memristor array by using a row decoder to apply a voltage amplitude (V_{dd}) to a given row that can vary in duration; a column decoder connects a given column to a resistance R_{load}. All other rows and columns remain floating. 3) A response circuit (to collect outputs to different challenges) would consists of R_{load} and a current comparator that compares I_{out} from a given column to a reference current I_{ref}. A logic 1 might be recorded if $I_{out} > I_{ref}$, while a logic 0 might be recorded if $I_{out} < I_{ref}$. With respect to PUF functionality, when a write pulse is applied, natural process variations will cause some memristors to turn on (leading to a logic 1), and others to remain off (leading to a logic 0). While the time of the right pulse serves as one variable,[671] the pulse's duration and amplitude may also be varied.[672]

4.1.3. RANDOM NUMBER GENERATORS (RNGS) AND EMERGING TECHNOLOGIES

The inherent randomness in emerging devices can also be used to generate random numbers.[660] As a representative case study, prior work[660] explores an approach based on contact-resistive random access memory (CRRAM).[673] (Note that a CRRAM device may be based on a layer of silicon dioxide that is sandwiched between two electrodes; the bottom electrode could simply be the drain of a CMOS transistor – which in turn suggests that RNGs based on emerging technologies can be CMOS compatible.[674])

During operation, the current flowing in a filament channel will be (randomly) impacted by any electrons trapped in the insulating layer. If a high voltage is applied to a device, the current in the filament channel will be large and not impacted by trapped electrons. However, with the application of a lower voltage, the width of a filament will shrink, and the trapped electrons *will* (randomly) influence output current.[674] Indeed, RNGs based on emerging devices[674] can successfully pass randomness tests such as those provided by the National Institute of Standards and Technology (NIST).

As random number are derived from current passing through filaments, memristors, PCM, and RRAM devices can also be leveraged to build similar RNGs.[660] Additional device options for random number generation are discussed in section 5.3.1.

4.1.4. OTHER HARDWARE SECURITY PRIMITIVES BASED ON EMERGING TECHNOLOGIES

Below, other security-centric primitives (non-PUFs and non-RNGs) based on emerging technologies are also discussed. How new devices might be employed for IP protection and to prevent side channel attacks are considered. In each section, device characteristics of interest are discussed first. Subsequent discussions then consider how device characteristics can be employed to achieve a security centric end.

4.1.4.1. EMERGING TECHNOLOGIES FOR IP PROTECTION

Tunable Polarity: In many nanoscale FETs (45nm and below), the superposition of n-type and p-type carriers is observable under normal bias conditions. The ambipolarity phenomenon exists in various materials such as silicon,[675] carbon nanotubes[676] and graphene.[677] By controlling ambipolarity, device polarity can be adjusted/tuned post-deployment. Transistors with a configurable polarity – e.g., carbon nanotubes,[678] graphene,[679] silicon nanowires (SiNWs),[680] and transition metal dichalcogenides (TMDs)[681] – have already been experimentally demonstrated.

As more detailed examples, SiNW FETs have an ultra-thin body structure and lightly doped channel which provides the ability to change the carrier type in the channel by means of a gate. FET operation is enabled by the regulation of Schottky barriers at the source/drain junctions. The control gate (CG) acts conventionally by turning the device on and off via a gate voltage. The polarity gate (PG) acts on the side regions of the device, in proximity to the source/drain (S/D) Schottky junctions, switching the device polarity dynamically between n- and p-type. The input and output voltage levels are compatible, enabling directly-cascadable logic gates.[682]

Ambipolarity is an inherent property of TFETs due to the use of different doping types for drain and source if an n/i/p doping profile is employed.[683] By properly biasing the n-doped and p-doped regions as well as the gate, a TFET can function either as an n- or p-type device, and no polarity gate is needed. As the magnitude of ambipolar current can be tuned (i.e., reduced) via doping or by increasing the drain extension length,[683] one can envision fabricating devices that could be better suited for logic as well as security-related applications. Given that the screening length in TMD devices scales with their body thickness, one can achieve substantial tunneling currents.

Polymorphic logic gates: The ability to dynamically change the polarity of a transistor opens the door to define the functionality of a layout or a netlist post fabrication. Though one may use field programmable gate arrays (FPGAs) to achieve the same goal, FPGAs cannot compete with ASICs in terms of performance and power, and an FPGA's reliance on configuration bits being stored in memory introduces another vulnerability. Security primitives to be discussed can serve as building blocks for IP protection, IP piracy prevention, and to counter hardware Trojan attacks.

Polymorphic logic circuits provide an effective way for logic encryption such that attackers cannot easily identify circuit functionality even though the entire netlist/layout is available. However, polymorphic logic gates have never been widely used in CMOS circuits mainly due to the difficulties in designing such circuits using CMOS technology.

SiNW FET based polymorphic gates to prevent IP piracy have been introduced.[684,685] If the control gate (CG) of a SiNW FET is connected to a normal input while the polarity gate (PG) is treated as the polymorphic control input, we can easily change the circuit functionality through different configurations on the polymorphic control inputs without a performance penalty. For example, a SiNW FET based NAND gate can be converted to a NOR gate, whereas a CMOS-based NAND cannot be converted to a fully functioning NOR by switching power and ground.

TFET-based polymorphic logic circuits have also recently been developed.[686] By properly biasing the gate, the n-doped region, and the p-doped region, a TFET device can function either as an n-type transistor or p-type transistor. If the n-doped region of the two parallel TFETs is connected to V_{DD}, and the p-doped region of the bottom TFET is connected to GND, the circuit behaves like a NAND gate. If the n-doped region of the two parallel TFETs is connected to GND and the p-doped region of the bottom TFET is connected to V_{DD}, the circuit behaves as a NOR gate. By using two MUXes (one at the top and the other at the bottom) to select between the two types of connections, the circuit then functions as a polymorphic gate where the control to the MUXes forms a 1-bit key.[686]

One can readily design polymorphic functional modules using the low-cost polymorphic logic gates built from either SiNW FETs or TFETs that only perform a desired computation if properly configured. If some key components (e.g., the datapath) in an ASIC are designed in this manner, the chip is thus encrypted such that a key, i.e., the correct circuit configuration, is required to unlock the circuit functionality. Without the key, invalid users or attackers cannot use the circuit. Thus, IP cloning and IP piracy can be prevented with extremely low performance overhead. A 32-bit polymorphic adder using SiNW FETs has been designed and simulated. Two pairs of configuration bits (with up to 32-bits in length) are introduced and the adder can only perform addition functionality if the correct configuration bits are provided.

Camouflaging Layout: Split manufacturing and IC camouflaging are used to secure the CMOS fabrication process, albeit with high overhead and decreased circuit reliability. With CMOS camouflaging layouts, both power and area would increase

significantly in order to achieve high levels of protection.[687] A CMOS camouflaging layout that can function either as an XOR, NAND or NOR gate requires at least 12 transistors. Emerging technologies help reduce the area overhead. Recent work has demonstrated that only 4 SiNW FETs with tunable polarity are required to build a camouflaging layout that can perform NAND, NOR, XOR or XNOR functionality.[688,689] Again, the SiNW FET based camouflaging layout has more functionality and requires less area than CMOS counterparts and could offer higher levels of protection to circuit designs.

Security Analysis: Logic obfuscation is subject to brute-force attacks. If there are *N* polymorphic gates incorporated in the design, it would take 2^N trials for an attacker to determine the exact functionality of the circuit. As the value of *N* increases, the probability of successfully mounting a brute-force attack becomes extremely low. In a preliminary implementation of 32-bit adder, the incorporated key size is 32 bit.[686] The probability that an attacker can retrieve the correct key becomes $1/2^{32}$ (2.33×10^{-10}). Obviously, polymorphic based logic obfuscation techniques are resistant to a conventional brute-force attack. With respect to camouflaging layouts, given that our proposed SiNW based camouflaging layout can perform four different functions, the probability that an attacker can retrieve the correct layout is 25%. Therefore, if *N* SiNW FET camouflaging layouts are incorporated in a design, the attacker has to compute up to 4^N times to resolve the correct layout design. Compared to polymorphic gate-based logic obfuscation, camouflaging layout embraces higher security level but with larger area overhead.

4.1.4.2. EMERGING TECHNOLOGIES TO PREVENT SIDE-CHANNEL ATTACKS

Many post-CMOS transistors aim to achieve steeper subthreshold swing, which in turn enables lower operating voltage and power. Many devices in this space also exhibit I-V characteristics that that are not representative of a conventional MOSFET. An example of how to exploit said characteristics for designing hardware security primitives is discussed.

Steep slope transistors: TFETs have been exploited to design current mode logic (CML) style light-weight ciphers.[690,691] The high energy carriers in TFETs can be filtered by the gate-voltage-controlled tunneling such that a sub-60 mV/decade subthreshold swing is achievable at room temperature.[692] With improved steep slope and high on-current at a low supply voltage, TFETs could enable supply voltage scaling to address challenges such as undesirable leakage currents, threshold voltage reduction, etc. Different types of TFETs have been developed and fabricated.[692,693]

Bell-Shaped I-Vs: Emerging transistor technologies may also exhibit bell-shaped I-V curves. Symmetric graphene FETs (SymFETs) and ThinTFETs are representatives of this group. In a SymFET, tunneling occurs between two, 2-D materials separated by a thin insulator. The I_{DS}-V_{GS} relationship exhibits a strong, negative differential resistance (NDR) region. The I-V characteristics of the device are "bell-shaped," and the device can remain off even at higher values of V_{DS}. The magnitude of the current peak and the position of the peak are tunable via the top gate (V_{TG}) and back gate (V_{BG}) voltages of the device.[684] Such behavior has been observed experimentally.[694,695] More specifically, V_{TG} and V_{BG} change the carrier type/density of the drain and source graphene layers by the electrostatic field, which can modulate I_{DS}. ITFETs or ThinTFETs may exhibit similar I-V characteristics.[696]

Preventing fault injection: Side-channel analysis, such as fault injection, power, and timing, allows attackers to learn about internal circuit signals without destroying the fabricated chips. Countermeasures have been proposed to balance the delay and power consumption when performing encryption/decryption at either the algorithm or circuit levels.[697] These methods often cause higher power consumption and longer computation time in order to balance the side-channel signals under different conditions. Thus, an important goal is to prevent fault injection and to counter side-channel analysis by introducing low-cost, on-chip voltage/current monitors and protectors. Graphene SymFETs, which have a voltage-controlled unique peak current can be used to build low-cost, high-sensitivity circuit protectors through supply voltage monitoring.

Recent work has developed a SymFET-based power supply protector.[684,685] With only two SymFETs, the power supply protector can easily monitor the supply voltage to ensure that the supply voltage to the circuit-under-protection is within a predefined range. In the event of a fault injection, the decreased supply voltage will power down the circuit rather than injecting a single-bit fault,[685] and can thus protect the circuit from fault injection attacks. If one uses V_{out} as the power supply to a circuit under protection (e.g., an adder), due to the bell-shaped I-V characteristic of the SymFET, an intentional lowering of V_{DD} cuts off the power supply. Thus, the sum and carry-out of the full adder output is '0', and no delay related faults are induced. A similar CMOS power supply protector would require op-amps for voltage comparison. As a result of the voltage/current monitors developed thus far, voltage/current-based fault injections can be largely prevented. By inserting the protectors in the critical components of a given circuit design, the power supply to these components can be monitored and protected.[686] (SymFET-based Boolean logic is also possible.[698])

Preventing differential power analysis (DPA): As an advanced side-channel attack scheme, DPA employs analysis of statistic power consumption measurements from a crypto system to obtain secret keys. Since the introduction of DPA[700], there has been many efforts to develop low-cost and efficient countermeasures. Countermeasures are generally classified into two categories: 1) algorithm-level solutions and 2) hardware-level solutions.

Algorithm-level solutions aim to design cryptographic algorithms that can withstand a certain amount of information leakage,[699] e.g., frequently changing the keys to prevent the attacker from collecting enough power traces[700] or using masking bits during the internal stages to limit information leakage.[701]

A more practical circuit-level method for preventing DPA attack leverages a *sense amplifier-based logic* (SABL) or *current mode logic* (CML) for cryptographic algorithm implementations.[702] A CML gate includes a tail current source, a current steering core and a differential load. A CML gate will switch the constant current through the differential network of input transistors, utilizing the reduced voltage swing on the two load devices as the output. Although CML is not widely used in mainstream circuit design, its unique features, namely low latency and stable power consumption, can be leveraged to serve as a countermeasure against a DPA attack.

The strength of the CML-based approach is the constant power consumption of differential logic which can counter power-based attacks as operation power is independent of processed data. The drawback with these (mostly CMOS-based) logic designs, is their large area and power consumption when compared to static single ended logic. When considering hardware for the IoT (where the systems can be severely power constrained), system designers are presented with a dilemma in which they need to choose either high security or low power consumption. Emerging transistor technologies could help mitigate risks of DPA attacks while maintaining low power consumption.

Recent work has implemented a standard cell library of TFET CML gates and conducted a detailed study of their performance, power and area with respect to CMOS equivalents.[703] Standard cells were used to implement and evaluate TFET-based CML on a 32-bit KATAN cipher (a light-weight block cipher). All KATAN ciphers share the same key schedule with the key size of 80 bits as well as the 254-round iteration with the same non-linear function units.[704]

The two CML implementations consume less gate equivalents and area compared to the two static counterparts given that the majority of KATAN32 is made up by the D flip flops. The area of TFET CML KATAN32 is 1.441 μm^2, which is about 60% less than the Static TFET KATAN32. The power consumption of TFET CML (9.76 μW) is slightly lower than *static* CMOS (9.96 μW). It also outperforms CMOS CML.

Moreover, the correlation coefficient of a TFET static KATAN32 reaches its highest when the correct keys are applied. By comparison, the correlation coefficient of TFET CML KATAN32 is much more scattered, and all four hypothetical keys are equally distributed. Thus, the TFET CML KATAN32 implementation can successfully counteract CPA. Because the power consumption is mainly determined by AND/XOR logic gates of two nonlinear functions – and the effect of CPA is maximized – the correlation coefficients for KATAN32 are higher on average than other block ciphers, e.g., CPA on S-box[705].

4.2. Cryogenic Electronics

With the 2018 Edition of the IRDS Roadmap, findings on cryogenic electronics and quantum information systems are captured in a standalone chapter, accessed at this link.

5. Emerging Device-Architecture Interaction

5.1. Introduction

Emerging Beyond-CMOS devices will likely have new issues at the interfaces between the device level and higher levels (*e.g.*, circuit, architecture and application) of computer design. Many of the emerging device classes that are currently being explored are not intended simply as “drop-in” replacements for CMOS devices, but will require new types of circuit designs, new functional module architectures, and even new software to best utilize the new devices’ capabilities.

Novel design issues that span the device and architecture levels need to be considered when adopting new low-level computing paradigms. Devices may be organized in radically new ways to carry out computation in a very different style from what we may consider the most “conventional” computing paradigm, which has relied on standard combinational and sequential irreversible Boolean logic. Examples of such unconventional or alternative computing paradigms include:

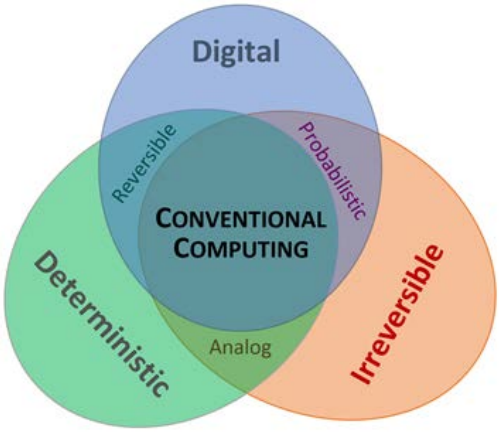


Figure BC5.1. Categorization of Conventional vs. Alternative Computing Paradigms Addressed in This Section

Note: The conventional computing paradigm is designed to be digital, deterministic, and irreversible. Typical analog computing schemes relax the digital requirement while maintaining (at least approximate) determinism and are often physically irreversible. In probabilistic computing, we abandon the requirement for determinism, while preserving the irreversible, digital nature of the computation. And typical reversible computing techniques maintain the digital, deterministic nature of computation while attempting to avoid irreversibility. More generally, alternative computing paradigms may respect only one (or none) of the three illustrated constraints.

Analog computing (§5.2) – This broad category of non-digital computing paradigms includes some of the neural models (discussed below) but also spans a much broader range of other analog approaches such as coupled oscillators (§5.2.3.1),[706] energy-minimization/annealing systems (§5.2.4), and chaotic circuits (§5.2.3.2).

Neural (including neuromorphic or neural-inspired) computing (§5.2.2) – Many of the new devices that have been considered for use in this sub-paradigm of analog computing are envisioned to play a role analogous to biological synapses. At a higher level, a variety of overall neural computation schemes (analog, spiking, etc.) can be envisioned. While neural models (like any analog model) can be simulated in conventional digital CMOS, a more direct circuit-level implementation potentially offers substantial performance improvements (per unit power consumption and/or per unit cost). Two-terminal synapse-like devices are frequently considered for organization in crossbar arrays (§5.2.1) which then offers the potential to perform very efficient analog matrix operations (§5.2.1.1, §5.2.1.2). A variety of different physical state variables (*e.g.*, capacitive, resistive, magnetic) have been explored for encoding the synapse weights.

Probabilistic/stochastic circuits (§5.3) – In relation to §4.1.3, devices and circuits that produce truly nondeterministic or random outputs at the hardware level may be useful for accelerating probabilistic algorithms such as Monte Carlo or simulated annealing, for generating secure cryptographic keys, and for other applications.

Reversible (adiabatic and/or ballistic) computing (§5.4) – Computing paradigms that approach logical and physical reversibility offer the potential to greatly exceed the energy efficiency of all other approaches to general-purpose digital computation. Primitive devices for reversible computing may include devices having fairly conventional functions (such as switches or oscillators). These devices would need to be optimized differently to use quasi-reversible physical processes such as near-adiabatic state transitions, near-ballistic signal propagation, highly elastic interactions, and highly underdamped oscillations. Reversible devices also must be organized into circuits and architectures in tightly constrained ways, for reversibility at the logical as well as physical level.[896] Careful fine-tuning and optimization of analog circuit characteristics (*e.g.*, resonator quality factors or elasticity of ballistic interactions) remains a difficult and crucially important engineering challenge that must be met in order for this paradigm to realize its promise.

Quantum computing – Quantum computing[707] offers the potential to carry out exponentially more efficient algorithms for a variety of specialized problem classes.[708] Devices for quantum computing are very different from conventional devices, and fine-tuning their characteristics to avoid decoherence while organizing them effectively into scalable architectures has, to date, proved to be a formidable engineering challenge.[709] IRDS is beginning to address quantum computing this year in the new Cryogenic Electronics & Quantum Information Processing chapter (CEQIP). We will not address quantum computing further in the present section.

This categorization can be understood by reference to Figure BC5.1. However, the reader should please note that the material in this section does not comprise an exhaustive list of *all* possible new computing paradigms, new devices, new circuits, or new architectures. It is only intended to serve as a representative sample of several new general computing paradigms and specific technology concepts and as a starting point for further discussion of this overall subject area in future workshops.

5.2. ANALOG COMPUTATION

Analog computing attempts to let "physics do the computation" by using physical processes more directly (as opposed to through the traditional digital abstraction barrier) to compute complex functions. Historically, this required inefficient analog circuitry for all elements, and expensive analog to digital conversion, resulting in limited applications, specifically those requiring analog signal processing. Recently, new analog devices have enabled a new generation of efficient analog architectures. This is especially true for hybrid analog and digital systems where efficient designs may exploit analog preprocessing and computation prior to digitization. Analog preprocessing can reduce the required A/D precision and therefore reduce the system energy consumption by orders of magnitude.[710] Additionally, new architectures can be used for ultra-low-power co-processors for conventional CMOS designs. A key challenge is that analog signals are typically low precision, with energy and latencies increasing exponentially with higher bit precision. Fortunately, many machine learning and other applications are being developed that can tolerate such lower precision computation.

In this subsection, we review a number of recent examples of analog computational technologies, starting with some currently popular neural-inspired architectures that also have broader applications in linear algebra.

5.2.1. CROSSBAR ARCHITECTURES

Analog crossbars or memory arrays can perform low-precision matrix operations in parallel, by processing analog data directly at each memory element. Thus, n 1990, Carver Mead projected that custom analog matrix vector multiplications would be thousands of times more energy efficient than custom digital computation.[711] Because a digital memory must individually access each memory cell and move the data to a separate computation unit, digital systems consume more energy and incur longer latencies. Computing on larger crossbars/matrices allows for any analog overhead to be averaged out over many matrix elements. Any two- or three-terminal device that features a modifiable internal physical state variable (which might be, for example, a variable resistance, a variable capacitance, a stored charge, or a stored magnetic field) that modifies the device's behavior can be used as a building block for analog operations. Several different types of crossbar architectures are summarized in the following sections.

5.2.1.1. MATRIX VECTOR MULTIPLICATION (MVM) AND VECTOR MATRIX MULTIPLICATION (VMM)

MVM and VMM are key computational kernels underlying many different algorithms. There are several approaches to accelerating these kernels. Any programmable resistor such as a two-terminal resistive memory or a three-terminal floating gate cell can be used. Alternatively, a capacitive MVM can be designed by adding charge from capacitive memory elements.[712]

For many algorithms such as neural network inference (of an already-trained network), accelerating MVM accelerates the bulk of the computation, allowing for large system level gains. An $N \times N$ crossbar accelerates $O(N^2)$ operations, leaving only $O(N)$ inputs and outputs that need to be processed and communicated. This allows each unit of communication and processing costs to be amortized over N memory elements.

Analog VMMs have been used for experimental demonstration of threshold logic,[713] compressed sensing initial filtering,[714] robotic navigation and control,[715] adaptive filtering,[716] Fourier transforms[717] and more. Additionally, Analog VMM techniques have been used for ultra-low power classification and neural networks.[718]

5.2.1.1.1. RESISTIVE MVM AND VMM

Resistive MVMs are based on using Ohms law, $V = I \times R$, to perform multiplication, and Kirchhoff's current law on of to perform addition by summing currents. Programmable resistors are used to program the weights. Arranging the memory elements in an array allows for the entire operation to be performed in a single parallel step, giving a fundamental $O(N)$ energy and latency advantage over a standard digital memory that, at best, must access a memory array one row at a time.[719] An MVM and the transpose VMM can be performed on the same memory array, by changing whether the rows of an array are driven and the columns are read, or vice versa.

The key metrics for a resistive MVM are 1) the energy per multiply and accumulate, 2) latency per MVM, 3) crossbar and supporting circuitry area per matrix element, 4) crossbar dimensions, 5) input/output bit precision for digitally driven MVMs, and 5) the standard deviation of the noise or error per weight when programmed as a percentage of the weight range.

If high-resistance memory elements ($R_{on} = 100$ MΩ) with good analog properties are developed, one ReRAM based crossbar design projects that each multiply and accumulate operation will require 12 fJ when using 8-bit A/Ds and only 0.4 fJ when using 2-bit A/Ds.[720] The latency for a 1024×1024 MVM will only be 384 ns or 11 ns for 8-bit or 2-bit A/Ds respectively. This is over $100 \times$ better than an optimized SRAM based accelerator, which would require 2,700 fJ and 4,000 ns for 8 bits. The area per weight for the 8-bit A/D ReRAM accelerator is 0.05 μm^2, $16 \times$ better than the 0.8 μm^2 needed for an SRAM accelerator. The energy and latency are dominated by the A/D circuitry and not by the crossbar itself, with the A/D converters and digital circuitry occupying $10 \times$ the area of the ReRAM array itself.

To allow for large arrays and minimize parasitic resistance drops, high resistance (~100 MΩ) memory elements are needed. The higher the resistance, the larger the array possible, and the more any A/D costs and system level communication costs are amortized out. However, such high resistances would prolong and potentially complicate the process of programming each conductance value accurately to encode already-trained neural network weights or matrix element values.

A key design choice is the bit precision of the inputs and outputs to the crossbar. The fewer the bits needed by an algorithm, the more efficient the crossbar is. If analog or binary inputs/outputs can be used, the A/D costs can also be avoided. The inputs to the crossbar can be encoded in voltage, time, or digitally. Voltage encoding applies different voltages to represent different analog input values. This requires circuitry to create different input voltages, and it requires that the memory elements have a linear I-V relationship, greatly complicating the use of nonlinear access devices.[721] Encoding inputs in variable length pulses requires longer reads and an integrator to sum the resulting current. Digital encoding applies each bit of the input sequentially and then combines the result digitally. For digital encoding, the usefulness of lower order bits in the input is limited by the noise/errors on the highest order bit.

The precision with which each resistor needs to be programmed depends on the particular application. For neural network inference, the algorithm can be robust to read noise of up to 5% of the weight range or more.[722]

Many different memory elements can be used for the programmable resistor:

***ReRAM*:** ReRAM memory is very dense and can be integrated in the back end of the line, avoiding the use of chip area for the memory. A key challenge is maintaining good analog properties and high resistance at the same time. A thermal confinement method was proposed to realize analog ReRAM[723] and demonstrated 1Kb ReRAM array for facial recognition.[724] Several ReRAM crossbars have been demonstrated for inference.[725, 726]

Phase Change Memory: Phase-change memory (PCM) offers a wide range of analog memory states due to the large contrast between the amorphous and crystalline phases.[727] Key challenges for inference include reducing resistance drift due to amorphous relaxation and ensuring long retention at high operating temperatures. Cell designs that can suppress resistance drift have been proposed.[728, 729] Most VMM results using PCM to date have focused on in-situ training (see section on Outer-Product Update below).[752]

***LISTA/ENODe*:** New three terminal battery inspired devices including the Li-Ion Synaptic Transistor (LISTA)[730] and the electrochemical neuromorphic organic device (ENODe)[731] were recently proposed as an analog memory element. They are based on charging/discharging a battery. As a battery is charged, the resistance of the cathode changes. These devices have shown very good analog control but are currently too slow for training accelerators, with write pulses on the order of a millisecond. Since these devices are effectively tiny batteries, an access device is needed on the third "gate" terminal, to prevent the device from discharging when the state is not being written in an array configuration.

Floating Gate: Floating gate-based synapses were first developed in 1994.[732] They are modified EEPROM devices and can be fabricated in a standard CMOS process. They can be programmed to within 0.2% accuracy,[733] and full systems have been developed to allow arbitrary devices in an array to be programmed.[734] The FG VMM is a slightly modified EEPROM array with the associated density from such a structure. EEPROM devices already store 4 bits (16 levels) in a single transistor of 100 nm × 100 nm area in 32nm process.[735] Commercial EEPROM manufacturers have shown devices at 15 nm and 19nm[736,737] and [738]). EEPROM devices are found on every CMOS IC node, including 7nm and 11nm nodes. At these nodes, we still expect very small capacitors to retain 100s of quantization levels (7-10 bits) limited by electron resolution; in practice, larger capacitors are used, resulting in sufficiently high potential resolution. One expects EEPROM linear scaling down to 10nm process to result in a 30 nm × 30 nm or smaller array pitch area.

Capacitor-on-Gate: A recent proposal was to tie a small capacitor that can be programmed with standard CMOS devices to the gate of a read transistor[739]. In contrast to DRAM, where the charge on the capacitor is transferred through a select transistor onto a bitline for readout, here the voltage on the capacitor modulates the conductance of a read transistor by direct attachment to its gate terminal. Although the charge leaks away with a time-constant of milliseconds, the training process can succeed if the time-per-example is at least 100,000x smaller than the decay constant (e.g., 20ms decay constant and 200ns-per-training-example).[740] In order to have good update linearity so that the amount of charge added and subtracted are balanced, additional large transistors can be used in each unit cell.[739,740] Recently, Ambrogio et al. introduced a combined PCM+capacitor-on-gate unit-cell, in which the PCM provided the non-volatile storage, the capacitor-on-gate devices provided high update linearity with a small number of transistors, and variability between charge-addition and charge-subtraction was compensated upon weight transfer from capacitor-on-gate cell to the PCM devices using a "polarity inversion" technique[741]. This unit-cell was shown to allow GPU-equivalent training accuracies, despite the known imperfections of PCM devices and typical fab-level CMOS variability in the capacitor-on-gate devices.[741]

5.2.1.1.2. CHARGE-BASED ANALOG ARRAYS FOR VMM

Charge-based analog arrays are amenable to very low energy and high-density parallel implementations of vector-matrix multiplication (VMM). Efficient charge storage and weighting in array-based analog computing are achieved through the use of capacitive reactive elements or other charge-based linear weighting elements such as charge-coupled devices (CCDs) and charge-injection devices (CID). Their efficiency stems from inherent charge conservation throughout the computational cycle.

Charge injection device (CID) arrays store each bit of the matrix element in a DRAM storage element. The charge for each bit in a weight is stored in one of two locations. If the input bit that is multiplying the weight bit is 1, the charge is non-destructively shifted between locations during readout causing a charge to be capacitively induced on the bit line. The charge induced by multiple weights can be summed and sensed allowing the entire matrix to be read out in a single operation. Multi-bit inputs are processed serially. Furthermore, charge is recycled during the computation, and so adiabatic techniques can be used to further lower the energy (at the cost of speed).

Table BC5.1 Metrics for Analog Capacitive Vector-Matrix Multiply (VMM) ICs

High-density mixed-signal adiabatic processors[742,743,744] using CIDs have been developed using these principles. To optimize for resonant adiabatic energy recovery a stochastic encoding and decoding scheme can be used to ensure a constant capacitive load of the CID array. This has resulted in better than 1.1 TMACS/mW efficiency excluding on-chip digitization.[744]

Alternatively, several approaches have combined a capacitive charge based VMM with analog to digital conversion to maintain high overall system efficiencies. Many analog multiply-and-accumulate operations can be performed for each digitization. High precision implementations of capacitive charge based VMM have achieved low-pJ/MAC energy efficiencies,[745] while low-precision versions have achieved efficiencies at the level of 100 fJ/MAC.[746] Comparison of key metrics with the state-of-the-art in analog capacitive VMM ICs[747,748,749,750,745] is given in Table BC5.1 above.

5.2.1.2. OUTER PRODUCT UPDATE (OPU)

Analog resistive memory crossbars can also perform a parallel write or an outer product, rank 1 update where all the weights are incremented by the outer product of a vector applied to the rows and a different vector applied to the columns. This is a key kernel for many learning algorithms such as backpropagation[722] and sparse coding.[719,751] Row inputs are encoded in time and column inputs are encoded in either time[751] or voltage.[722]

When a VMM and MVM are combined on the same crossbar, extremely efficient learning accelerators can be designed,[720,752,753] with the potential to be 100–1000× more energy efficient and faster than an optimized digital ReRAM or SRAM based accelerator.[720]

The same figures of merit and design considerations for a VMM apply to the OPU. Additionally, the 1) write noise and 2) asymmetric write nonlinearity are important for determining how well a learning algorithm will perform. The 3) ability to withstand failures, and 4) endurance are also important for training systems. To have an efficient learning accelerator, parallel blind updates are needed where weights are updated without knowing the previous value and without verifying that the correct value is written. To obtain ideal accuracies, a low write noise is needed, less than 0.4% of the weight range. Even more important is having low asymmetries in the write process. The change in conductance for a positive pulse should be the same as that for a negative pulse for all starting states.[722] Often the conductance will saturate near a maximum where a positive pulse will not change the conductance, while a single negative pulse will cause a large decrease in conductance. This significantly lowers accuracy as it only takes a single negative write pulse to cancel many positive pulses.

Several devices have been examined for neural network training, including phase change memory,[752] resistive memory[720,754] and novel lithium-based devices.[730,731] Currently no devices meet all the ideal requirements for training (high resistance >10 MΩ, low write noise <0.4%, low write asymmetry[722]). Nevertheless, algorithmic approaches such as periodic carry,[755] Local Gains,[756] or the inclusion of semi-volatile capacitor-on-gate devices[741] can be used to help compensate and achieve ideal accuracies. Several co-design tools have been developed to model the impact of device level properties on algorithmic performance[752,757,758] which have allowed for the algorithmic development needed. Additionally, lower resistance devices can be used to give smaller near-term gains in performance.

The need for high on-state resistance and good analog characteristics means that filamentary resistive memories may not work as well as non-filamentary devices. A resistance higher than a quantum of conductance, 13 kΩ, requires current to tunnel through a barrier. This presents a fundamental problem for a filamentary device: a single atom can halve that tunneling barrier, resulting in huge variability and poor analog characteristics.

5.2.1.3. LARGE-SCALE FIELD PROGRAMMABLE ANALOG ARRAYS (FPAAS)

A field programmable analog array has configurable analog blocks and configurable interconnects between those blocks.[759,760,761] FPAAs allow users to build analog applications without having expertise in IC design. The fundamental breakthrough was recognizing that a switch matrix of single floating gate elements could be used for analog computation. The routing crossbar networks were, in fact, crossbar networks that could support VMM computation as well as a number of other computations.[762] Routing was no longer dead weight, as perceived for FPGA architectures. The floating gate cells could also allow for mismatch calibration at the mismatch source.[763,764] The density for VMM in FPAA architectures is nearly the level of custom IC design. These analog computations can be made robust to temperature fluctuations.[765] These techniques have been utilized by a number of students in university courses.[766,767] FPAA based VMMs can be scaled to small geometry (*e.g.* 40 nm and smaller) and operated at RF frequencies.[768,769]

5.2.1.4. RESISTIVE MEMORY CROSSBAR SOLVER

Resistive memory crossbars can be used to solve matrix problems, $Ax = b$ for x as illustrated in Figure BC5.2.[770] Each resistive memory is a programmable resistor that represents a matrix element in A. (Alternatively, any programmable analog element can also be used.) The equation $Ax = b$ can be mapped to Ohm's law, $\sum G_{ij}(V_j - V_i) = I_i$. The V_i are set to zero by an op-amp. Currents, I_i, are applied to the crossbar and the resulting voltages, V_j, are measured. The op-amps provide feedback allowing the V_j to be determined.

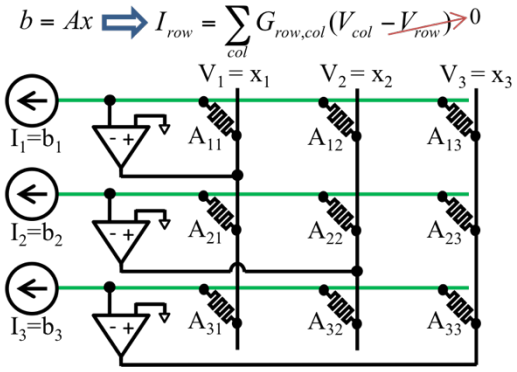


Figure BC5.2 A Resistive Memory Crossbar $Ax = b$ Solver is Illustrated

Note: The op-amps are used to provide feedback to find the solution and force the row voltages to zero.

The biggest challenge in taking advantage of analog solvers for HPC is that analog operations only offer low precision, ~8 bits fixed point, while HPC applications often demand 32 or more bits of floating point precision. This can be potentially overcome by hybrid analog/digital systems where the computationally intense parts of a calculation can be done in analog, while the required precision can be achieved by refining the solution in digital using a method with lower computational complexity[771]. This allows for some digital computation, while still getting a reduction in the overall computational complexity. The precision can potentially be improved by using iterative refinement or by using the crossbar to initialize a digital solver. The analog solution can also be used as a preconditioner within a Krylov method like CG or GMRES. Large matrices can be broken down into smaller blocks compatible with the accelerator and scaling can be used to compensate for finite on/off ranges. Work is still needed to show how noisy crossbar solvers can be used with ill-conditioned matrices. In general, iterative refinement will only converge if the noise is less than $1/\kappa$ where κ is the condition number of a matrix.

5.2.1.5. TERNARY CONTENT ADDRESSABLE MEMORY (TCAM)

Content-addressable memory (CAM), or associative memory, compares input search data against a table of stored data and returns the address of matching data. Ternary CAM (TCAM) allows for partial matches or "don't care" values. Conventional TCAM cells require multiple transistors per cell, resulting in a low-density, high cost cell, which could only be used in applications where speed is critical. Resistive memory crossbars can be used to build a high density TCAM that do not require any transistors per memory cell.[772,773,774]

The TCAM array accesses the entire memory in parallel, similar to an MVM, allowing for extremely efficient search operations. To realize a TCAM the resistive memories must be able to reliably switch between two different resistance states that differ by at least three orders of magnitude. Second, to maintain competitive energy dissipation, the resistive memories should have a high resistance >500 kΩ. The higher the ON/OFF ratio and the higher the resistance, the larger the array that can be built. A key challenge in the practical realization of TCAM arrays is the need for highly reliable devices and/or error correction that is compatible with a TCAM array.

5.2.2. NEURAL COMPUTING

Broadly speaking, neural (or neuromorphic or neural-inspired) computing models consist of a network of localized elements or "neurons," and connections or "synapses." As discussed in §5.2.1, analog crossbars can be used as building blocks for conventional neural networks to give significant improvements in energy, latency and area over digital accelerators. For accelerators specialized to a particular algorithm, various analog neurons can be used to process the crossbar outputs and avoid the need for and high cost of analog to digital conversion.

There is also a lot of work on more biologically inspired neural hardware. For biologically inspired neurons, connections are often designed to be persistent on short timescales, but (depending on the model) may exhibit mutability/plasticity in their strength and/or topology on longer timescales to facilitate, for example, adaptive in-situ learning. Connections between neurons can be modeled as discrete events or spikes (often implemented using an address event representation) or continuous-valued analog signals such as voltage or current. A key challenge for more biologically inspired architectures is the need for algorithmic co-design. For many neuro-inspired computational models, further research is needed to demonstrate state of the art machine-learning performance.

5.2.2.1. ANALOG NEURON FUNCTIONAL BLOCK

Depending on the algorithm being accelerated, analog neurons can accelerate a variety of functions such as:

1. spatial and temporal integration of input signals
2. stochastic firing of an action potential after a threshold is reached
3. relaxation to the resting potential if the time delay between excitations is too long.[775,776,777]
4. Non-linear activation functions. In many neural networks, after a linear multiply accumulate is performed on a set of inputs, or in a hidden layer, a non-linear activation or transfer function is applied. The presence of this function prevents the network from mathematically collapsing into a single linear equation, which helps improve the computational capabilities as the number of layers increases. Common functions include sigmoid, tanh and rectified linear (ReLu). In an analog network it is desirable that this function be performed by a single device.

These analog blocks are often with other building blocks such as crossbars, §5.2.1, to accelerate neural networks, to build dynamical systems, §5.2.3, create energy minimization circuits, §5.2.4 and enable probabilistic circuits, §5.3. Stochastic neurons/devices are discussed in §5.3 rather than here. Using an analog neuron allows analog data to be processed directly, obviating the need for time- and energy-consuming ADC/DAC in the circuits.

Recently, Mott memristors,[778] phase change based memristive switches,[779] and chalcogenide threshold switches[780] have all been reported to be capable of performing temporal voltage signal integration in which the effects of non-simultaneous unitary postsynaptic potentials add in time. Device candidates to perform the transfer function include STT-MRAM.[781]

Ionic diffusion dynamics or electrical instabilities enable a single memristive device to perform analog functions like resistance tuning or pulse generation after accumulating input,[779,782] which typically requires a large number of CMOS transistors. These analog functions are critical in emulating synaptic and neuronal behavior. Taking into account the simple structure and scalability of a two terminal memristor, both the complexity of a circuit and the area consumed to build a neuron network will be much less compared to a CMOS circuit. Being a passive device, the memristor offers stimulation dependent electric conductance. However, the passive nature results in a lack of power to maintain sustainable neural signal propagation in a network if passive synaptic blocks are employed. Additional power sources are mandatory for neural networks with multiple layers.

The benchmarks used to evaluate electronic spiking neurons generally measure the energy per operation, the fabrication cost, or the chip area of the integrated functional block, and the fidelity to the desired neuron function (e.g. integrate and fire). High reliability and low variation of devices are two key factors for the viability of a neuron technology. Device failure will cost a lot more circuitry for error detection and correction.[783] Large variation increases the difficulty for designing peripheral circuits and degrades the adaptability of the block.

To achieve unsupervised learning in a network, particularly those based on spike-timing-dependent plasticity, neuron blocks should be capable of programming the synaptic blocks. A key design challenge will be engineering the forward and back-propagating action potentials from the analog neuron blocks to potentiate or depress synapses for real time and *in situ* learning.

5.2.2.2. CELLULAR NEURAL NETWORK

The cellular neural network (CeNN) is a non-Boolean computing architecture that contains an array of computing cells that are connected to nearby cells. Since interconnects are major limitations in modern VLSI systems, CeNN systems take advantage of the local communication and encounter fewer constraints imposed by interconnects. The CeNN is a brain-inspired computing architecture that relies on neurons to integrate the incoming currents. The accumulated and activated output signal drives nearby neurons through weighted synapses. CeNNs can be used to create associative memories for voice and image recognition.

CMOS based CeNNs can be implemented by analog circuits using operational amplifiers and operational transconductance amplifiers (OTAs) as neurons and synapses, respectively.[784,785] Some recent work has also investigated CeNN using beyond-CMOS charge-based devices, such as TFETs, to potentially improve energy efficiency[786,787] thanks to their steep subthreshold slope and low operating voltage.

Using novel devices whose dynamics match the dynamics state of cells in CeNN can be far more efficient than op-amp and OTA based CeNNs. For instance, magnet switching dynamics that follow the Landau-Lifshitz-Gilbert (LLG) equation with a spin-transfer-torque term[788,789] are quite similar to the cell dynamics in CeNN. CeNNs have been designed based on spin diffusion using all-spin logic (ASL) with PMA magnets as the basic building block.[790] A CeNN cell can also be implemented by using MTJs as synapses and using spin Hall effect or domain wall propagation based devices as the neuron.[791] In all these cases, the read-out circuit consists of read and reference MTJs and an inverter that amplifies the voltage division between the two MTJs.

The associative memory application is widely used in the tasks of voice and image recognition, which can be efficiently performed in the CeNN architecture.[792,793] Five numbers, '1' – '5', are associated with the other five numbers, '6' – '0'. Hebbian learning is used for storing patterns.[794] Patterns with noisy input pixels can still be recalled. The delay per CeNN operation is dependent on the input pattern, input noise, and thermal noise.

In Fig. BC5.3, CeNN architectures based on the following devices are benchmarked: ferroelectric negative capacitance FET (NCFET),[795,796] tunneling FET (TFET),[797,798,799,800] piezoelectric FET (PiezoFET),[801] graphene pn junction switch (GpnJ),[802] various FETs based on two-dimensional materials,[803,804] all-spin logic (ASL),[805] charge-coupled spin logic (CSL),[806] and domain wall logic (mLogic).[807] In addition, the benefit of adding an extra layer of the copper plate between the SHE material and the free magnet is investigated to enhance spin injection through lateral diffusion.[808]

Fig. BC5.3 shows the performance comparison among three types of CeNN implementations using 4-bit weight synapses to achieve 90% recall accuracy for a given input noise of 10%. For the charge-based CeNN implementation, CMOS HP and LV devices are employed to quantify the performance of the digital CeNN and to compare against their analog counterparts. It is shown that the digital CeNNs are quite power hungry and slow. This is because multiple cycles are required to read out the weights from the register and perform the summation in the adder, which is energy and time consuming. In general, the analog CeNNs implemented by TFETs dissipate less energy thanks to their steep subthreshold slope and lower supply voltage. For optimal circuit-level performance, the preferred device properties for charge-based devices are steep threshold swing, large bias current, low supply voltage, and low capacitance.

In contrast to Boolean circuits, spintronic devices are more competitive compared to charge-based devices. This is because a single magnet can mimic the functionality of a neuron, and these spintronic devices operate at a low supply voltage. The domain wall device provides the best performance, in terms of Energy-Delay Product, thanks to its low critical current requirement. The spin diffusion based CeNN with IMA magnets consumes more energy due to the large critical current required to switch the magnet. For optimal circuit-level performance using spintronic devices, several properties are desired including: MTJs with a large TMR and a moderate resistance-area product, large spin injection coefficient β, large perpendicular anisotropy Ku for PMA magnets, large spin Hall angle θ for SHE materials, and small critical depinning current for domain wall magnets.

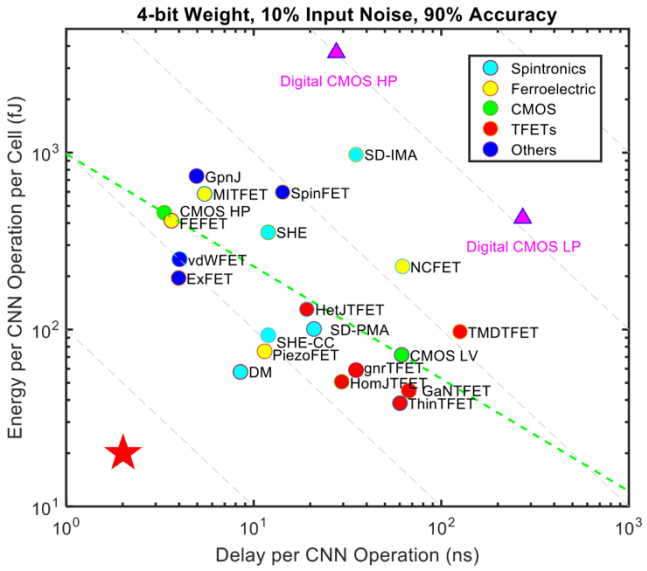


Figure BC5.3 Comparison of Energy and Delay per Operation Among Various Beyond-CMOS Technologies for CeNN Based on Analog, Digital, and Spintronic Implementations

Note: For the text labels, SD, SHE, and DW stand for spin diffusion, spin Hall effect, and domain wall motion, respectively, and CC represents the copper collector.

5.2.3. COMPUTING WITH DYNAMICAL SYSTEMS

In computing with dynamical systems, the built-in dynamical behavior of a physical system exhibiting continuous degrees of freedom is used to compute. The entire computational process can be analog, with only the results being digitized. The following subsections give a few examples of different types of dynamical systems-based approaches.

5.2.3.1. COMPUTING WITH COUPLED OSCILLATORS

A popular class of computing models utilizing continuous-time dynamical systems are the *coupled oscillator models*.

5.2.3.1.1. DEVICE TECHNOLOGIES FOR COUPLED OSCILLATOR SYSTEMS

It is challenging to build compact, low-power oscillators that can also be coupled together to give predictable phase or frequency dynamics. Standard digital ring oscillators based on CMOS inverter feedback loops, as well as the typical transistor-driven LC oscillators used in RF designs, are both less than ideal, due to device nonlinearities in the digital regime and the high biasing currents used in linear-regime analog small-signal oscillators, as well as relatively large oscillator sizes in both cases. Thus, various "Beyond CMOS" oscillator technologies have been explored. Such technologies can use and manipulate the charge, spin, or quantum properties of electrons, or use photons. Important examples include spin-torque,[809,810,811] insulator-metal-transition,[812] optical,[813,814] and quantum.[815] Memristor based oscillators have also been constructed.[816,817,818]

Non-silicon electrical oscillators include two important kinds which are currently being developed. One prominent effort is the use of spin torque oscillators (STOs) coupled with using spin diffusion currents, or electrical signals, for providing a computational platform for machine learning, spiking neural networks, and others.[809,810,811,813,819,820,821] However, the high current densities of STOs and the limited range of spin diffusion currents continue to pose serious challenges in creating coupled networks of such oscillators. Optical oscillators have been studied[814, 822] and used for computing,[813] but challenges include bulky components, difficult interfacing between the electrical and optical domains, and lack of programmability to enable an optical computing apparatus. Another promising non-silicon technology for very compact oscillators is the IMT (insulator-metal transition) material-based oscillator technology.[823,824] As the oscillation mechanism is completely electrical, the coupling of oscillators can be done easily using electrical components. There have been other implementation efforts for electrical oscillators[825,826,827,828,829] but the focus has been to build high frequency and low power individual oscillators, as opposed to the demonstration of coupled systems of oscillators, or the generation of interesting dynamics for computing. A comparison of some computing-focused electrical oscillators is shown in Table BC5.2 below:

Table BC5.2 Comparison of Some Electrical Oscillators for Computing

5.2.3.1.2. THEORETICAL MODELS OF COUPLED OSCILLATOR SYSTEMS

Coupled oscillator models can explain many natural, chemical and biological synchronization phenomena like the synchronized flashing of fireflies, pacemaker cells in the human heart, chemical oscillations, neural oscillations, and laser arrays, to name a few.[830] The simplest theoretical models of oscillators start with sinusoidal oscillators which have been extensively studied,[831,832,833] and their application in the computational paradigm has been well demonstrated.[834,835] A generalized description of oscillators in these models is usually a canonical phase model,[830,836] where the coupling mechanisms are generally assumed to be weak and composed of simple periodic functions which explicitly depend on phases. This model calls for simple harmonic oscillators with coupling that is assumed to affect each other's phases linearly. If the oscillators with phases θ_1 and θ_2 have frequencies ω_1 and ω_2, then in Kuramoto models the coupling of two oscillators will result in the phase equations:

$$\dot{\theta}_1 = \omega_1 + k(\theta_1 - \theta_2)$$
$$\dot{\theta}_2 = \omega_2 + k(\theta_2 - \theta_1)$$

where k is the coupling constant. A *Kuramoto* system of N oscillators is described by

$$\dot{\theta}_i = \dot{\omega}_i + \frac{K}{N}\sum_{j=1}^{N} \sin(\theta_j - \theta_i), \quad i = 1, \ldots, N$$

where θ_i and ω_i are the phase and frequency respectively of the i^{th} oscillator. Several studies on more general periodic coupling functions have also been studied.[837]

Along with sinusoidal oscillators, non-linear Van der Pol oscillators[838] and several of its variants, like the Morris-lecar neuron model,[839] have also been studied, and the applicability of such models in neurobiological and chemical oscillators has been demonstrated.[840,841,842] A single Van der Pol oscillator is defined by adding a non-linearity in the simple harmonic oscillator model

$$u'' + \epsilon(u^2 - 1)u' + u = 0$$

which results in relaxation behavior. Hence these are also called *relaxation* type oscillators. These analyses also assume non-realistic coupling dynamics like weak or pulse coupling, and do not focus on engineering aspects of building such coupled oscillators.

Such analytic models of coupled oscillatory systems almost always require a canonical phase description of the oscillators and a periodic phase dependent additive coupling that can be classified as weak. Strong coupling for relaxation type oscillators built using electrical circuits lack good explanations. Some theoretical studies have focused on pulse coupling,[843,844,845] and injection locking,[846,847] but these models are not suitable for understanding coupled relaxation oscillators that are based on repeated charging and discharging of a capacitor.[848, 849,850] These oscillators show piecewise linear dynamics instead of continuous dynamics as in the previous models, and the analysis of coupling is rather difficult as the limit cycle spans different "pieces" of the dynamics.

5.2.3.1.3. Computing Models Using Coupled Oscillators

Computing models using coupled oscillators can be categorized into pairwise coupling and multi-oscillator coupling. Pairwise coupling, *i.e.* coupling of just two oscillators, has simpler dynamics and hence can be used for simple operations like analog subtraction in a discriminant circuit.[851] Multi-oscillator coupling can be used for computing complex operations. Coupled oscillator based associative memories[835,852,853] have been proposed, where the dynamics can retrieve stored patterns and the steady state corresponds to the memorized pattern closest to the input, but successful implementations have yet to come. Another important application for combinatorial optimization, specifically graph coloring, was described[849] and developed theoretically with support from experimental demonstrations using relaxation oscillators based on phase-change IMT materials. Another model using multi-oscillator coupling is the Ising Machine; an implementation of this model using Optical Parametric Oscillators (OPO) was shown.[813]

5.2.3.2. Sub kT Computing Using Chaotic Logic

Shannon's noisy channel coding theorem[854] shows that one can reliably communicate information on a channel subject to noise (at a sufficiently low bitrate) even when the transmitted signal power is below the noise floor (*i.e.*, at a signal-to-noise ratio of less than 1). Moreover, any computational process can be viewed as just a special case of a communication channel, namely, one that simply happens to transform the encoded data in transit—since the derivation of Shannon's theorem relies solely on counting distinguishable signals, and nothing about how the signals are being counted in Shannon's argument precludes the encoded data from being transformed as it passes through the channel. This observation suggests that performing reliable computation utilizing signal energies (that is, energies associated with the dynamical variables in the system) at average levels $\ll kT$ (*i.e.*, well below the thermal noise floor) should theoretically also be possible—although the output bit rate (per unit signal bandwidth) will scale down with the average signal energy.

In 2016, Frank and DeBenedictis investigated a theoretical approach for implementing digital computation using chaotic dynamical systems[855,856,857] which provided evidence that the above theoretical observation is correct. In that approach, the long-term average value of a chaotically evolving dynamical degree of freedom encodes a digital bit. The interactions between degrees of freedom are tailored such that the bit-values represented by different degrees of freedom correspond to the results that would be computed in an ordinary Boolean circuit. This method can also be considered an example of the more general category of analog energy-minimization-based approaches (§5.2.3.3 and §5.2.4.2). However, this method does not require cooling the system to low noise temperatures, as is frequently done in energy-minimization approaches. Instead, the dynamical network uses a variation on adiabatic/reversible computing principles (§5.4) to adiabatically cause the system to transition between different warm, chaotic "strange attractors" that represent different computational states reversibly, without energy loss. The dynamical energy of the signal variables is itself conserved within the (Hamiltonian) dynamical system, and so the total energy dissipated per result computed can approach zero in this model as the rate of transformation decreases.

One disadvantage of the particular approach explored in that work is that it exhibits an apparent exponential increase in the real time required for convergence of the results as the complexity of the computation (number of logic gates) increases. However, as far as is known at this time, it is possible that faster variations on this or similar techniques may be found with further investigation.

5.2.3.3. Other dynamical systems for computing

Apart from coupled oscillators and chaotic logic, a number of other dynamical system models have been studied for various applications, but few have been implemented in some kind of hardware with proven advantages over corresponding digital

implementations of algorithms. Hopfield networks are attractor networks proposed for associative memories[858] where the fixed points (or stable states) of the system correspond to memories, and the dynamics of the network is such that the system settles to the fixed point which is closest to the initial state the system starts from. Hopfield style models have also been used for optimization.[859]

Cellular neural networks[860] (addressed in more depth in §5.2.2.2 above) consist of interconnected nodes where each node has linear or non-linear dynamics and the connections specify the coupling between their corresponding differential equations. Their CMOS implementations have been proposed with applications like pattern matching. Ising Machine[813,861,862] models have been proposed based on coupled spin glasses. The energy minima of such networks correspond to the solutions of an NP-hard combinatorial optimization problem and hence can model other NP-hard problems as well.[861] Another dynamical system for constraint satisfaction[863] is built on similar principles. An architecture based on non-repeating phase relations[864] between fabricated CMOS oscillators tries to emulate stochastic local search (SLS) for constraint satisfaction problems. An interesting approach based on memory co-processors was introduced as Memcomputing.[865] Interesting insights can also be obtained by looking into dynamical systems like iterated maps,[866] cellular automata,[867,868,869] and 0-1 continuous reformulations of discrete optimization problems.[870]

Although some of the above-mentioned methods target NP-hard problems, it's important to note that, to date, no general physical computing method (including analog and quantum approaches) has yet been clearly demonstrated to be capable of solving NP-hard problems without requiring exponential physical resources (energy and/or time) to be invested in the physical process performing the computation. The prevailing belief among computational complexity theorists[871] is that solving NP-hard problems efficiently would require uncovering new physics (*i.e.*, beyond standard quantum mechanics).

5.2.4. ANALOG ARCHITECTURE & ENERGY MINIMIZATION

Table BC5.3 Some Useful Analog Computing Design Patterns

In the past, IRDS principally roadmapped digital logic and memory, but the expansion to analog involves moving beyond the digital design paradigm. Digital systems comprise gates and DRAM that use analog devices internally yet create a digital interface to wiring. A wiring network then defines an architecture, possibly hierarchical, that is largely independent of the analog properties of the wires.

The digital design paradigm can be adapted to analog, but the resulting design paradigm is more complex. An analog system has a variety of signal types, such as voltage, current, or frequency, that are transported over the wiring. Modules based on nanodevices may be passive or too small to include a powerful signal drive, often making the analog properties of the wire an important part of the circuit's behavior.

General properties of computing systems have been studied with results such as Landauer's implementation-independent minimum energy dissipation for irreversible digital operations.[872] However, "analog" and "digital" are both implementation approaches for computing systems, so one may expect that there should be an equivalent to Landauer's minimum energy for irreversible *analog* systems—and indeed, at least in some cases, there is,[873] but such analog limits are not as well known.

5.2.4.1. BUILDING BLOCKS OF ANALOG SYSTEMS

The analog systems of interest today can be expressed as the hierarchical composition of a set of building blocks, just like digital electronics and software. There is no universally accepted set of building blocks at the moment, but Table BC5.3 (above) lists some commonly-encountered analog building blocks or design patterns that can be seen to apply to many of the analog architecture concepts discussed in this section.

5.2.4.2. ENERGY MINIMIZATION FOR THE TRAVELING SALESMAN PROBLEM

Some principles of analog system design will now be illustrated using a system that solves the Traveling Salesman Problem.

The Traveling Salesman Problem is to find the best route for a salesman that needs to visit a series of cities, each pair separated by some distance. The salesman seeks the shortest route that visits each city exactly once and then returns to the starting city. Exact solutions to this problem are known in computational complexity theory to be NP-hard, meaning that it is too hard for any computer, analog or digital, to solve exactly, in general, and at large scale. However, there are many ways to compute approximate solutions, meaning finding a short route but not necessarily the shortest route.

An example solution uses energy minimization using multiple runs on a Hopfield network. A Hopfield network is essentially one of the popular neural network arrays with its outputs fed back to its inputs. The synapse weights define an energy landscape based on binary values emerging from the neurons. If a Hopfield network is initialized or driven to a particular combination neuron values and then the drive is removed, the network will follow a trajectory that will take it to a minimum, or local minimum, of the energy landscape.

To use a Hopfield network for the Traveling Salesman Problem, the synapse weights are set to encode the $n \times n$ intercity distances. The system drives the neurons to a starting point for the salesman's route and removes drive. The system will settle into a candidate salesman's route in an amount of time equal to a few time constants of the feedback loop.

The method described above may find the ideal solution or just a better but suboptimal solution. To improve the odds of finding the best solution, the circuit can include either a true random noise generator or a chaotic pseudo-random noise generator. Under control of an external digital computer, the Hopfield network is driven to a random starting point and released many times in a cycle. The randomness causes many of the starting points to be different, making it more likely that the system will find the global minimum. The digital computer collects all the results, checking each to see which is best.

Such a system leverages multiple new circuit blocks including both a crossbar to encode the $n \times n$ intercity distances, an analog neuron to run the Hopfield network and either a chaos or noise generator to get randomness. As the Traveling Salesman problem is NP-hard, no solution method can solve it exactly at scale. Nevertheless, the analog solution seems to be at least comparable in efficiency with some software algorithms. It is also one of the more sophisticated analog computing examples, including all the aspects from Table BC5.3.

5.2.5. ANALOG COMPUTING—CLOSING REMARKS

Analog computation, as surveyed above, presents us with an intriguing and varied array of options for transcending the limitations that apply to the present-day digital approaches to computing. However, more work is needed to better characterize the range of applications for which analog computation can provide significant advantages over digital.

Enormously complex digital information-processing systems have been constructed by leveraging hardware description languages and programming languages that enable encapsulation, composability, and hierarchical design. In order to enable complex analog systems, more flexible, powerful languages (graphical and/or textual) for representing general classes of analog circuits and architectures are needed, to allow for a similar "modular" design approach.

Even the most advanced and sophisticated analog computational structures reviewed above in this section are only just the beginning. It appears that analog computing represents a vast field of future study, one that would likely benefit from a much more intensive level of exploration than it has received to date.

5.3. PROBABILISTIC CIRCUITS

Traditionally, conventional computational processes are designed to be deterministic, with computational results determined by the machine's initial state and inputs. Nevertheless, computations that are *intentionally* designed to behave randomly or stochastically, even at the level of individual bit-operations, are of interest and can have many useful applications such as simulated annealing, Monte Carlo simulation, machine learning or Boltzmann machines, randomized algorithms[874] as studied in computational complexity theory, and cryptographically secure random number generation for generating secure private keys. Noise in biological neurons is beneficial for information processing in nonlinear systems, and is essential for computation and learning in cortical microcircuits.[875,876,877,878]

Obtaining randomness in traditional CMOS is difficult and typically relies on a pseudo-random number generator. This requires a large circuit block and significant computational effort to obtain high quality random numbers. Several new devices have been proposed to obtain true randomness as discussed in §5.3.1. These allow for a random bit to be generated with a single device. Chaotic devices can be used to turn poor quality randomness into high quality random numbers. New architectures such as probabilistic p-logic (§5.3.2) or a travelling salesman solver (§5.2.4.2) can be designed using the new true random number generators.

5.3.1. DEVICE TECHNOLOGIES FOR RANDOM BIT GENERATION

New devices based on memristors, avalanche breakdown, and magnetic tunnel junctions and other technologies have been proposed for generating random bits. A key enabling functionality for some architectures like probabilistic (p)-logic is the ability to tuneably control the probability of a zero or one based on an input current or voltage. Several proposed devices are listed below. (See also §4.1.3.)

Magnetic Tunnel Junctions (MTJ): Existing Embedded MRAM technology can be used to create a tuneable random bit, provided that the Magnetic Tunnel Junctions are engineered to be thermally unstable. Such thermally unstable magnets have been experimentally observed. As MTJ dimensions are scaled, keeping them thermally stable becomes a hard challenge for memories, therefore destabilizing them in a controllable manner should be feasible in current technology.

Low-barrier MTJs can convert ambient thermal noise on nanomagnets into a fluctuating resistance, which is then used to build a device with tunable randomness when integrated with minimal CMOS periphery. The fluctuating resistance change due to thermal magnetic noise in MTJs can be measured by Tunneling Magneto resistance (TMR). State-of-the-art TMR values range from upwards of 100% to 600% demonstrated by the Tohoku Group,[879] and commercial STT-MRAM devices

exhibit >100% TMR. A large TMR would enable a robust functional unit for controllable randomness. The theoretical limit for TMR in MgO-based MTJs has been reported[880] to be 1,000% and can presumably be larger. There is currently intense research activity in half-metallic ferromagnets to increase TMR.

Single-Electron Bipolar Avalanche Transistor (SEBAT): The single-electron bipolar avalanche transistor (SEBAT) is a novel Geiger-mode avalanche bipolar transistor structure.[881,882] The device generates Poisson-distributed digital output pulses at rates between 1kHz and 20MHz. The pulse rate is linearly proportional to the emitted current. A MOS transistor is also formed within the base region of the device, allowing for voltage control of the pulse rate. The device is fully compatible with low-voltage CMOS circuits and standard digital process steps.

Memristors/Resistive RAM: The intrinsic variability of memristive switching, particularly the switching delay time of memristors, can be a good source of stochasticity.[660,883,884] Such stochasticity originates from the ionic dynamics within the memristors.[885]

Contact-resistive random access memory (CRRAM): CRRAM can be used for random number generation.[660,673] A CRRAM device may be based on a layer of silicon dioxide that is sandwiched between two electrodes; the bottom electrode could simply be the drain of a CMOS transistor.[674] During operation, the current flowing in a filament channel will be (randomly) impacted by any electrons trapped in the insulating layer. If a high voltage is applied to a device, the current in the filament channel will be large and not impacted by trapped electrons. However, with the application of a lower voltage, the width of a filament will shrink, and the trapped electrons *will* (randomly) influence output current.

CMOS: There are different ways to obtain random number generators (RNG) in CMOS using different physical noise sources, one being "jitter" in ring oscillators.[886] These TRNGs can be tuned into tunable random number generators as required but require significant amounts of area when compared to single device alternatives.

5.3.2. PROBABILISTIC (P)- LOGIC

In a series of recent papers, Camsari and Datta proposed a device-to-systems framework for a probabilistic (*p*)-logic[887,888,889,890,891,892,893] introducing the concept of *p*-bits and *p*-circuits. The authors explored how *p*-bits can be enabled by existing technology and showed different applications of them including image recognition,[894] combinatorial optimization,[890] Bayesian inference[887] and an enhanced type of Boolean logic including "invertible" operation.[888,889]

The main function of a *p*-bit is to provide a *tunable* randomness at its output terminal controlled by an input terminal. The tunability of randomness allows a network of *p*-bits (*p*-circuits) to be able to get correlated with one another when appropriately connected. This enables the *p*-bits to behave as a *hardware* building block for a range of systems level applications. By externally fixing any of the bits in a *p*-circuit, the other bits will stochastically oscillate between values that are allowed by the circuit. This allows circuits to be operated in "reverse." For example, a *p*-circuit implemented as a standard digital multiplier can function as a divider (or factorizer) operating in "reverse" as a consequence of the input/output equivalence of *p*-circuits.[888] Such "invertible" units are envisioned as part of a larger system that can be used as efficient hardware accelerators for specific problems that may not come as naturally to standard CMOS.

5.4. REVERSIBLE COMPUTING

Besides analog computing (§5.2) and probabilistic computing (§5.3), a third dimension along which we may explore departures from the conventional computing paradigm, as illustrated in Fig. BC5.1, is *reversible computing*.[895] When a computation is *reversible* in this context, we mean that the lowest-level computational processes should be arranged to approach a condition of being both *logically reversible* and *thermodynamically reversible*. To say that a computation is *logically reversible* means that known or deterministically computed information is not discarded from the digital state of the machine and ejected to a randomizing thermal environment. To say that it approaches being *thermodynamically reversible* here means that the total increase in physical entropy incurred by the machine's operation per useful computational operation performed is extremely small, with the vision that it can be brought closer to zero asymptotically as the technology continues to be improved.

In 1961, Rolf Landauer of IBM argued[872] that there is a fundamental physical limit on the energy efficiency of conventional *irreversible* digital operations, meaning those that carry out a many-to-one transformation of the space of computational states that is used. Landauer's limit states that an amount $kT \ln 2$ of energy (where k is Boltzmann's constant and T is the temperature of the heat bath) must be (irreversibly) dissipated to heat per bit's worth of (known or correlated) information that is lost from the computational state. Landauer's argument can be rigorously derived from fundamental physical considerations.[896,897,898]

An important caveat is that Landauer's limit only applies to computational information that is correlated with other available information, as opposed to independent random information.[897,899] A computational bit that includes *no* correlations with other available bits is, in effect, *already* entropy, and thus it can be transferred back and forth between a stable, digital form in a computer and a rapidly-fluctuating physical form in a thermal environment with asymptotically zero net increase in total entropy, by, for example, adiabatically raising and lowering a potential energy barrier separating two degenerate states.

However, most bits in a digital computer are correlated bits, having been computed deterministically from other available bits. Performing a many-to-one transformation such as destructively overwriting or erasing such a bit *obliviously* (*i.e.*, without regards to its existing correlations) therefore increases total entropy by one bit's worth ($k \ln 2$) and thus implies at least $kT \ln 2$ energy consumption (decrease in free energy). Fundamentally, then, the only way to avoid Landauer's limit, in a deterministic computational process, is to avoid many-to-one transformations of the computational state. Bennett[900] showed that this is always possible; that is, any desired irreversible computation can always be embedded into an equivalent reversible one. Such an embedding generally appears to incur some algorithmic overheads,[901] but if reversible devices become cheaper and more energy-efficient over time, in principle, these resource overheads can be outweighed by the achievable energy savings. In the long run, reversible computing is the *only* physically possible path by which the amount of general digital computation that can be performed per unit energy and cost might continue to be increased indefinitely, without any known fundamental limit.

In typical adiabatic implementations of reversible computing in specific device technologies, there is frequently a linear device-level tradeoff between the energy dissipation and the time required to carry out a given primitive digital operation in the adiabatic limit. (*Energy dissipation*) × (*Time*) = *const*. However, there is no proof that this same tradeoff relation extends to all possible implementation technologies, and in fact, recent results suggest that an exponential downscaling of energy dissipation with delay may sometimes be possible when quantum effects are leveraged.[902] Further, even among cases where the relation applies, there are no known technology-independent lower bounds on the value of the energy-delay constant. Although there are indeed firm quantum lower limits on the product of energy *invested* times delay,[903] there are no known fundamental limits (greater than zero) on energy *dissipated* for a given delay value. Further, even given a fixed value of the constant, thermally limited parallel processors can still benefit from reversible computing in terms of their aggregate performance. For example, in cooling-limited stacked 3D logic scenarios, the per-area performance advantage of asymptotically adiabatic technologies increases with the square root of 3D processor thickness.[904] And in loosely-coupled, arbitrarily-massively parallelizable applications with fixed power budgets, the aggregate performance gain from reversible computing scales up with the energy efficiency, that is, arbitrarily.

Unfortunately, as of today, experimentally realizing reversible computing's promise to far exceed the system-level energy efficiency of all conventional computers remains an extremely difficult engineering challenge. Although a variety of different adiabatic[905,906,907,908,909,910,911,912,913,914,902] and ballistic[915,916,917,918,919,920,921,922,923,924,925] schemes for the realization of reversible logic have been proposed, it is challenging in practice to actually achieve large energy efficiency gains at the system level when accounting for a wide variety of real-world parasitic energy dissipation mechanisms that exist, which would all need to be systematically eliminated or reduced. There is not yet any "magic bullet" method that automatically addresses all of the many possible energy-loss mechanisms in a complete system at once. Logical reversibility (when suitably generalized[896]) is a *necessary* condition for approaching physical reversibility in deterministic digital computations, but by no means a *sufficient* one.

However, while approaching the ideal of physically reversible computing is by no means an *easy* path forward, it is at least *a* way to move forward. Potentially, even in CMOS, adiabatic circuits might be able to demonstrate useful energy efficiency gains for some applications even in the relatively near term if sufficiently high-*Q* resonators can be developed.[926] And in principle, even some of the existing reversible superconducting logic styles (such as RQFP[927,928,929,930,931,932] and nSQUID[933,934] logic) already appear to be capable of achieving energy dissipation below the Landauer limit in principle, although the available analyses of these logic styles do not yet account for energy dissipation associated with supplying the power-clock driving signals.

Reversible computing can also, potentially usefully, be combined with probabilistic computing (§5.3); if random digital bits are obtained by taking in entropy from the thermal environment and capturing it in a stable form, this can actually reduce environmental entropy (albeit without reducing total entropy, since the entropy of the digital state has then increased). Once a randomized reversible computation utilizing such bits of "true" entropy has completed, those random bits can later be returned to the thermal environment with no net thermodynamic cost.[897] Thus, the requirement for a nondeterministic computation to be thermodynamically reversible is somewhat looser than is the case for a deterministic computation; many-to-one (irreversible) transformations can be allowed together with one-to-many (nondeterministic) transformations in a computation,[935] as long as, overall over the course of the computation, previously-established correlations are not becoming lost.

Reversible computing is normally conceived of as a strategy for making *digital* computation more energy efficient. More generally, can a broad variety of *analog* computing schemes be developed that are also thermodynamically reversible? Record energy efficiencies for charge-based analog vector-matrix multiplication have been demonstrated using adiabatic principles as discussed in §5.2.1.1.2.[744] Further, fundamental physics is reversible at the microscale, which suggests that a sufficiently carefully-engineered analog computer might be made to approach macroscopic reversibility, and that its energy efficiency might be increased without limit as its technology is further refined. The degrees of freedom utilized for the analog physical computation would likely have to be very well-isolated from the system's thermal degrees of freedom, and the usual tendency for complex dynamical systems to devolve towards chaotic behavior would have to be suppressed in some way, or else made into a useful feature of the computational process. The previously mentioned work on chaotic logic (§5.2.3.2) suggests one potential technique

for harnessing the chaotic analog behavior of conservative dynamical systems usefully for computational purposes, but many other, more sophisticated methods may be possible.

5.5. Device-Architecture Interaction: Conclusions/Recommendations

In this section, we have surveyed a variety of concepts and R&D directions for the development of novel Beyond CMOS computing technologies that represent an effort to think "outside the box," in the sense of looking beyond just developing simple drop-in replacements for traditional logic and memory cells. More broadly, new hardware designs spanning multiple levels from the devices up through circuits and architectures must be considered, and the interactions between the various levels explored. More specifically, we expand the scope of future computing technologies beyond traditional irreversible, deterministic digital logic to include a broad range of alternative, unconventional computational paradigms, such as analog, probabilistic, and (classical) reversible computing paradigms. Quantum computing[707] is another paradigm that may become increasingly important for certain applications; it is being addressed in a new IRDS chapter (Cryogenic Electronics and Quantum Information Processing).

This section's focus on analog computing and, in particular, analog implementations of neural computational models that also facilitate efficiently performing complex computational functions such as matrix operations, reflects a set of presently popular research directions. Neural computing is an extremely "hot" area right now, due to the blossoming commercial success of neural computing techniques such as Deep Learning, Convolutional Neural Nets, and machine learning technologies. These techniques are widely used in analyzing and mining massive datasets in this present age of Big Data, and for developing "smart" IoT and mobile/wearable products.

Apart from analog/neural computing, the other alternative computing paradigms addressed in this section (probabilistic and reversible) may be covered more extensively in the future, to the extent that they prove necessary and useful for transcending the energy efficiency limits of deterministic, irreversible styles of computation (which includes many of the analog and neural styles). Of course, the broadest possible class of computational mechanisms consists of those that are not necessarily exclusively digital, deterministic, *or* irreversible (*i.e.*, the entirety of the Venn diagram in Figure BC5.1, including its exterior), and so certainly, the most efficient future machines will be found somewhere within that broadest class. However, at this time, the exact range of computational applications for which loosening each of these traditional constraints confers large benefits, as well as the exact extent of those benefits, remains very unclear, and will need to be proved out over time by ongoing R&D efforts.

Recommendations. In general, computing paradigms outside of the traditional irreversible, deterministic, digital paradigm are still very under-developed, compared to the conventional paradigm. This is not surprising, considering that the conventional paradigm historically facilitated the development of a design abstraction hierarchy that permitted enormously complex systems to be constructed. As a result, the complexity and efficiency of those systems increased exponentially as Moore's Law made the underlying devices cheaper and more efficient. However, Dennard scaling has now ended, the end of the CMOS roadmap appears to be in sight, with no clear successor having been identified, and fundamental thermodynamic limits are also coming into view. Thus, today there is an increasing level of interest in expanding the scope of our investigations to include unconventional computing paradigms that may transcend the limits of the traditional computing paradigm.

Analog computing offers many promising potential directions for technology development, some of which were outlined in §5.2, and it is likely that many other analog computing concepts also exist that are less well-developed at this time. Given the somewhat immature status today of analog computing technologies in general, it still seems too early in the game to "choose winners," in terms of specific analog technologies to focus exclusively on developing commercially. Thus, at this time, the ongoing exploration of an even broader range of alternatives at the research level may be called for. However, design hierarchy remains a useful concept even in the analog realm, so it seems likely that an extensive range of abstractions and reusable building blocks facilitating some (more or less) "general-purpose" style of analog computing, such as that envisioned in §5.2.4, which allows heterogeneously mixing analog computing primitives of various types, can be developed over time.

That being said, in the nearer term, it's quite possible that special-purpose analog accelerators for certain applications (such as the VMM and other matrix operations, and other neural-related applications addressed in §5.2.2) may appear commercially relatively soon, since that line of research has already progressed significantly towards applications, and the demand for these kinds of applications from the Big Data analytics and Machine Learning market sectors remains strong.

Beyond this, the other technologies addressed in this section (including the broad spectrum of analog computing technologies, as well as the probabilistic and reversible technologies) are mostly at a relatively low technology readiness level, and so major commercial applications for these are probably a bit further out. However, looking forwards, there should probably be an increased level of investment in terms of basic research and early-stage technology development in such areas. Neural computing is certainly extremely valuable right now, for a wide range of machine learning, data analytics, and pattern recognition applications, but it is still somewhat special purpose, compared to conventional computing, and so it is not necessarily directly highly beneficial for *all* computing applications of interest. In contrast, if, for example, reversible computing can be developed

successfully, including favorably engineered cost/performance tradeoffs,[936] it offers the potential to make *all* computing applications (including general-purpose digital computing) much more energy-efficient (and, ultimately, cost-efficient) than is possible in the conventional paradigm. Probabilistic logic may have its own broad range of applications as well. However, since these kinds of alternative technology directions are much less well-developed than the neural approach at present, they will require an increased level of long-horizon research investments in the near to medium term, if they are to make substantial progress towards realizing their promise by the time progress stalls in the presently more well-developed areas (conventional and neural computing).

Overall, the potential utility of new styles of "Beyond CMOS" computing that rethink computation — not just at the device level, but also in terms of the entire computing paradigm, with changes to the machine design also at the circuit level, the architecture level, and higher levels — is vast. It is our recommendation, based on the results of a 2017 workshop and our overall efforts in surveying this field, that these alternative computing styles deserve a greatly increasing level of attention and investment as the apparent end of the CMOS roadmap draws closer.

6. ASSESSMENT

6.1. INTRODUCTION

The purpose of this section is to assess beyond-CMOS memory and logic devices considered in this chapter benchmarked against current memory or CMOS technologies. Emerging architectures are not compared as each architecture often accelerates a different computational kernel. Assessments for individual architectures are given in the respective sections. Two methods of assessments were reported previously in the ITRS ERD chapter: a "quantitative emerging device benchmarking" conducted by research consortia, e.g., the Nanoelectronics Research Initiative (NRI), and a "survey-based assessment".

In the "quantitative emerging device benchmarking", each emerging device is evaluated by its operation in conventional Boolean Logic circuits, *e.g.*, a unity gain inverter, a 2-input NAND gate, and a 32-bit shift register. Metrics evaluated include speed, areal footprint, power dissipation, *etc*. Each parameter is compared with the performance projected for high performance and low power 5nm CMOS applications. This "beyond CMOS" chapter will update the quantitative benchmarking section with the latest NRI results.

Up to the 2013 ERD Chapter, a survey-based critical review was conducted based on eight criteria to compare emerging devices against their CMOS benchmark. Spider chart has been used to visualize the perceived potential of these technology entries. However, the limited number of survey results sometimes raises questions of the accuracy of this survey. The most recent "survey-based assessment" was conducted in the 2014 ERD Emerging Memory and Logic Device Assessment Workshops (Albuquerque, NM). The survey collects voting on emerging technologies evaluated in the workshops in the categories of the "most promising" and the "most need of resources" to assess the potential of these technology entries perceived by ERD experts. Although the survey-based assessment has not been conducted recently, a summary of previous assessments is included in this chapter for reference.

An important issue regarding emerging charge-based nanoelectronic switch elements is related to the fundamental limits to the scaling of these new devices, and how they compare with CMOS technology at its projected end of scaling. An analysis[937] concludes that the fundamental limit of scaling an electronic charge-based switch is only a factor of 3 times smaller than the physical gate length of a silicon MOSFET in 2024. Furthermore, the density of these switches is limited by a maximum allowable power dissipation of approximately 100W/cm^2, and not by their size. The conclusion of this work is that MOSFET technology scaled to its practical limit in terms of size and power density will asymptotically reach the theoretical limits of scaling for charge-based devices.

Most of the proposed beyond-CMOS devices are very different from their CMOS counterparts, and often pass computational state variables (or tokens) other than charge. Alternative state variables include collective or single spins, excitons, plasmons, photons, magnetic domains, qubits, and even material domains (*e.g.*, ferromagnetic). With the multiplicity of programs characterizing the physics of proposed new structures, it is necessary to find ways to benchmark the technologies effectively. This requires a combination of existing benchmarks used for CMOS and new benchmarks which take into account the idiosyncrasies of the new device behavior. Even more challenging is to extend this process to consider new circuits and architectures beyond the Boolean architecture used by CMOS today, which may enable these devices to complete transactions more effectively.

6.1.1. ARCHITECTURAL REQUIREMENTS FOR A COMPETITIVE LOGIC DEVICE

The circuit designer and architect depend on the logic switch to exhibit specific desired characteristics in order to insure successful realization of a wide range of applications. These characteristics,[938] which have since been supplemented in the literature, include:

- Inversion and flexibility (can form an infinite number of logic functions)
- Isolation (output does not affect input)
- Logic gain (output may drive more than one following gate and provides a high I_{on}/I_{off} ratio)
- Logical completeness (the device is capable of realizing any arbitrary logic function)
- Self restoring / stable (signal quality restored in each gate)
- Low cost manufacturability (acceptable process tolerance)
- Reliability (aging, wear-out, radiation immunity)
- Performance (transaction throughput improvement)
- Span of control (measures number of devices that may be reached within a characteristic delay of the switch[939])

Devices with intrinsic properties supporting the above features will be adopted more readily by the industry. Moreover, devices which enable architectures that address emerging concerns such as computational efficiency, complexity management, self-organized reliability and serviceability, and intrinsic cyber-security[940] are particularly valuable.

6.2. QUANTITATIVE EMERGING DEVICE BENCHMARKING

The Nanoelectronics Research Initiative (https://www.src.org/program/nri/) has been benchmarking several diverse beyond-CMOS technologies, trying to balance the need for quantitative metrics to assess a new device concept's potential with the need to allow device research to progress in new directions which might not lend themselves to existing metrics.[941, 942,943] Several of the more promising NRI devices have been described in detail in the Logic and Emerging Information Processing Device Section. Some results of this benchmark study were included in 2015 ITRS ERD chapter.

While all these efforts are still very much a work in progress – and no concrete decisions have been made on which devices should be chosen or eliminated as candidates for significantly extending or augmenting the roadmap as CMOS scaling slows – this section summarizes some of the data and insights gained from these studies. Further benchmarks may alter some of the conclusions here and the outlook on some of these devices, but the overall message on the challenge of finding a beyond CMOS device which can compete well across the full spectrum of benchmarks of interest remains.

6.2.1. QUANTITATIVE RESULTS

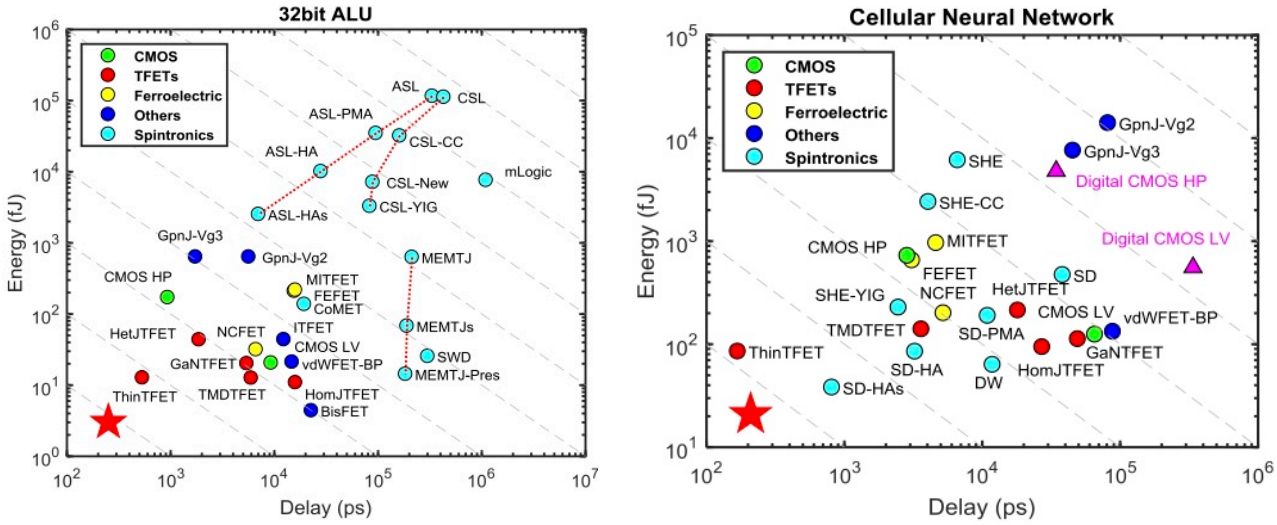
NRI benchmarking analyzes the potential of major emerging switches using a variety of information tokens and communication transport mechanisms. Specifically, the projected effectiveness of these devices used in a number of logic gate configurations was evaluated and normalized to CMOS at the 5nm generation (projection). The initial work has focused on "standard" Boolean logic architecture, since the CMOS equivalent is readily available for comparison. It should be noted that the majority of devices are evaluated via simulations since many of them have not yet been built, so it should be considered only a "snapshot in time" of the potential of any given device. Data on all of them are still evolving.

Device name	acronym	input(s)	control	int. state	output	material
Si MOSFET high perf.	CMOS HP	V	Vg	Q	V	silicon
Si MOSFET low voltage	CMOS LV	V	Vg	Q	V	InAs
van der Walls FET	vdWFET	V	Vg	Q	V	MoS_2
Homojunction III-V TFET	HomJTFET	V	Vg	R	V	InAs
Heterojunction III-V TFET	HetJTFET	V	Vg	R	V	GaSb/InAs
Graphene nanoribbon TFET	gnrFTET	V	Vg	R	V	graphene
Interlayer tunneling FET	ITFET	V	Vg	R	V	graphene
Two D Heterojunction Interlayer TFET	ThinFET	V	Vg	R	V	$WTe_2/SnSe_2$
GaN TFET	GaNFET	V	Vg	R	V	GaN
Transition Metal Dichalchogenide TFET	TMDTFET	V	Vg	R	V	WTe_2
Graphene pn-junction	GpnJ	V	Vg	R	V	graphene
Ferroelectric FET	FEFET	V	Vg	P	V	PZT
Negative capacitance FET	NCFET	V	Vg	P	V	PZT
Piezoelectric FET	PiezoFET	V	V	σ	V	AlN
Bilayer pseudospin FET	BisFET	V	Vg	BC	V	graphene
Excitonic FET	ExFET	V	Vg	BC	V	$MoS_2/MoSe_2$
Metal-insulator transistor	MITFET	V	Vg	Orb	V	$NdNiO_3$
SpinFET (Sughara-Tanaka)	SpinFET	V	Vg, Vm	Q, M	V	CoFeB
All-spin logic	ASL	M	V	M	M	CoPtCrB
Charge-spin logic	CSL	I	V	M	I	CoPtCrB
Spin torque domain wall	STT/DW	I	V	M	I	CoFeB
Spin majority gate	SMG	M	V	M	M	PMN-PT
Spin torque oscillator	STO	I	V	M	I	CoPtCrB
Spin wave device	SWD	M	I or V	M	M	PMN-PT
Nanomagnetic logic	NML	M	B or V	M	M	PMN-PT

Figure BC6.1 List of Devices Considered in NRI Benchmarking with Their Computational Variables and Classification[943]

At a high level, the data from these studies corroborates qualitative insights from earlier works, suggesting that many new logic switch structures may have some advantages over CMOS in terms of power or energy, but they are also inferior to CMOS in delay. This is perhaps not surprising; the primary goal for nanoelectronics and NRI is to find a lower power device[944] since power density is a primary concern for future CMOS scaling. The power-speed tradeoffs commonly observed in CMOS are also extended into the emerging devices. It is also important to understand the impact of transport delay for the different information tokens these devices employ. Communication with many non-charge tokens can be significantly slower than moving charge, although this may be balanced in some cases with lower energy for transport. The combination of the new balance between switch speed, switch area, and interconnect speed can lead to advantages in the span of control for a given technology. For some of the technologies (*e.g.*, nanomagnetic logic), there is no strong distinction between the switch and the interconnect, indicating the need for novel architecture to exploit unique attributes of these technologies. Figure BC6.1 lists the devices studied in the NRI benchmarking[943].

A simplified 32-bit arithmetic logic unit (ALU) was built from these devices to evaluate their performance and the result is summarized in Figure BC6.2(a) [945]. While tunneling devices (e.g., TFET) show limited advantages over CMOS in terms of energy-delay product, most beyond-CMOS devices are inferior to CMOS in energy and/or delay. For example, the majority of spintronic devices are slower than CMOS and also show no energy advantage.



(a) (b)

Figure BC6.2 (a) Energy versus Delay of a 32-bit ALU for a Variety of Charge- and Spin-based Devices; (b) Energy versus Delay per Memory Association Operation Using Cellular Neural Network (CNN) for a Variety of Charge- and Spin-based Devices[945]

At the architecture level, the ability to speculate on how these devices will perform is still in its infancy. While the ultimate goal is to compare at a very high level – *e.g.*, how many MIPS can be produced for 100 mW in 1 mm^2? – the current work must extrapolate from only very primitive gate structures. One initial attempt to start this process has been to look at the relative "logical effort"[946] for these technologies, a figure of merit that ties fundamental technology to a resulting logic transaction. Several of the devices appear to offer advantage over CMOS in logical effort, particular for more complex functions, which increases the urgency of doing more joint device-architecture co-design for these emerging technologies.

The direction of device-architecture co-optimization has driven NRI benchmarking to explore non-Boolean applications of beyond-CMOS devices. Cellular Neural Network (CNN) has been utilized as a benchmarking model that has been implemented with various novel devices.[945] The energy and delay of CNN based on beyond-CMOS devices are compared with CMOS-based CNN in Figure BC6.2(b). Tunneling devices have significant performance improvement because of their steep subthreshold slopes and large driving current at ultra-low supply voltage. Interestingly, spintronic devices are much closer to the preferred corner in CNN implementation in comparison with 32-bit ALU. This is because some characteristics of spintronic devices (e.g., spin diffusion, domain wall motion) may mimic the functionality of a neuron (e.g. integration) more naturally in a single device.

6.2.2. OBSERVATIONS

A number of common themes have emerged from these benchmark studies and in the observations made during recent studies of beyond-CMOS replacement switches[947]. A few noteworthy concepts:

1. The low voltage energy-delay tradeoff conundrum will continue to be a challenge for all devices. Getting to low voltage must remain a priority for achieving low power, but new approaches to getting throughput with 'slow' devices must be developed.
2. Most of the architectures that have been considered to date in the context of new devices utilize binary logic to implement von Neumann computing structures. In this area, CMOS implementations are difficult to supplant because they are very competitive across the spectrum of energy, delay and area – not surprising since these architectures have evolved over several decades to exploit the properties of CMOS most effectively. Novel electron-based devices – which can include devices that take advantage of collective and non-equilibrium effects – appear to be the best candidates as a drop-in replacement for CMOS for binary logic applications.
3. As the behavior of other emerging research devices becomes better understood, work on novel architectures that leverage these features will be increasingly important. A device that may not be competitive at doing a simple NAND function may have advantages in doing a complex adder or multiplier instead. Understanding the right building blocks for each device to maximize throughput of the system will be critical. This may be best accomplished by thinking about the high-level metric a system or core is designed to achieve (*e.g.*, computation, pattern recognition, FFT, *etc.*) and finding the best match between the device and circuit for maximizing this metric.
4. Increasing functional integration and on-chip switch count will continue to grow. To that end, in any logic architectural alternative, both flexible rich logic circuit libraries and reconfigurability will be required for new switch implementations.
5. Patterning, precision layer deposition, material purity, dopant placement, and alignment precision critical to CMOS will continue to be important in the realization of architectures using these new switches.
6. Assessment of novel architectures using new switches must also include the transport mechanism for the information tokens. Fundamental relationships connecting information generation with information communication spatially and temporally will dictate CMOS' successor.

Based on the current data and observations, it is clear that CMOS will remain the primary basis for IC chips for the coming years. While it is unlikely that any of the current emerging devices could entirely replace CMOS, several do seem to offer advantages, such as ultra-low power or nonvolatility, which could be utilized to augment CMOS or to enable better performance in specific application spaces. One potential area for entry is that of special purpose cores or accelerators that could off-load specific computations from the primary general purpose processor and provide overall improvement in system performance. If scaling slows in delivering the historically expected performance improvements in future generations, heterogeneous multi-core chips may be a more attractive option. These would include specific, custom-designed cores dedicated to accelerate high-value functions, such as accelerators already widely used today in CMOS (e.g. Encryption/Decryption, Compression/Decompression, Floating Point Units, Digital Signal Processors, etc.), as well as potentially new, higher-level functions (e.g. voice recognition). While integrating dissimilar technologies and materials is a big challenge, advances in packaging and 3D integration may make this more feasible over time, but the performance improvement would need to be large to balance this effort.

As a general rule, an accelerator is considered as an adjunct to the core processors if replacing its software implementation improves overall core processor throughput by approximately ten percent; an accelerator using a non-CMOS technology would likely need to offer an order of magnitude performance improvement relative to its CMOS implementation to be considered worthwhile. That is a high bar, but there may be instances where the unique characteristics of emerging devices, combined with a complementary architecture, could be used as an advantage in implementing a particular function. At the same time, the changing landscape of electronics (moving from uniform, general purpose computing devices to a spectrum of devices with varying purposes, power constraints, and environments spanning servers in data centers to smart phones to embedded sensors) and the changing landscape of workloads and processing needs (Big Data, unstructured information, real-time computing, 3D rich graphics) are increasing the need for new computing solutions. One of the primary goals then for future beyond-CMOS work should be to focus on specific emerging functions and optimize between the device and architecture to achieve solutions that can break through the current power/performance limits.

6.3. Survey-Based Benchmarking of Beyond CMOS Memory & Logic Technologies

Although survey-based emerging device assessment has not been continued after the 2015 ITRS ERD chapter, previous survey-based assessments in ERD chapters are summarized here for references.

6.3.1. Emerging Device Assessment in 2014 ERD Workshops

In August 2014, ERD organized an "Emerging Memory Device Assessment Workshop" and an "Emerging Logic Device Assessment Workshop", where nine memory devices and fourteen logic devices were evaluated. A survey was conducted in the workshops for the experts to vote on the "most promising" devices and devices "needing more resources". Figure BC6.3 shows

the relative number of votes received by emerging devices in these two categories, ranked from high to low in the "most promising" category (red color bars).

In the "most promising" memory device category, the vote clearly accumulated to a few well-known memory devices: STTRAM, ReRAM (including CBRAM and oxide-based ReRAM), and PCM, ranked from high to low. Some memory devices received few vote, due to lack of progress. Results in this category reflect consensus among experts based on R&D status of these devices. The "need more resources" category reflects perceived value of these devices in the view of the experts and also experts' consideration of R&D resource allocation based on existing investment (or lack of investment) for each device. For example, with heavy R&D investment on STTRAM that is considered most promising, it is not surprising that it ranks low in the need of resources. The strong interest in emerging FeFET memory is closely linked to the discovery of ferroelectricity in doped HfO_x. Among emerging logic devices, "carbon nanomaterial device" (mainly carbon nanotube FET), tunnel FET, and nanowire FET were ranked as one of the most promising emerging logic devices. Notice that they are all charge-based devices, but involve novel materials, structures, and mechanisms. "Piezotronic transistors", "negative-capacitance FET", and "2D channel FET" were considered top choices for enhanced research investment.

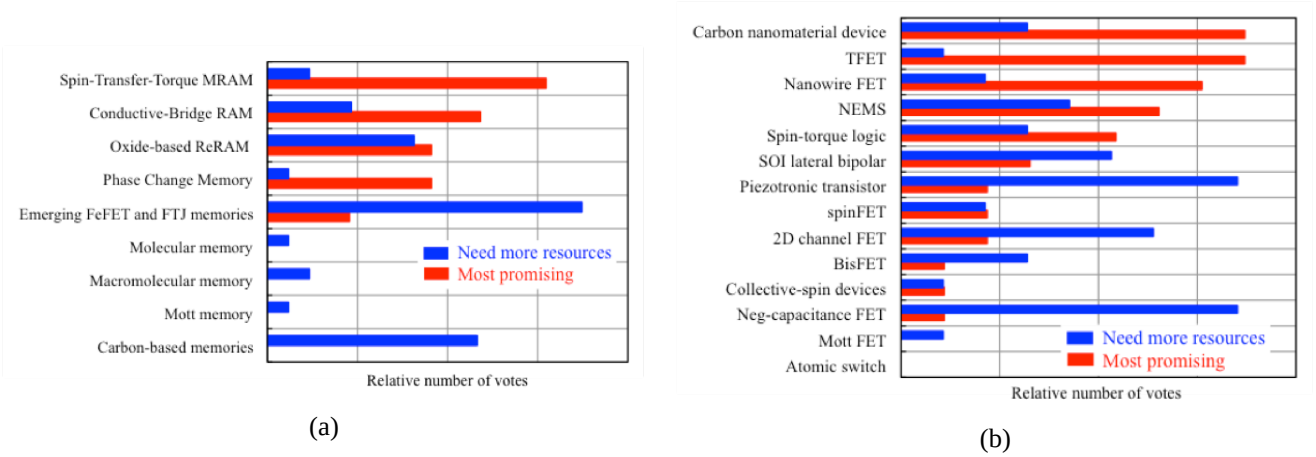


Figure BC6.3 (a) Survey of Emerging Memory Devices and (b) Survey of Emerging Logic Devices in 2014 ERD Emerging Logic Workshop (Albuquerque, NM)

6.3.2. ERD Survey Criteria, Methodology, and Results

In the traditional survey-based assessment conducted by ERD, a set of relevance or evaluation criteria, defined below, are used to parameterize the extent to which "CMOS Extension" and "Beyond CMOS" technologies are applicable to memory or information processing applications. The relevance criteria are: 1) Scalability, 2) Speed, 3) Energy Efficiency, 4) Gain (Logic) or ON/OFF Ratio (Memory), 5) Operational Reliability, 6) Operational Temperature, 7) CMOS Technological Compatibility, and 8) CMOS Architectural Compatibility. Description of each criterion can be found in 2013 ERD chapter.

Each CMOS extension and beyond-CMOS emerging memory and logic device technology is evaluated against these criteria according to a single factor. For logic, this factor relates to the *projected potential performance* of a nanoscale device technology, assuming its successful development to maturity, *compared to that for silicon CMOS scaled to the end of the Roadmap*. For memory, this factor relates the *projected potential performance* of each nanoscale memory device technology, assuming its successful development to maturity, *compared to that for ultimately scaled current silicon memory technology which the new memory would displace*. Performance potential for each criterion is assigned a value from 1–3, with "3" substantially exceeding ultimately-scaled CMOS, and "1" substantially inferior to CMOS or, again, a comparable existing memory technology. This evaluation is determined by a survey of the ERD Working Group members composed of individuals representing a broad range of technical backgrounds and expertise. Details of the assessment values are also included in 2013 ERD chapter.

Although this survey-based critical review has been conducted in ERD for several versions and has been widely cited in literatures, the decreasing number of votes of some less popular devices has raised concerns about the accuracy of some of the results. Figures BC6.4 and EBC6.5 summarize the last critical review conducted in 2013 for emerging memory devices and emerging logic devices, respectively. Notice that the technology entries in these figures are based on the 2013 ERD chapter, while some of them have been removed in this chapter (*e.g.*, molecular memory, atomic switch, *etc.*) and several new technologies are added in this chapter (*e.g.*, novel magnetic memory, transistor laser, *etc.*)

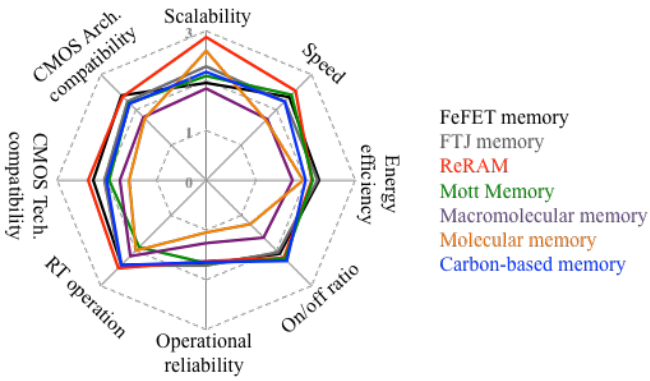
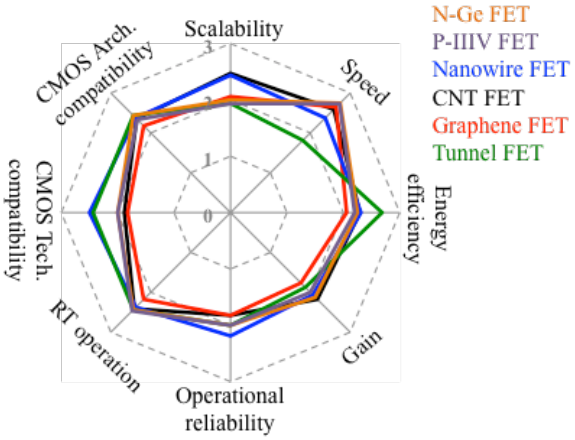
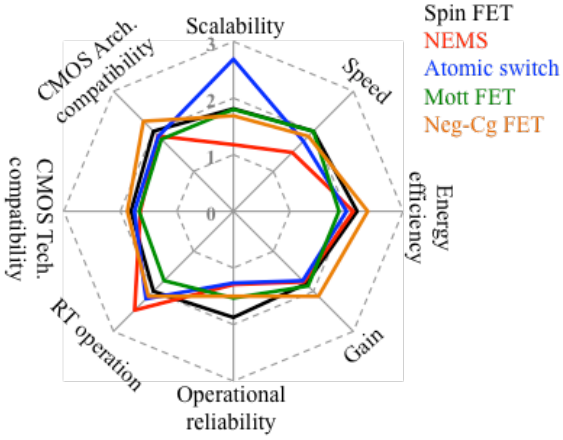


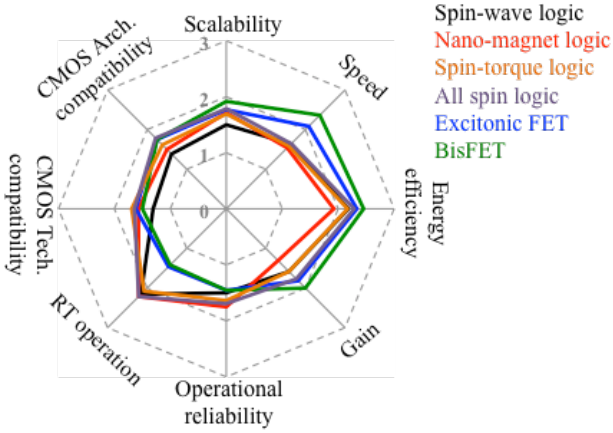
Figure BC6.4 Comparison of Emerging Memory Devices Based on 2013 Critical Review



(a) CMOS extension devices



(b) Charge-based beyond-CMOS devices



(c) Non-charge-based beyond-CMOS devices

Figure BC6.5 Comparison of Emerging Logic Devices Based on 2013 ITRS ERD Critical Review: (a) CMOS Extension Devices; (b) Charge-based Beyond-CMOS Devices; (c) Non-charge-based Beyond-CMOS Devices

Since "3" represents the best result and "1" the worst in the spider chart, devices with larger circle area represent more promising devices. In Figure BC6.5 for emerging logic devices, the perceived potential of "beyond-CMOS devices" is generally poorer than "CMOS-extension devices". Within "beyond-CMOS devices", "non-charge-based devices" area also perceived slightly less promising than "charge-based devices". The general trend is consistent with the quantitative assessment in section 6.2. Multiple factors contribute to this result, including the strength of CMOS as a platform technology, the challenges of beyond-CMOS

devices in materials, fabrication, and even mechanisms, the lack of memory and interconnect solutions for beyond-CMOS devices, *etc*.

7. SUMMARY

The "beyond-CMOS" chapter systematically surveys emerging memory and logic devices (sections 2 and 3), novel technologies (section 4), and alternative architectures and computing paradigms (section 5), to explore potential solutions beyond the conventional scaling of CMOS technologies. Although high performance at low power consumption has been a primary objective of beyond-CMOS devices, novel functionalities and applications have become increasingly important. The recent emergence of energy-efficient data-intensive cognitive applications is also shifting the emphasis from high-precision computing solutions to novel computing paradigms with massive parallelism and bio-inspired mechanisms. Research opportunities exist in the co-optimization of beyond-CMOS devices and architectures to explore unique device characteristics and architectural designs.

Although a beyond-CMOS device competitive against CMOS FET has not been identified, beyond-CMOS devices with dramatically enhanced scalability and performance while simultaneously reducing the energy dissipation per functional operation would still be fundamentally important and a worthwhile research objective. In considering the many disparate new approaches proposed to provide order of magnitude scaling of information processing beyond that attainable with ultimately scaled CMOS, the following set of guiding principles are proposed to provide a useful structure for directing research on "Beyond CMOS" information processing technology.

- ***COMPUTATIONAL STATE VARIABLE(S) OTHER THAN SOLELY ELECTRON CHARGE***

These include spin, phase, multipole orientation, mechanical position, polarity, orbital symmetry, magnetic flux quanta, molecular configuration, and other quantum states. The estimated performance comparison of alternative state variable devices to ultimately scaled CMOS should be made as early in a program as possible to down-select and identify key trade-offs.

- ***NON-THERMAL EQUILIBRIUM SYSTEMS***

These are systems that are out of equilibrium with the ambient thermal environment for some period of their operation, thereby reducing the perturbations of stored information energy in the system caused by thermal interactions with the environment. The purpose is to allow lower energy computational processing while maintaining information integrity.

- ***NOVEL ENERGY TRANSFER INTERACTIONS***

These interactions would provide the interconnect function between communicating information processing elements. Energy transfer mechanisms for device interconnection could be based on short range interactions, including, for example, quantum exchange and double exchange interactions, electron hopping, Förster coupling (dipole–dipole coupling), tunneling and coherent phonons.

- ***NANOSCALE THERMAL MANAGEMENT***

This could be accomplished by manipulating lattice phonons for constructive energy transport and heat removal.

- ***SUB-LITHOGRAPHIC MANUFACTURING PROCESS***

One example of this principle is directed self-assembly of complex structures composed of nanoscale building blocks. These self-assembly approaches should address non-regular, hierarchically organized structures, be tied to specific device ideas, and be consistent with high volume manufacturing processes.

- ***ALTERNATIVE ARCHITECTURES***

In this case, architecture is the functional arrangement on a single chip of interconnected devices that includes embedded computational components. These architectures could utilize, for special purposes, novel devices other than CMOS to perform unique functions.

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