IEEE
Advancing Technology for Humanity

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

2017 EDITION

LITHOGRAPHY

THE IRDS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

COPYRIGHT © 2018 IEEE. ALL RIGHTS RESERVED.

Table of Contents

Acknowledgments iii
1. Introduction 1
1.1. Lithography Drivers 1
1.2. Development of Roadmap 1
2. Technology Requirements 2
2.1. Summary 2
3. Potential Solutions 3
3.1. Line and Space Potential Solutions 3
3.2. Contact Hole, Via and Cut type pattern Potential Solutions 4
4. Challenges 5
4.1. Short-term Challenges (2017 to 2024) 5
4.2. Long-term Challenges (2025 and Beyond) 7
5. Summary and Key Points 7

List of Figures

Figure LITH-1 Line and Space Potential Solutions 4
Figure LITH-2 Contact Hole, Via and Cut Type Pattern Potential Solutions 5

List of Tables

Table LITH-1 Lithography Technology Requirements 3
Table LITH-2 Near-term Challenges (2017 to 2024) 7

Link to Lithography Excel file of Tables and Figures

COPYRIGHT © 2018 IEEE. ALL RIGHTS RESERVED.

ACKNOWLEDGMENTS

We wish to thank the 2017 Lithography International Focus Team members:

Ted Fedynyshyn, Heiko Feldmann, Cesar Garza, Frank Goodwin, Naoya Hayashi, Hidemi Ishiuchi, Ryoung-han Kim, SeongSue Kim, Ajay Kumar, David Kyser, Mark Neisser, Shinji Okazaki, Masahiko Okumura, Abbas Rastegar, Doug Resnick, Tadatake Sato, Kiwamu Sue, Walt Trybula, Takeo Watanabe, John Wiesner, Jim Wiley, Grant Willson, Stefan Wurm, Akiyoshi Yamazaki

COPYRIGHT © 2018 IEEE. ALL RIGHTS RESERVED.

LITHOGRAPHY

1. INTRODUCTION

Historically, improvements in lithography have been a key enabler to make improved chip technologies. The International Roadmap for Devices and Structures (IRDS) Lithography roadmap predicts where current patterning capability can support future chip generations and where there are challenges and improvements are needed. It is intended to be used to by semiconductor industry participants, by industry analysts, and by researchers who want or need to know how the industry will evolve in the future and what challenges need to be addressed.

1.1. LITHOGRAPHY DRIVERS

This Lithography roadmap projects how the patterning needs of new devices in the More Moore roadmap might be met and where the key challenges are. In the past, both logic and memory devices have driven improvements in patterning technology. Key drivers of patterning technology have been high performance logic chips, DRAM memory and flash memory. New capabilities to shrink dimensions enabled smaller devices that performed better than the previous generation. Once a new lithography technology became available, it was adopted for both memory and logic, perhaps with slightly different timing. But now devices are small enough that just shrinking them can give unacceptable electrical performance. For example, shrinking metal level critical dimensions can increasing the resistance of metallization too much and shrinking insulation critical dimensions can increase current leakage and give unacceptable power consumption. This has driven the industry to innovate in device design to avoid these effects and keep increasing the number of devices per unit of silicon area. This innovation has taken different forms for different types of devices.

Flash memory becomes unreliable as the physical size of the bits becomes too small. So planar (or 2D) flash memory will stop shrinking critical dimensions (CDs), and the smallest CD devices will have a critical dimension of about 15 nm half pitch. These CDs can be achieved by the self-aligned quadruple patterning (SAQP) technology already in extensive use. So planar flash will not be a driver for new patterning technology. The industry is moving to three-dimensional (3D) flash memory to enable improved bit density on chips. In 3D flash, the memory bits are much larger than in 2D, and higher bit density per chip is achieved through extensive stacking of bits on top of each other. For these 3D devices the smallest CD is 20 nm half pitch and that is only on one level. The other levels have much larger CDs. These CDs are readily achieved by currently available patterning technology. However patterning cost and also potentially the difficulty of patterning over topography are concerns. This is driving the evaluation of nanoimprint technology for 3D flash use.

Already, high performance logic implemented the finFET device to improve performance and enable higher density devices. The 2017 More Moore roadmap calls for more such device changes. These improved devices are projected to require smaller printed features. DRAM devices are also shrinking but are more cost sensitive and have less complicated designs that are less demanding of lithography than logic. So high performance logic is the key driver for higher resolution in patterning, and DRAM is projected to follow closely.

1.2. DEVELOPMENT OF ROADMAP

This roadmap was developed through consultation with an international team of patterning experts and through review of publicly available literature and other publicly available documents. The current contributing membership is shown in the Acknowledgments. Contributing members come from Asia, Europe, and the United States and represent semiconductor, equipment and material manufacturers, as well as research institutes. The IRDS More Moore focus team provides the device roadmap from which lithography requirements are derived. Through polls of the lithography team members the key options, their timing and their key challenges are developed. These are codified in a set of Excel tables and those tables were used to write this document. The table and this document undergo internal review by the team and by the overall IRDS before publication. In this year, the tables follow the convention of the More Moore tables and have only columns for each year a new product node is expected to be introduced. Intervening years are omitted. However, in the potential solutions' charts the x axis is time, so the intervening years are included so the reader can readily see the time frames required for innovation. There are two possible options charts, one for lines and spaces and one for hole type patterns such as contacts, vias, cuts and vertical gate all around devices, because these two types of patterning have very different requirements and the timing of innovation is different for each of them. Some of the tables from previous years' roadmaps have not been updated, due to lack of significant changes in the general content or the lack of new information to add to previous year's roadmaps. For details of these tables, please consult prior roadmaps.

COPYRIGHT © 2018 IEEE. ALL RIGHTS RESERVED.

2. Technology Requirements

2.1. Summary

The More Moore requirements related to lithography are shown in the Table LITH-1 below, along with the Lithography team's color coding for feasibility. Feature sizes that can be done with extreme ultraviolet (EUV) single patterning using the generation of tools currently being shipped are in yellow, meaning "manufacturing solutions are known," because semiconductor manufacturers now have enough confidence in EUV to commit to EUV manufacturing by 2019. Line and space half pitches of 10.5 nm are coded red, meaning "manufacturing solutions are not known", because this is not doable with EUV single patterning using available tools; and, although it is larger than the theoretical resolution limit for argon fluoride (ArF) immersion patterning, it is considered that the tolerance build up issues for quadruple patterning such small features aren't solved yet. Any lines and spaces smaller than 10 nm half pitch are also coded red as are hole type patterns below the current single exposure resolution capability of EUV and below the quadruple patterning limit for ArF immersion. However, the logic contacted poly half pitch and the physical gate length for high performance logic are coded white to the end of the table. This is because these two dimensions are set by thin film deposition processes and not set lithographically.

The lines and spaces coded red in Table LITH-1 can all be reached with EUV double patterning. This is not true for most of the hole type patterns coded red in the table. So, hole type patterns are expected to be more of a challenge in the future than lines and spaces. The vertical gate all around (VGAA) patterns are expected to be a particular challenge. In these devices the gate is a vertical pillar of silicon with a thin collar of insulator around it that is the equivalent of gate oxide. The pillar of silicon is a cylinder, so defining it lithographically requires a hole type pattern. For the largest VGAA patterns, expected to be in volume production in 2030, the silicon cylinder has a diameter 6 nm and is on a pitch of 14 nm. The collar is project to be 4 nm thick, so this pattern requires either printing 6 nm holes on a 14 nm pitch and then turning the sides of the cylinder into insulator or printing 10 nm holes on a 14 nm pitch and then adding four nm of insulator to the side walls. Printing such a pitch would require EUV triple or quadruple patterning, clearly not a feasible technique today. The VGAA gate pattern sizes projected for 2030 onward are probably out of reach even with EUV quadruple patterning.

Line edge roughness (LER) and line width roughness (LWR) are the main challenges in the requirements other than reaching the desired critical dimension. High numerical aperture (NA) EUV exposure tools with a reduced field size are projected to be available in the early 2020's, in time for the 2024 column shown in Table LITH-1. However, there are challenges associated with such tools. Besides the normal challenges for new tool generations of overlay, resolution, aberrations and such, stochastic effects will be worse with smaller features. Also, EUV multiple patterning could compete with High NA EUV as an option for 7 to 10 nm half pitch lines and spaces.

Copyright © 2018 IEEE. All rights reserved.

Table LITH-1 Lithography Technology Requirements

YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
DRAM							
DRAM minimum ½ pitch (nm)	18	17.5	17.0	14.0	11.0	8.4	7.7
Key DRAM Patterning Challenges	Resolution improvements at reasonable cost						
CD control (3 sigma) (nm) [B]	1.8	1.8	1.7	1.4	1.1	0.8	0.8
Mininum contact/via after etch (nm) [H]	18	17.5	17	14.0	11.0	8.4	7.7
Minimum contact/via pitch(nm)[H]	54	53	51	42	33	25	23
Overlay (3 sigma) (nm) [A]	3.6	3.5	3.4	2.8	2.2	1.7	1.5
Flash							
2D Flash ½ pitch (nm) (un-contacted poly)	15	15	15	15	15	15	15
Key 2D Flash Patterning Challenges	none						
Flash 3D Channel half-pitch targets (nm)	80	80	80	<80	<80	<80	<80
3D NAND bit line half pitch(nm)	20.0	20.0	20.0	20.0	20.0	20.0	20.0
Key 3D Flash Patterning Challenges	Overlay, patterning over topography						
CD control (3 sigma) (nm) [B]	1.5	1.5	1.5	1.5	1.5	1.5	1.5
Overlay (3 sigma) (nm) [A]	5.0	5.0	5.0	5.0	5.0	5.0	5.0
MPU / Logic							
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
Key MPU/Logic Patterning Challenges	LWR & LER, metal half pitch, VGAA structures						
MPU/ASIC Minimum Metal ½ pitch (nm)	18.0	14.0	12.0	10.5	7.0	7.0	7.0
Metal LWR [C]	1.8	1.4	1.2	1.1	0.7	0.7	0.7
Metal CD control (3 sigma) (nm) [B]	1.8	1.4	1.2	1.1	0.7	0.7	0.7
Contacted poly half pitch (nm)	27.0	24.0	21.0	18.0	16.0	16.0	16.0
Gate LER [C]	1.4	1.3	1.1	1.0	0.8	0.8	0.8
Physical Gate Length for HP Logic (nm)	20	18	16	14	12	12	12
Gate CD control (3 sigma) (nm) [B]	2.0	1.8	1.6	1.4	1.2	1.2	1.2
Overlay (3 sigma) (nm) [A}	3.6	3.5	3.4	2.8	2.2	1.7	1.5
MPU/ASIC finFET fin minimum 1/2 pitch (nm)	16.0	14.0					
Fin CD control (3 sigma) (nm) [B]	0.45	0.35					
FIN LER [C]	0.45	0.35					
Lateral Gate All Around (LGAA) 1/2 pitch			12.0	10.5	9.0		
LGAA CD control (3 sigma) (nm) [B]			0.7	0.7	0.7		
GAA LER [C]			0.49	0.49	0.49	0.21	0.21
Vertical Gate All Around (VGAA) half pitch (nm)						7.0	7.0
Vertical GAA Diameter (nm)						6.0	6.0
VGAA CDU (nm)						0.3	0.3
Contact-Gate enclosure thickness per side (nm)						2.0	2.0
MPU/ASIC minimum contact hole or via pitch (nm)	51	40	34	30	20	20	20
Contact/via CD after etch (nm) [H]	18	14	12	10.5	7.0	7.0	7.0
Contact CD (nm)after etch - finFET, LGAA	18	16	14	12	10		
Contact CD (nm) after etch - VGAA [I]						12	12
Chip size (mm^2)							
Maximum exposure field height (mm) [E]	26	26	26	26	26	26	26
Maximum exposure field length, i.e. scanning direction (mm) [E]	33	33	33	16.5	16.5	16.5	16.5
Maximum field area printed by exposure tool (mm^2) [E]	858	858	858	429	429	429	429

3. Potential Solutions

3.1. Line and Space Potential Solutions

Lines and spaces are the flagship pattern of lithography. In practice, the minimum imageable half pitch for lines and spaces is smaller than the minimum imageable half pitch for contact hole patterns, so when leading edge resolution is discussed it usually refers to dense line and space capability. The roadmap predicts that DRAM and logic metal levels will drive

Copyright © 2018 IEEE. All rights reserved.

improvements in line and space resolution. Figure LITH-1 shows different product nodes and their projected time frames for implementation along with possible patterning options for each node. Note that the logic node names are the commonly used names for each node but are not the same as the minimum half pitches of those nodes. Resolution improves to 11 to 12 nm half pitch over the next four years. Then a further increase in line and space resolution isn't needed until 2027, when minimum line and space resolution is expected to reach 7 or 8 nm half pitch. After that no further improvement in required resolution is projected.

The 10 nm logic node and the 18 nm DRAM have already selected quadruple patterning for their smallest lines and spaces. The 7 nm logic node will have versions made both with EUV patterning and with ArF immersion patterning and no EUV. The 5 nm and 3 nm Logic nodes after that will potentially need EUV double patterning for their smallest pitches but could still use ArF immersion quadruple patterning if necessary. It's also possible that improvements in EUV single patterning will occur enabling smaller half pitches with EUV single patterning. For DRAMs, either quadruple patterning with ArF immersion, EUV or nanoimprint lithography (NIL) will be used for nodes down to 10 nm half pitch.

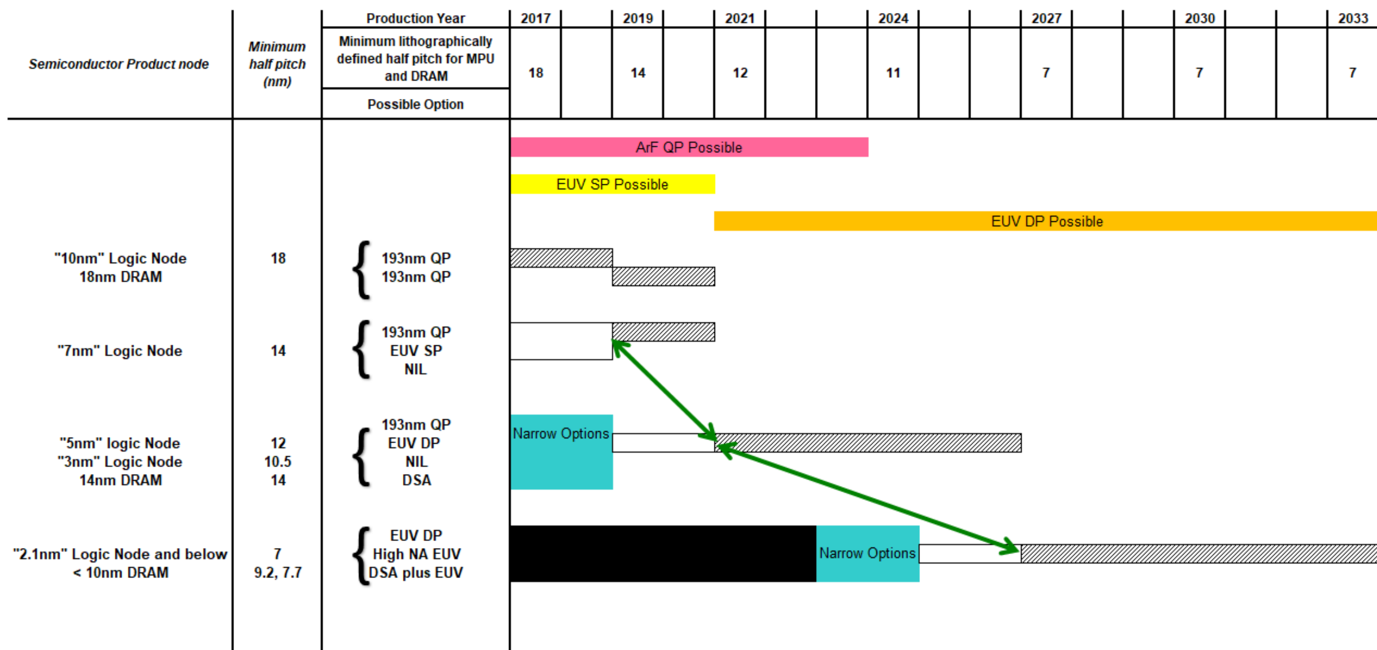

Figure LITH-1 Line and Space Potential Solutions

3.2. Contact Hole, Via and Cut type pattern Potential Solutions

In the past, contact holes and other hole type patterns usually have had a larger minimum pitch than the lines and spaces in a memory or logic device. However, the current roadmap predicts their minimum pitch will shrink faster than the minimum pitch for lines and spaces. When VGAA geometries are implemented, minimum hole type pattern half pitch will match the minimum pitch of lines and spaces. This is a big patterning challenge. Potential solutions for hole type patterns are shown in Figure LITH-2. Already by 2019 more than four ArF immersion exposures could be necessary for some levels, and by 2024, EUV double patterning will not have adequate resolution. As shown in the roadmap, this will drive the evaluation of many technologies. The advent of vertical gate all around transistors will drive patterning of very small pitch holes. A lot of patterning research and development will be needed in the next eight years to achieve this capability.

Copyright © 2018 IEEE. All rights reserved.

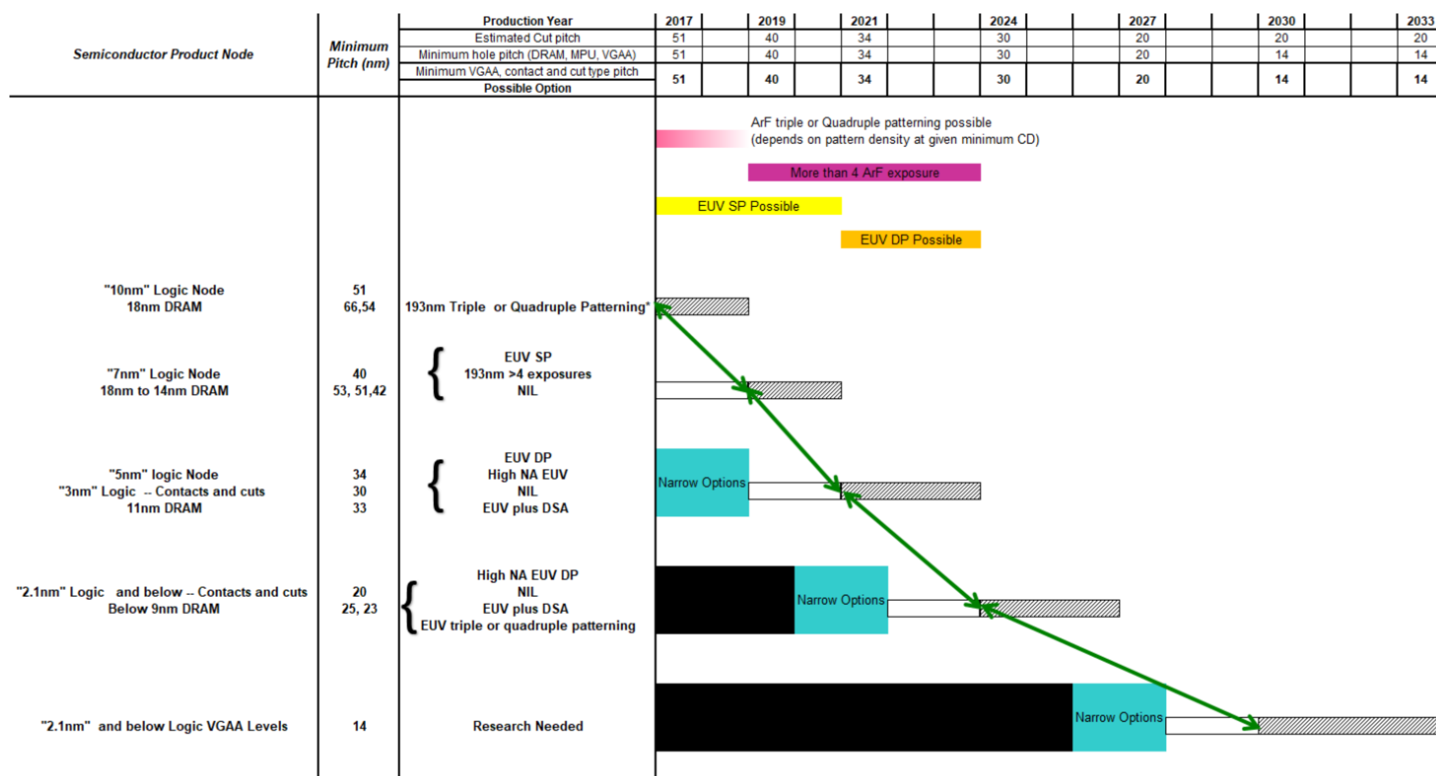

Figure LITH-2 Contact Hole, Via and Cut Type Pattern Potential Solutions

4. CHALLENGES

4.1. SHORT-TERM CHALLENGES (2017 TO 2024)

The challenges for improving patterning are different depending on what novel patterning approach is taken. In the current environment, different novel patterning techniques are being applied to different applications. Five different potential new patterning technologies have had significant research and development applied to them.

Multiple patterning with more than 4× pitch reduction or more than 4 exposure steps per level is the alternative every other method is compared to. 4× pitch multiplication is already in use, and the extension to smaller features is considered doable. However, each of the individual steps in a multiple patterning process has tolerances associated with it and the more the multiplication, the more the steps, the more tightly controlled each of those tolerances needs to be. This makes the cycle time of developing such a process long and expensive. What is more, even given a working multiple patterning process, the actual process time to do such layers is long. This makes the cycle time for making new chip designs also quite long. This is a substantial drawback for multiple patterning extensions. All of the four alternative technologies discussed below have faster cycle times than >4× multiple patterning. Even if they prove to be as expensive as a multiple patterning process, the reduction in process complexity could drive adoption of one or more of these technologies.

EUV has made significant progress in the last two years. Manufacturing tools are now in use that provide enough throughput and uptime to do chip pilot-scale production. Logic foundry producers have announced their commitment to producing products using EUV with a target date of early 2019 and possible use late in 2018.

Challenges do remain. Tool uptime is running at 70 to 85%, which is not enough for manufacturing. The only manufacturing level EUV exposure tool supplier has a target of 95% uptime by the time actual manufacturing commences. A second challenge is the resolution LER and sensitivity (RLS) tradeoff, that is, the need to have usable photospeed and resolution in combination with low enough stochastic effects. More experience is needed to determine if acceptable resist defects can be realized at a reasonable photospeed. A third challenge is defectivity, particularly for masks. There is no actinic inspections system for patterned mask inspection. This makes eliminating mask defects a challenge. The need to eliminate defects in mask blanks reduces their yield and constrains mask supply. Improved airborne molecular contamination (AMC)

COPYRIGHT © 2018 IEEE. ALL RIGHTS RESERVED.

and metrology are also needed for EUV. With ArF immersion lithography the smallest features actually printed in resist are 40 nm critical dimension or so. With EUV the smallest CD is less than half this size and in a thinner film of resist. This is both harder to measure and more sensitive to AMC.

The lack of a usable pellicle system means that mask defect adders can occur in production and reduce yield substantially. Currently, EUV users must do extensive inspection of exposed patterns to overcome this lack of pellicles. Pellicles are under development, but not available yet. When pellicles are available, they will reduce exposure throughput by absorbing some EUV, leading to a different sort of cost impact. EUV tool uptime and the lack of pellicle technology are concerns that, once resolved, should stay resolved. However, stochastic issues will require continual improvement because extension of EUV to smaller features will make stochastics worse. It is not known how to resolve stochastics for future nodes, and this needs to be the subject of research. High NA EUV is under development, but is not projected to be ready until the early 2020's.

Nanoimprint lithography has also made significant progress in the last two years. Defect levels and throughput have both been improved. Now manufacturing grade tools are available. Since the templates are 1× (that is, the feature sizes on the template are the same size as the printed features, unlike conventional lithography), the templates are difficult to make for logic and DRAM leading edge feature sizes. But 3D flash memory has much larger feature sizes that 2D flash, so it is a natural type of product to first use nanoimprint on. The newly available nanoimprint tools are now in use to develop production processes for 3D flash memory with possible high-volume manufacturing in 2019.

Directed self-assembly (DSA) has not done as well in the past two years as nanoimprint or EUV. Defectivity issues were not resolved in time for use in targeted memory product nodes, and memory makers turned to other techniques. Logic makers are still investigating DSA, mostly for improving contact hole critical dimension uniformity and for making fin structures for finFETs. The earliest possible implementation is probably the 5 nm logic node. Research into DSA continues. DSA has very different stochastics than traditional resist. As feature sizes shrink, stochastic issues will become more important, and this may be an opportunity for DSA compared to traditional resist.

Direct write ebeam lithography using multiple beams has made progress for writing mask patterns. Beta type mask writing machines are available now. However, little progress was reported in 2016 or 2017 on chip writing tools. The generation of tools that was under development two years is no longer suited to leading edge critical dimensions. If they are successfully developed, they could find application for personalizing computer chips, but they are not currently a factor in the roadmaps for leading edge dimensions discussed here. However, the 2018 SPIE conference has several updates on this technology, so progress may have resumed.

Near term challenges, together with target applications and potential earliest timing for each of the options discussed above are shown in Table LITH-2as a function of the patterning approach.

COPYRIGHT © 2018 IEEE. ALL RIGHTS RESERVED.

Table LITH-2 Near-term Challenges (2017 to 2024)

Next Generation Technology	First Possible Use in Mfg.	Feature Type	Device Type	Key Challenges	Required Date for Decision making
Multiple Patterning Extension to >4X patterning	2019	Vias, contacts or cut patterns for high performance logic	"7nm" Logic Node	-Tolerances, EPE and OL -Development cycle time too long -Cost of process	Already committed
EUV	2018	22 to 24nm hp CH/Cut Levels back end metals at 18nm hp LS	"7nm" Logic Node	-Tool uptime -Defectivity, especially keeping masks defect free -Resist speed combined with LER and Stochastics	Already committed
NanoImprint	2019	20nm lines and spaces 20 to 30nm hp contact holes	3D Flash Memory	-Defectivity -Overlay -Master Template writing and inspection <20nm -Template replication <20nm	2018
DSA (for pitch multiplication)	2021	Contact holes/cut levels for logic. Possibly nanowire patterning	"5nm" Logic Node	-Pattern Placement -Defectivity and defect inspection -Design -3D Metrology	2019
Maskless Lithography (ML)	No current leading edge semiconductor plans	Not applicable	Not applicable	-Concept demonstration -Functioning tool	Not Applicable

4.2. Long-term Challenges (2025 and Beyond)

Resolution may not be a challenge in after 2027, if device development focuses on 3D devices. The large number of masking levels and the many steps for 3D stacking of devices will make yield and cost high priorities. So, potential patterning challenges will probably be related to cost, yield and defectivity, imaging over topography, and alignment and overlay over complicated 3D stacks. Etch and deposition of sub 10 nm structures are also major challenges. Innovative integration schemes that use the intersection of edges to produce small hole or pillars might also be needed to produce VGAA structures at a reasonable cost.

Another potential challenge might be implementing patterning on 450 mm wafers. However, if EUV is a mainstream patterning method in widespread use, this could limit the financial benefit of switching to 450 mm wafers. In past wafer size transitions, the change in wafer size has enabled more silicon area to be exposed per unit time, giving substantial lithography cost benefits. But in EUV lithography, the throughput is limited by the power of the light source. A larger wafer will take proportionally longer time to expose, so little or no throughput benefit will be gained for EUV by switching from 300 mm to 450 mm wafers. Thus, the financial benefit of switching to 450 mm could be smaller than the financial benefit of past wafer size transitions; since there is no cost benefit for some of the lithography exposure steps, which are a substantial cost contributor to semiconductor chip production. Potentially other patterning methods could be used for 450 mm wafers giving a different financial tradeoff. But to our knowledge, little or no current work is currently being done on extending any patterning methodology to larger wafer sizes than 300 mm.

5. Summary and Key Points

Higher resolution patterning is needed to support the industry device roadmap. Flash memory innovation has switched to 3D structures and is looking for lower cost patterning rather than higher resolution patterning. The leading candidate for novel 3D flash patterning is nanoimprint and it is competing with krypton fluoride (KrF) lithography for adoption. DRAMs and logic are both driving higher resolution patterning, with logic devices slightly ahead of DRAMs in their critical dimension roadmap. The roadmap for hole-type patterns is more aggressive than the roadmap for line and space-type patterns and will be the biggest challenge in the future. Potential new patterning technologies for improved resolution are high resolution EUV, extensions of multiple patterning, nanoimprint and DSA. The roadmap shows continued resolution improvements through 2027. But after that, logic devices will switch to 3D architectures and DRAM minimum dimensions will plateau. So long term, patterning challenges will be related to etch, deposition yield and topography, rather than minimum resolution.

Copyright © 2018 IEEE. All rights reserved.