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EMERGING RESEARCH MATERIALS

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EMERGING RESEARCH MATERIALS

1. INTRODUCTION

1.1. CURRENT STATE OF TECHNOLOGY

The semiconductor industry was historically driven by a strong correlation between technology scaling and performance of most integrated circuits (ICs). The PC market required more complex and faster microprocessors that largely drove the development and scaling of transistors and memory. These devices required new materials and processes such as strained silicon, high-κ gate dielectrics and metal gate electrodes that are now widely, and will continue, to be used in IC manufacturing. In the past decade, a completely new ecosystem has emerged. New system integrators, from mobile to data centers to the Internet of Everything (IoE), have appeared with new and complex technology requirements. These system integrators will have impact that includes microprocessors, but extends towards new applications including medicine, energy, and the environment.

1.2. DRIVERS AND TECHNOLOGY TARGETS

As transistors and memory begin to run out of horizontal space and ICs continue to be limited by power, device technologies will enter a phase characterized by vertical integration and performance specifications driven towards reduction of power. New transistor, memory, interconnect, lithography materials and processes will be required to enable this new More Moore scaling paradigm. As conventional information processing and storage technology reaches its ultimate limits, entirely new non-CMOS logic and memory devices and even new, non-Von Neumann circuit architectures are potential Beyond CMOS solutions. Such solutions ideally can be integrated onto the Si-based platform to take advantage of the established processing infrastructure, as well as being able to include Si devices such as memories, onto the same chip. However, while these technologies will likely be integrated on a Si-based platform, the vast majority of these Beyond CMOS technologies are based on entirely new materials and physics. Finally, new system integrators require materials that enable potentially trans-disciplinary advances in monolithically integrated complex functionality, i.e., functional scaling. Significant challenges must be overcome for these emerging materials to provide viable solutions for future integrated circuit technologies. To deliver these capabilities, enhanced metrology will be needed to accelerate material evaluation, improvement, and capabilities. The ultimate goal is to provide timely guidance on emerging material and process performance, cost, reliability, and sustainability options that will drive breakthrough advances in future manufacturing technology.

2. SCOPE OF REPORT

The IRDS represents a strategic repositioning of the devices and systems' community's scope, needs, and set of emergent opportunities. In alignment with this new perspective, this edition of the Emerging Research Materials (ERM) chapter represents a work in transition with a primary goal of aligning with the needs of related IRDS working groups. Much of the associated information in the detailed requirements and solutions tables comes from prior ERM chapters from the ITRS roadmap work and input from current IRDS working groups and will be updated in future editions. The chapter emphasizes strategic difficult challenges and/or enabling of novel, breakthrough and potentially disruptive opportunities for emerging material properties, synthetic methods, and metrology, organized in the following areas:

1. ***Scaled technology materials needs for More Moore:*** transistors, memory, interconnects, lithography, heterogeneous integration, assembly and packaging.
2. ***Novel materials for Beyond CMOS:*** emerging logic and information processing devices, emerging memory and storage devices, and novel computational paradigms and architectures.
3. ***Potentially disruptive material opportunities for functional scaling and convergent applications****:* Heterogenous components, outside system connectivity, and high impact application areas such as energy, environment, agriculture, health, medical, etc.

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3. CHALLENGES

3.1. NEAR-TERM CHALLENGES

Table ERM1 Near-term Difficult Challenges

Near-Term Challenges: 2017–2024	*Description*
Materials and processes that achieve performance and power scaling of lateral fin- and nanowire FETs (Si, SiGe, Ge, III-V).	Integrated high κ dielectrics with equivalent oxide thickness (EOT) <0.5 nm and low leakage. Integrated contact structures that have ultralow contact resistivity. Achieving high-hole mobility in III-V materials in field effect transistor (FET) structures. Achieving high-electron mobility in Ge with low-contact resistivity in FET structures. Processes for achieving low dislocations and anti-phase boundary generating interface between Ge/III-V channel materials and Si. Dopant placement and activation, i.e., deterministic doping with desired number at precise location for V_{th} control and source/drain (S/D) formation in Si as well as alternate materials.
Materials and processes that improve copper interconnect resistance and reliability	Mitigate impact of size effects in interconnect structures. Patterning, cleaning, and filling at nano dimensions. Cu wiring barrier materials must prevent Cu diffusion into the adjacent dielectric but also must form a suitable, high quality interface with Cu to limit vacancy diffusion and achieve acceptable electromigration lifetimes. Reduction of the κ value of inter-metal dielectrics.
Materials and processes for continued scaling of dynamic random access memory/static random access memory (DRAM/SRAM) and embedded nonvolatile memory (NVM)	Low temperature materials for high performance vertical transistor memory select structures. High-κ, low leakage DRAM dielectrics. Processes for stacking of 3D Flash.
Materials and processes that extend lithography to sub-10 nm dimensions with reproducible properties	Novel resists to extend 193 nm lithography and support extreme ultra-violet (EUV) lithography. Directed self-assembly (DSA) with materials such as block-copolymers to potentially extend lithography though pattern rectification and pattern density multiplication.
Materials for heterogeneous integration of multi-chip, multi-function packages.	Materials to modify polymer properties to enable increased product reliability. Novel electrical attaching materials to allow lower assembly temperatures and improved product reliability. Simultaneously achieve package polymer coefficient of thermal expansion (CTE), modulus, electrical and thermal properties, with moisture and ion diffusion barriers. Nanosolders compatible with <200°C assembly, multiple reflows, high strength, and high electromigration resistance. Nanoinks that can be printed as die attach adhesives with required electrical, mechanical, thermal, and reliability properties.

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3.2. LONG-TERM CHALLENGES

Table ERM2 Long-term Difficult Challenges

Long-term Challenges: 2025–2032	*Description*
Materials and processes that achieve 3D monolithic and vertical integration of high mobility and steep subthreshold transistors	Processes for sequential 3D vertical integration of transistors. Methods to lower the synthesis temperature of vertical semiconductor nanowires. Methods to dope and contact vertical semiconductor nanowire transistors. Lithography-free and low-temperature methods to achieve gate stack on vertical transistors.
Materials and processes that replace copper interconnects with improved reliability and electromagnetic performance at the nanoscale	Synthesis or assembly of carbon nanotubes (CNTs) in predefined locations and directions with controlled diameters, chirality and site-density. Carbon and collective excitations. Novel interlayer dielectrics: Metal Organic Framework (MOF) and Carbon Organic Framework (COF). Metals with less size effects such as silicides.
Materials and processes for charge-based and non-charge-based beyond CMOS logic that replaces or extends CMOS	Achieving a bandgap in graphene in FET structures. Synthesis of CNTs with tight distribution of bandgap and mobility. Complex metal oxides with low defect density. High mobility transition metal dichalcogenides with low defect density and low resistance ohmic contacts. Spin materials: characterization of spin, magnetic, and electrical properties, and correlation to nanostructure.
Materials and processes for emerging memory and select devices to replace DRAM/NVM.	Multiferroic with Curie temperature >400 K and high remnant magnetization to >400 K. Ferromagnetic semiconductor with Curie temperature >400 K. Complex Oxides: Control of oxygen vacancy formation at metal interfaces and interactions of electrodes with oxygen and vacancies. Switching mechanism of atomic switch: Improvements in switching speed, cyclic endurance, uniformity of the switching bias voltage and resistances both for the on-state and the off-state.
Materials and processes that enable monolithically 3D integrated complex functionality including thermal and yield challenges	Integration on CMOS Platforms. Integration with flexible electronics. Biocompatible functional materials. Leveraging convergent materials expertise in adjacent sectors.

4. TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

4.1. SUMMARY

The IRDS seeks a framework for managing the convergence of scaled information processing and storage, i.e., More Moore (MM) and Beyond CMOS (BC), with the next emerging era of monolithically integrated systems that achieve enhanced overall functional density. The trend towards the convergence of monolithically integrated functional diversification with miniaturization manifests as increasing complexity in the road-mapping process. The IRDS reflects this growing complexity, with an increasing number of projected roadmap parameters and requirements associated with new functionalities. While ERM continues to support the evolutionary, and semiconductor centric needs of the traditional semiconductor community, emerging architectures could benefit from new device functionality, which may require new materials and new physical mechanisms. New waves of emerging materials technologies may represent potentially disruptive opportunities.

Candidate ERM materials and processes exhibit unique and useful properties that may require atomic level structural, interface, defect, and compositional control. In some cases, current synthetic or manufacturing technologies are not yet capable of producing such materials with the required level of control. The difficulties could be due to: 1) The inability of a research environment to produce materials with the required level of control that would express the desired properties; or 2) scaling up the synthetic and fabrication processes to satisfy commercial manufacturing requirements. In some cases, current materials growth processes effect unacceptable levels of defect formation, which drive the need for new and more

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robust fabrication methods. In other cases, synthetic methods exist for producing high-quality materials, but these processes cannot be scaled to the higher growth rates, yields, or purity needed for insertion into viable commercial applications. While these materials may provide proof of concept and suggest a potential solution, new cost-effective fabrication technologies may be required to warrant a candidate material's insertion into high volume manufacturing.

4.2. Scaled Technology Materials for More Moore

As described in the More Moore chapter, after 2027 there is no headroom for 2D geometry scaling and 3D very large scale integration (VLSI) of circuits and systems using sequential/stacked integration approaches will likely begin. Whether one is considering 2D geometry scaling or 3D integration, there are numerous materials challenges to achieving increasing device density and integrated performance. The following outlines key materials challenges for transistor scaling and integration, lithography, interconnects, heterogenous integration, assembly and packaging, and outside system connectivity.

4.2.1. Materials for Transistor Scaling and Integration

Continued increases in transistor device density require a variety of new materials and processes including new channels (Ge, III-V), improved doping techniques, gate stacks, and contacting structures. Table ERM3 provides a set of materials and processes priorities for transistor scaling and integration.

Table ERM3 Materials for Transistor Scaling and Integration

Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
High mobility semiconductors for complementary circuits	InGaAs, InSb, strained III-V on silicon for p-channel	High hole mobilities for complementary MOSFETs.	Achieving low defect density and elastic strain enhancement in selective deposition on silicon. Dislocations have been reduced, but other defects need attention.
			Integration of high-κ dielectric with low defect density. Interface control has been achieved by III-V surface passivation.
			Low contact and parasitic source-drain resistances. Satisfactory contact resistance has been achieved for planar devices using standard III-V contact methodologies.
			Control of stress in process and assembly and packaging needs additional effort
	n-channel Ge	High electron mobilities for complementary MOSFETs.	Integration of high-κ dielectric with low defect density. Ozone oxidized surface have reduced interface state density.
			Low contact and parasitic source-drain resistances. Metal Schottky S/D contacts need continued effort.
	Co-integration of III-V and Ge	High electron and hole mobility	Activating Ge dopants requires higher temperature than III-V processing.
			Co-integrated process compatible Schottky S/D contact metallurgies need to be investigated.

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Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
3D monolithic and vertical integration of high mobility and steep subthreshold transistors	Si or Ge nanowires	High gate control of leakage current, possibly low surface scattering, and promise for 3D monolithic integration.	Ability to grow nanowires in desired locations and directions. NW deposition in controlled locations has been demonstrated, but more work is required to integrate with monolithic processing.
			Catalyst compatible with CMOS back-end processing and associated low temperatures with introduction of deep level defects. Most efforts have focused on gold nanoparticles. Further work is required for other catalysts.
			Demonstrate controlled doping of NWs with atomically sharp boundaries. Initial co-linear and surround NW doped structure have been grown by CVD, but not monolithically.
			Develop manufacturing methodologies for surround gate structures for both horizontal and vertical NWs. Individual NW structures have been demonstrated, but monolithic structures have not.
	III-V nanowires	High electron mobility with high gate control of leakage current. Promise for 3D monolithic integration.	Ability to grow nanowires in desired locations and directions. NW deposition in controlled locations has been demonstrated, but more work is required to integrate with monolithic processing.
			Catalyst compatible with CMOS back-end processing and associated low temperatures with introduction of deep level defects. Most efforts have focused on gold nanoparticles. Further work is required for other catalysts.
			Demonstrate controlled doping of NWs with atomically sharp boundaries. Initial co-linear and surround NW doped structure have been grown by CVD, but not monolithically.
			Develop manufacturing methodologies for surround gate structures for both horizontal and vertical NWs. Individual NW structures have been demonstrated, but monolithic structures have not.
	Carbon nanotubes [1–9]	High mobility with good channel control.	Chirality control, Aligned multiple CNTs, doping, Improved contacts. Achieving semiconducting CNT purity: >99.9999% and # of aligned CNTs: 200 CNTs/micrometer
	Graphene [10]	High mobility with good channel control.	Achieving band gap formation with high mobility and ON/OFF ratio >1e4. Armchair/zigzag nanoribbon formation, Improvement of contact, doping.
	Other 2D materials (MoS_2, WSe_2, germanene, silicene, etc.) [11–14]	High mobility, good channel control, possibility of heterostructure and tunneling devices.	Large-area synthesis with low defect density, techniques for doping, improvement of contact resistance.

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Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
Deterministic doping of fin- and nanowire FETs	Single ion implant	Lateral abruptness with manufacturable technique	Dopant placement <10 nm with high throughput
	STM positioning	Atomic-scale control of position	Dramatically higher throughput and extending to different materials and dopants
	Block co-polymer or Langmuir self-assembly	Can achieve sub-5 nm ultra-shallow junctions with spike anneals, due to the lack of transient-enhanced diffusion, often encountered in ion implantation	Long range order & smaller size <5 nm
	Hybrid approach of implanting through directed block co-polymer self-assembled structure	Sub-5 nm ultra-shallow junctions	Long range order & smaller size <5 nm
	Dopant electrical activation	Maintain high concentration of active dopants with an abrupt transition	Low thermal budget; ms-timescale energy pulses, Microwave uniformity
Ultra-high k gate dielectric with EOT <0.5 nm	Deposit a thin dielectric with a high barrier to electron and hole tunneling followed by an extremely high-k dielectric such as TiO_2 or $SrTiO_2$.	Improved transistor performance with low gate leakage and improved energy efficiency	Identifying higher dielectric constant materials to achieve sub-0.5 nm EOT with low leakage and low Dit.
Contacts for fin- and nanowire FETs	Tunnel barrier contacts	Eliminates contact Fermi level pinning	Identifying passivating materials for the semiconductor that does not impact contact resistivity
	Dielectric dipoles	Reduces Schottky barrier heights	Identifying passivating materials for the semiconductor that does not impact contact resistivity

4.2.2. Materials for Lithography and Patterning

The future of scaled technologies depends upon emerging patterning materials (resist or self-assembled) to enable extensible lithographic capabilities. New resist materials must concurrently exhibit higher resolution, higher sensitivity, reduced line edge roughness, and sufficient etch resistance to enable robust pattern transfer. 193 nm and EUV extension materials are being developed that can improve line width roughness (LWR), pattern shrink materials, and topcoats for EUV to ameliorate issues with out-of-band optical flare and outgassing. Evolutionary approaches for enhancing positive, negative, and chemically amplified families of resists will continue to be evaluated. Leading process approaches to pitch division include multiple patterning (MP) and spacer patterning (SP) as options for extending 193 nm immersion lithography. Alternate technologies are utilizing patterning materials to create guide patterns for directed self-assembly, which can include resists to form chemoepitaxy and graphoepitaxy guides, or directly patternable brushes and self-assembled monolayer (SAMs). DSA with block-copolymers or polymer pairs has made significant progress in characterizing sources of defect formation and in applications such as contact rectification, fin patterning, and pattern density multiplication. Table ERM4 provides a set of materials and processes priorities for lithography and patterning.

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Table ERM4 Materials for Lithography and Patterning

Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
Extending 193 nm	Self-aligned selective growth and post-pattern modification processes/materials (ALD and spin-on) [1]	Increasing process window, narrowing linewidth and process simplification	Edge placement error. Line width roughness (LWR) mitigation. Subsequent etch removal
EUV	Novel resists including inorganic-organic hybrids, resist with acid amplifiers and non-chemically amplified resists [2–6]	Improved line edge roughness, high etch resistance and increased sensitivity	Achieving resolution, etch resistance, low defect density, thermal stability and acid diffusion control.
Directed self-assembly	Block copolymer (BCP) [7–11]	Improve feature control to sub 7 nm and pitch multiplication.	Improve defect density of BCPs. Identify BCPs with high strength of interaction (χ) that meets performance and process requirements. Effective neutral surfaces with new materials

4.2.3. INTERCONNECT MATERIALS

Key challenges for continued increased performance of future integrated circuit interconnects consist of maintaining reductions of RC time constants for delivery of signals and power with high reliability. For copper interconnects, the sidewall copper barrier thickness must continue to be reduced, which is a significant challenge. For post copper interconnect scaling, novel interconnects, such as carbon nanotubes, are being explored. Also, lower dielectric constant (κ for both intra- and inter-level dielectric is needed; however, each of these emerging families of materials must overcome significant challenges for them to warrant adoption. Airgap, another approach to reducing the effective κ, places additional requirements on barrier layers or novel interconnects. Table ERM5 provides a set of materials and processes priorities for interconnects.

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Table ERM5 Interconnect Materials

Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
Conductor conductivity improvement	Barrier-less metal conductor (e.g. CuGe, etc.)	Eliminate the need for a barrier layer	Integrating novel materials in the conductor, eliminating metal diffusion and reducing the interconnect resistance. Continued research is needed.
	Novel additives (e.g. CNTs, etc.)	Reduce grain boundary scattering resistance effects.	Effective integration of the novel materials in the conductor (Cu) and simultaneously reducing the resistance of the interconnect. Continued research is needed. Integration of CNTs in Cu allowed increased current density[1] and reduced resistivity[2].
Cu barrier materials	Self-Assembled Monolayers (SAM)	Reduce barrier volume of the interconnect while reducing interconnect resistance and capacitance	Adhesion to low-κ ILD and Cu. Barrier performance and leakage current for <2 nm. Barrier performance in presence of topography and defects. Continued research needed.
	2D barrier materials: graphene, h-BN, TMDs		
Low κ ILD	Nanoporous ILD	Reduce interconnect capacitance	All low κ materials have a significant challenge to maintain dielectric constant after integration and processing. Mechanical strength, adhesion, leakage current, compatibility with patterning and packaging processes. Continued research needed.
	Mesporous ILD		
	Novel polymers		
	Air gap materials		Air gap pinch off/formation control, stability, barrier integrity, conformality. Continue research needed.
Novel vias	Carbon nanotubes (CNTs)	High density in small vias	Need of 5-10E12 tubes/cm^2, tube diameter <5-3 nm. Ability to grow in-situ and integrate 1E12 vertically aligned tubes/cm2 in 70 nm vias with repeatable yield [3,4]. 2.5E12tubes/cm^2 in 1000 nm vias [5].
		High aspect ratio (AR) via filling	Need of extremely high aspect ratio (AR) via hole filling by CNTs. Selective growth from bottom of the via hole is required. MWCNTs grown from the bottom of 90nm via hole with aspect ratio of 19 [6].
		Defect-free metal contacts	Need to produce direct metallic contacts to all the shells to minimize risks of resistance, local heating, and electromigration. Pd to date is the best metal to contact nanotubes [7].
		Effective Resistivity	Resistances down to 0.05 Ohm in 2.8 µm diameter vias (60 nm high) filled with MWCNTs have been reported [8].
		Control of chirality	All MWCNTs behavior is metallic. Need to achieve accurate control of chirality distribution for SWCNTs.
		Thermal behavior	Intrinsic CNT thermal resistance is low. Thermal interface resistance may limit performance.

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Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
Novel interconnects	Carbon nanotubes	Ability to grow in controlled locations	CNTs can be grown in specific locations with patterned catalyst [9].
		Ability to grow in controlled directions	Directional growth of a bundles of MWNTs is reported. Need higher growth rate [10]. Top-down approach to align single-walled carbon nanotubes on silicon substrate [11].
		Defect-free metal contacts	Continued research needed
		Thermal behavior	Intrinsic CNT thermal resistance is low. Thermal interface resistance may limit performance.
		Effective resistivity	Need to improve the quality of CNTs to achieve longer ballistic length.
	Graphene	Ability to prepare at controlled locations	Graphene can be grown in specific locations with patterned catalyst [12]. Transfer of graphene from a different substrate, followed by its patterning is also possible [13,14]. Graphene selectively grown on Ni damascene interconnect patterns on 300 mm Si wafer [15], but quality improvement is needed.
		Ability to grow/transfer high-quality graphene at low temperature	Graphene can be grown at 600°C using Co [16] and Co-Ir alloy [17] as catalytic layers. With Fe catalyst, graphene growth at 650°C was demonstrated [12]. But, the quality needs improvement. High-quality multi-layer graphene growth at 1000°C, and subsequent graphene-transfer were demonstrated [13].
		Ability to control thickness	Multi-layer graphene with a relatively uniform thickness can be obtained on an epitaxial metal catalyst [13], but further improvement is needed.
		Highly selective etch	Continued research needed to identify a dielectric etch that doesn't damage or etch the graphene.
		Defect-free contacts	Continued research needed to produce good contacts to vertical interconnects (vias) to minimize risks of resistance and local heating.
		Thermal behavior	Intrinsic graphene thermal resistance is low. Thermal interface resistance may limit performance.
		Effective resistivity	The resistivity of multi-layer graphene grown by CVD is as low as ~50 μΩcm (L). The resistivity can be as low as ~4 μΩcm by intercalation of alien molecules [14].

4.2.4. HETEROGENEOUS INTEGRATION, ASSEMBLY AND PACKAGING MATERIALS

The ERM and Heterogeneous Integration teams are in the process of prioritizing key heterogeneous integration and assembly and packaging ERM challenges, which include:

- New engineered materials: Substrate, mold, underfill, wafer bond alloys, solder alloys
- Conductors: Nanomaterials (CNT, graphene, nanowires (NWs), metals (Cu, Al, W, Ag, etc.), composites
- Dielectrics: Oxides, polymers, porous materials, composites

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- Semiconductors: Elemental (Si, Ge), Compounds (III-V, II-VI, tertiary), polymers
- Critical factors: Cost, CTE differential, thermal conductivity, fracture toughness, modulus, processing temperature, interfacial adhesion, operating temperature, and breakdown field strength

Table ERM6 provides a set of heterogeneous integration and assembly and packaging priorities for ERM.

Table ERM6 Heterogeneous Integration, Assembly and Packaging Materials

Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
Stacked chip adhesives (low power density)	Die attach materials/back side films, materials for thin packages	Low coefficient of thermal expansion (CTE) systems	Using nanoparticles, low BLTs can be achieved and by increasing their loading, CTE can be lowered, but the viscosity goes up upon addition of nanoparticles and their dispersion is difficult to control at high loadings
Stacked chip adhesives (high power density)	Better cooling solutions with low thickness	Low bond line thickness (BLT), low CTE	Reducing thermal interface resistance
Novel printable die attach adhesive	Nanoink (with either insulating particles or conductive particles depending on the application)	Adhesion, electrical properties (insulating and conductive), thermal conductivity, particle size smaller than bond line (<50% of bond line)	Adhesion, flexibility, strength
EMI shielding materials	Nanoink	Electrical conductivity	Adhesion to polymer package materials
	Graphene film (multilayer)	Adhesion	Defect free graphene, Integration
	Carbon nanotube composite or CNT paper	Ion barrier	Integration and cost
		Electrical insulation and high thermal conductivity	
Mold compound	Next generation mold compound	Need to avoid cracking in bending stresses with thin silicon, CTE between silicon and the flexible substrate and high adhesion to IC materials. Flow compatible with flip chip underfill to enable one step (UF and Mold). Undermold must be void free!!! Material must be compatible with stress requirements of thin packages.	Using nanoparticles, low CTEs can be achieved, but the viscosity goes up upon addition of nanoparticles and their dispersion is difficult to control at high loadings. In order to achieve high toughness [to withstand bending stress], filler-matrix adhesion needs to be strong (Improved Moisture Performance)
		High effective thermal conductivity	Achieving high thermal conductivity without degrading properties
3D electrical interconnects	New polymer with nanofillers	High interfacial adhesion, high fracture toughness, low CTE (between Si and substrate CTE), resistance to electromigration, low process temperature, low moisture sensitivity, stress decoupling capacity	High current capacity with reliability in the use case with low assembly cost. Thermal & thermal Mechanical Stress need to be addressed especially for κ ~<2.

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4.2.5. *Materials Challenges for Outside System Connectivity*

Table ERM7 provides a set of top Outside System Connectivity material priorities for ERM.

Table ERM7 Emerging Research Materials Needs for Outside System Connectivity

Need	*Challenge/Status*
Photonic Interconnects	Polymer Waveguide Materials that have loss <0.01 dB/cm @ 1550 nm and are compatible (not degraded) with board assembly temperatures (~250°C) (near term PCB use)
	Conventional and flexible displays; Price point; Smart and adaptive skins and structures
	Materials that "glue" the fiber in place without distortion when curing (Single Mode Photonic Connector Assembly)
	Substrate materials CTE matched to components (~4 ppm/°K) (Package related)
	Adhesives with high thermal conductivity and low modulus/CTE to absorb strain between the substrate and silicon photonic device
	Electro-Optic Modulators that have a high electro-optic coefficient and a very low thermo-optic (wavelength stability) coefficient.
RF Materials	Materials or structures to enable low electrical contact resistance in devices (FETs, BiPolars, etc.).
	Materials to shield electromagnetic interference between devices operating at multiple frequencies in smart phones (Blue Tooth, Wi-Fi, 4G and 5G) (Package Related)
	"Case" materials that are transparent to 28–70 GHz radiation for smart phones (5G)
	Materials that support Massive MIMO and 28+ GHz Active Phased Array Antenna impedance requirements with low energy losses.

4.3. Emerging Research Materials for Memory, Beyond CMOS Logic, and Alternative Information Processing

Beyond 2030, MOSFET scaling will likely become ineffective and/or very costly. As described in the Beyond CMOS chapter, completely new, non-CMOS types of memory, logic devices, and maybe even new circuit architectures are potential solutions. Such solutions ideally can be integrated onto the Si-based platform to take advantage of the established processing infrastructure, as well as being able to include Si devices such as memories onto the same chip. The following outlines key materials challenges for emerging materials for memory, beyond CMOS logic and alternative information processing.

4.3.1. *Emerging Materials for Memory*

Emerging memory devices includes capacitive memories (Fe FET), and resistive memories including ferroelectric devices, resistance change devices, devices based on Mott transitions and novel magnetic memories. Another key requirement for memory technology is the development of corresponding select devices that access only the selected memory cell of interest without perturbing non-selected cells. Table ERM8 provides a set of materials and associated challenges for emerging memory materials, and Table ERM 9 provides materials and associated challenges for memory select.

Table ERM8 Emerging Materials for Memory

Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
Ferroelectric FET	Interface Material: SiO_2 or HfAlOx	Excellent endurance	Understanding the origin of FE effect in doped HfO_2 [1]
	FE Material: HfO_2, HfO_2(Si, La, ...doped)[1],SrBi2Ta_2O_9		Depolarization field - control of charge trapping
			Memory retention time and fatigue – choice of metallic electrode
Ferroelectric tunnel junction	FEFET:$BaTiO_3$, $BiFeO_3$ (tunnel barrier)	Excellent endurance	Maintain FE domain properties in ultrathin films
			Single domain polarization

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Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
Conductive bridge RAM	Insulator: GeSe, GeS, AgS, CuS, AgSe, CuSe, Ta_2O_5; Electrode: Ag, Cu, etc. [2,3]	Scalability and nonvolatility	Scalability, stability and reliability.
ReRAM - OxRAM - Filamentary	Insulator: HfOx, TaOx, TiOx, NiO; Electrode: TaN, TiN, Ni [4,5]	Scalability and nonvolatility	Reproducible filament forming process. Scalability, stability and reliability.
ReAM - OxRAM - Nonfilamentary	Insulator: $PrCaMnO_3$, Nb:$SrTiO_3$, etc.; Electrode: Pt, $SrRuO_3$, etc. [6]	Scalability and nonvolatility	Understand the mechanisms for different materials. Integration of perovskites with CMOS process [6]. Improve data retention.
Mott memory	Complex Metal Oxides and Transition Metal Oxides: e.g. Nd1-xSrxMnO_3 and VO_2.	Scalability and nonvolatility	Determining whether the electronic transition can reversibly occur with or without the first order structural phase transition. Determining the thermal control required for reversible operation.
	Chalcogenides: AM4Q8 (A=Ga, Ge; M =V, Nb, Ta, Mo; Q= S, Se) [7,8,9,10]		Need to understand retention and scaling effects.
Novel magnetic memory	Voltage torque MRAM: FeCo, CoFeB-MgO, etc. [11–14]	Low power and high speed	Need better retention and demonstration of integration
	Spin orbit torque MRAM: Pt, β-Ta, β-W, oxygen doped W [15]		Need lower resistivity materials to lower power consumption.

Table ERM9   Emerging Materials for Memory Select

Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
Polysilicon diode	Polysilicon [1–3]	Compact 3D integration of memory with high on-off ratio	Lower crystallization temperatures to permit integration while reducing off current and contact resistance.
Oxide diode	p-NiOx/n-TiOx, p-CuOx/n-InZnOx, TiOx/Pt, Ag/n-ZnO, etc. [4–13]	Lower processing temperature and ease of integration	Improved contact resistance and density of states to improve on-off ratio
Mott switch	VO_2, $SmNiO_3$, etc. [14–15]	Good switching performance	Complex materials. Need improvements in leakage current and endurance.
Threshold switch	NbOx/Pt, AsTeGeSiN [16–21]	Good switching performance	Complex materials. Need improvements in leakage current and endurance.
Tunneling devices	Ni/TiO_2/Ni, etc. [22–25]	Lower processing temperature and ease of integration	Need improved reliability and endurance.
Mixed ionic and electronic conduction materials	Copper-containing MIEC materials [26–29]	Good switching performance	Copper accumulation failure.

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4.3.2. EMERGING MATERIALS FOR BEYOND CMOS LOGIC AND INFORMATION PROCESSING

There are generally two classes of devices/materials for beyond CMOS logic and alternative information processing. The first are those that do not involve spin or magnetism such as ferroelectric FETs, nanoelectromechanical (NEMS) switches and transistors based on the Mott effect. The second are those based on spin and magnetism that each uses a variety of materials. Table ERM10 contains materials and associated challenges for the non-spin devices. Table ERM11 maps various spin device concepts to associated materials types and Table ERM12 describes the requirements of these materials.

Table ERM10 Emerging Materials for Non-spin-based Beyond-CMOS Logic and Information Processing

Application/Need	*Emerging Material or Process Solutions*	*Potential Advantages*	*Challenges/Status*
Negative gate capacitance FET	HfO_2 doped with Zr,Al,Si, $SrTiO_3$:STO, Pb(x)Zr(1-x)TiO_3:PZT [1–5]	Step up voltage transformer leading to subthreshold swing lower than 60 mV/dec for an otherwise conventional MOSFET. Potential for integrating memory with logic and for non-von Neumann architectures.	Reduction of hysteresis while maintaining steep SS behavior. Reduction of interface states. Further understanding of the mechanism. Optimizing materials properties for scaled technology nodes.
NEMS switch	W, Ru, TiW, TiN, Poly-Si, Pt, CNTs, graphene, SiC, etc. [6–10]	Potential for zero off-state leakage and zero subthreshold swing. Inherently ambipolar. Robust temperature response. Potential for BEOL integration	Further development of refractory metals to minimize wear, stiction, materials transfer, and surface oxidation.
Mott FET	VO_2, $SmNiO_3$, $SrTiO_3$, La1-xSrx MnO_3 [11-13]	Steep subthreshold swing with low off current. Potential for non-von Neumann architectures.	Understanding phase transition mechanisms. Achieving bulk electronic phase transition. Improve material growth to achieve low defect density and high carrier mobility. Improve gate oxide and interface.

Table ERM11 Spin Devices Versus Materials

	Spin MOSFET	*Spin FET*	*Spin Wave Devices*	*Nanomagnetic Logic*	*Spin Torque Majority Gate*	*All Spin Logic*	*Out of Plane STT*
Ferromagnetic Semiconductor	Source/Drain Need Higher Tc and higher remnant magnetization	Source/Drain Need Higher Tc and higher remnant magnetization	N/A	Nanomagnets: Need higher RT remnant magnetization			
Ferromagnetic Metal	Source/Drain: Schottky or MTJ	Source/Drain	Spin Wave Channel	Nanomagnets	Free Layer: Out of plane magnetization achieved with CoFeB/MgO	Spin Wave Channel & Spin Torque Device	Achieved in CoFeB/MgO MTJs
Heusler Alloys	Source/Drain (i.e. $Co_2FeA_{l0.5}Si_{0.5}$)	Source/Drain (i.e. $Co_2FeA_{l0.5}Si_{0.5}$)					
Permanent Magnetic Materials	S/D Pinning Material	S/D Pinning Material			Fixed layer pinning	Fixed Pinning Layer	
Dielectric	Spin Tunnel Barrier: MgO, Al_2O_3, or graphene Used with FM Metals	Spin Tunnel Barrier:MgO, Al_2O_3, or graphene Used with FM Metals			Spin Tunnel Barrier: MgO, graphene; Electric field control of magnetization: CoFeB/MgO	Spin Tunnel Barrier: MgO, graphene; Electric field control of magnetization: CoFeB/MgO	Perpendicular magnetization achieved in CoFeB/MgO

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	Spin MOSFET	*Spin FET*	*Spin Wave Devices*	*Nanomagnetic Logic*	*Spin Torque Majority Gate*	*All Spin Logic*	*Out of Plane STT*
Strongly Correlated Electron Materials			Magnetoelectric Switch(I/O): Need higher ME coupling with high speed			Magnetoelectric Switch (I/O): Need higher ME coupling with high speed	
Semiconductor	Spin Channel	Spin Channel High Spin Orbit Coupled Material: InGaAs, InAs, InSb					

Table ERM12 Spin Material Requirements and Properties

Application	*Requirements*	*Ferromagnetic Metal*	*Half Metals*	*Compound Ferromagnetic Metals*	*Dilute Magnetic Semiconductor*	*Wide Bandgap Magnetic Semiconductors*
Ferromagnetic Spin Injector	High Remnant Magnetization (>400 K)	Co, Fe, Ni and alloys >50% RM 400 K	LSMO Tc=350	Cu_2MnAl, Cu_2MnSi, etc.	Ga(Mn(As) Tc 195 K	TiO_2: Co, SnO_2:Co, etc.
	High injection efficiency	Acceptable through Schottky Barrier and tunnel dielectric		Excellent below Tc	Excellent below Tc	Unknown: Low Carrier Mobility
	Resistance Mismatch	High Schottky Barrier	TBD	Low	Low	Low
	Ability to modulate magnetization with electric potential	Now achieved in CoFeB/MgO structures at 300 K		High Coupling below Tc	High Coupling below Tc	Unknown
	Mechanism	*Materials*				
Novel Spin Injectors	Dynamical Exchange Interaction	$Ni_{0.81}Fe_{0.19}$-GaAs [1]				
	Spin torque exchange with Giant Spin Hall Effect	$Co_{0.40}Fe_{0.40}B_{0.20}$(4 layers)/Ta(8 layers) [2]				
	Inverse spin hall effect to induce spin current	Pt/ $Y_3Fe_4GaO_{12}$ [3]				

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Application	*Requirements*	*Ferromagnetic Metal*	*Half Metals*	*Compound Ferromagnetic Metals*	*Dilute Magnetic Semiconductor*	*Wide Bandgap Magnetic Semiconductors*
		Oxide Dielectrics	*Other Dielectrics & Materials*	*Complex Metal Oxides*		
Spin tunnel barrier	TMR% >1000%	MgO ~ 350% @300 K (400°C Anneal) 604% @300 K (600°C Anneal) [4]	CaF_2	LSMO/LAO/ LSMO ~150% @ 10 K [6]		
			2D materials: Graphene, h-BN (TMR predicted to exceed MgO) initial experiments confirm tunneling for single layer, but need 3–5 layers to achieve high TMR — work in progress			
		Al_2O_3 ~ 1–20% @ 300 K [5]	AlN			
		Dilute Magnetic Semiconductors	*Half Metals*	*Complex Metal Oxides (MagnetoElectric)*		
Magnetoelectric Switch	High Coupling of Electric Field to Magnetization	(GaMn)N: 300 K; Saturation Magnetization=3 μemu [7]	None Reported	$BiFeO_3$:CoFe: Saturation magnetization >1000 emu/cc [8] (300ºK)		
	Operation >400 K	Voltage controlled magnetization reversal now demonstrated in CoFeB/MgO/CoFeB structures at 300 K — achieved P and AP orientation	Candidates: – Complex Metal Oxide Heterostructures (e.g. STO-LAO, etc.) – Huesler Alloys (e.g. Cu2MnAl, CuMnSi, etc.)			
		Silicon	*Graphene and CNTs*	*III-V*		
Spin Torque & Transport	Spin coherence time or length	10 microns; 100 microseconds (85 K) [9]	Graphene:2.7 ns/ 7 microns(300 K) [10] CNT >130 nm (20ºK) [11]			

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4.4. Metrology Needs and Challenges for Emerging Research Materials

Metrology is needed to characterize composition, properties, and understand structure of emerging research materials, at nanometer dimensions and below. The most difficult ERM metrology challenges would be those associated with the introduction of DSA, such as evaluating critical material properties, size and location of features, registration, and defects. Also needed are non-destructive methods for characterizing embedded materials and interfaces defects, as well as platforms that enable simultaneous measurement of complex nanoscopic properties, and modeling of probe-sample interactions. Table ERM13 summarizes the current set of continuing and prioritized metrology related ERM challenges and needs.

Table ERM13 Metrology Needs and Challenges for Emerging Research Materials

Metrology Need	*Challenges/Status*
Directed self-assembly (DSA)	For directed self-assembly (DSA) to be viable as a lithography extension or to assemble nanostructured materials in predefined locations and alignment, metrology is needed to evaluate critical material properties, the size and location of features, and the registration to previously patterned structures [1–3]. Characterization techniques are needed to evaluate neutral surfaces and the interfacial energy between the chemical surfaces and the polymers. Metrology capabilities to detect defects over large areas and under the surface are also needed. In addition, there needs to be increased focus on higher chi X materials for smaller features, and this may potentially require neutral top surfaces as well. Optical, electron and scanning probe methods [4–5] have been used in DSA metrology, but new characterization techniques should leverage a combination of physical and chemical properties.
Interfaces and embedded nano-structures	Emerging research materials will be integrated with other materials and will form interfaces which dominate nanostructured devices. Thus, understanding and control of the atomic structure, composition, bonding, defects, stress, and their effects on nanoscopic properties at these interfaces is critical. While some progress has been made towards nondestructive characterization of structural and electronic properties of buried interfaces, embedded contacts and other heterostructures using visible-ultraviolet internal photoemission [6] and scanning microwave probe methods [7,8], further progress is needed. As alternate state variables are explored for Beyond CMOS, there is a need for correlated, multimodal microscopies, and modeling of probe-specimen interactions to maximize information return from nanoscale objects and interfaces.
Characterization and imaging of nano-scale structures and composition	To enable fundamental understanding and improvement of new materials for integration into nanometer scale structures, metrology is needed to characterize the atomic structure and composition of a wide range of new complex materials, such as 2-dimensional materials such as graphene, boron nitride, meta- chalcogenides (e.g., MoS_2), etc. Nondestructive in-situ measurement methods that offer real time characterization of material nanostructure, composition and orientation, while also allowing for correlation to macro properties are also needed. Research on emerging materials could benefit from further standardization [9] of electrical characterization methodologies to enable direct comparison of the data from various laboratories.
Interconnect materials metrology	Characterization methods for thermal conductivity of nanometer scale thin films in both static and stressed conditions are needed. As the size of interconnects continues to decrease, the thickness of the Cu diffusion barriers must be reduced to minimize the impact of this layer on the interconnect resistance. Metrology and characterization capabilities are needed to determine the effectiveness of sub-2 nm novel materials in blocking the diffusion of Cu into the interlayer dielectric (ILD) and device regions. It is important to determine such variables as, the mechanisms for Cu diffusion through the barrier when they fail (i.e., pinholes vs. diffusion, etc., and diffusion coefficient, etc.), and low k-metal interface structure and bonding. For example, there is a need to understand why molybdenum (Mo)-doped Ruthenium (Ru) thin films are thermally stable up to 725°C, whereas those of a pure Ru film fail at a lower annealing temperature of 575°C [10].
	As transistor areal densities continue to increase and stacked die 3D integration schemes are considered to drive transistor densities even higher, heat dissipation through the metal interconnect is becoming an increasingly important consideration. Recent theoretical and experimental investigations have shown that the chemical bonding and detailed structures of interfaces can have a significant influence on thermal boundary resistance (TBR) [11]. Therefore, new methods for efficiently characterizing the TBR of the numerous interfaces present in low-κ/Cu interconnects are needed, as well as research to better understand how the processes influencing interface formation and chemical bonding influence TBR.
	Through substrate via (TSV) has emerged as a leading technology for 3D integration schemes. New metrology is needed to characterize TSV enabled 3D system. For example, thermally induced defect formation and growth, as well as embedded materials degradation, affect the reliability of TSV. Any metrology to study TSVs must be capable of detecting discontinuities due to defects and material distortions in otherwise electrically contiguous structures [12]. Therefore, there is also a requirement for a measurement technique that fully characterizes stress evolution in 3D interconnects and the surrounding Si [13].

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Metrology Need	*Challenges/Status*
Monolayer conformal and deterministic doping	For devices whose properties depend on the position of atoms in the channel, metrology for deterministic doping is required to confirm the presence, placement, and electronic state of individual dopants. Established continuum techniques, such as scanning probe based four-point probe, secondary ion mass spectroscopy (SIMS), and spreading resistance profiling (SRP), are still useful for characterizing ultra-shallow junctions formed by conformal doping. Ultra- shallow junction imaging techniques, i.e., scanning capacitance microscopy and scanning spreading resistance microscopy [14], are also available. Single dopants can be imaged with scanning tunneling microscopy (STM) and low-temperature frequency-modulated Kelvin force microscopy [15,16]. The STM technique, sensitivity is limited to the first 2 or 3 atomic layers. Atom probe tomography (APT) / local electron atom probe (LEAP) can provide detailed 3D atomic level images of the positions of all the atoms in the device [17,18].
Simultaneous spin and electrical measurements	Multiple emerging devices are based on control of spin as an alternate state variable including, but not limited to, spin transfer torque magnetic random access memory (STT-MRAM), nanoscale spin transistors, spin wave devices, hybrid-ferroelectric/ magnetic structures, and other spin-based logic concepts. These require metrology that depends on understanding nonlinear device dynamics, coupling, and noise. For example, metrology is needed for spin currents and transport in multilayered / heterogeneous systems.
Ultra-scaled devices	Emergent nanoscopic properties will introduce new failure mechanisms which will require trading device performance for reliability. Hence, new metrologies and models are needed to characterize the performance and reliability of emerging nano-scale devices. A thorough understanding of the sources of variability and their impact on device noise is critically needed for enabling the successful design and integration of emerging materials into nanoelectronics. This foundational need will drive the development of tools for identifying and characterizing the significant emergent sources of variability and noise in nanoscopic systems. There is a need to characterize and understand the aging of nano- materials and nanostructured devices, and the consequences of such aging on device performance since most of the existing data based on bulk material properties may not be applicable.
	The introduction of 3D device structures, requires imaging of a complex structures with atomic resolution of interfaces and chemistry. Furthermore, the integration of the newly introduced materials, such as high-k dielectrics in combination with metal-gate stack, needs careful optimization to produce excellent reliability [19] This requires imaging of a complex 3D structure with atomic resolution of interfaces and chemistry. Some progress has been made in this regard; for example, using aberration corrected electron energy-loss spectroscopy, two-dimensional elemental and valence-sensitive imaging at atomic resolution, of a La0.7Sr0.3MnO_3/$SrTiO_3$ multilayer have been demonstrated, and the data show an asymmetry between the chemical intermixing on the manganese-titanium and lanthanum-strontium sublattices [20]. For 3D interconnects, penetration of x-rays provides a major advantage to nondestructively imaging a 3D volume [21]. Strategically, segmentation of 3D data allows objective, quantitative analysis of complex structures [22]. Further research work is needed to avoid distortions due to interactions between probes and the very thin films used.

5. CROSS TEAMS

The ERM chapter incorporated valuable inputs from the following IRDS international focus teams (IFTs).

- More Moore IFT
- Beyond CMOS (BC) IFT
- Lithography IFT
- Outside connectivity (OSC) IFT
- Packaging IFT
- Metrology IFT

6. EMERGING/DISRUPTIVE CONCEPTS AND TECHNOLOGIES

As mentioned at the beginning of the chapter, new system integrators, from mobile to data centers to the Internet of Everything, have appeared with new and complex technology requirements. These application domains require a highly interdisciplinary set of expertise, e.g. electrical and mechanical engineering; as well as materials, biological, medical, energy, aerospace, transportation, communication, and sustainability sciences. The trend towards the convergence of monolithically integrated functional diversification with miniaturization manifests as increasing complexity in the road-

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mapping process. Collaborative transdisciplinary research is needed to identify materials and processes that catalyze breakthrough and convergent advances in these technologies. Initiatives that leverage the expertise of colleagues in adjacent spaces who know the local environment, e.g., biology, energy, etc., will help to drive novel approaches and more optimal materials, process, manufacturing, and performance solutions to emerging IoT challenges than can be achieved by semiconductor centric approaches. Table ERM14 identifies several emerging application opportunities that will drive and enhance future ERM working group activities.

Table ERM14 Summary of Potentially Disruptive Emerging Research Materials Application Opportunities

Convergent Opportunities	*Emerging Material, Process or Technology Need*
Mobile Communication and Information	Security; Ubiquitous and low power communication and information processing; Optical switching for routing, Monolithically integrated smart nano-composite materials for enhanced functional density; Flexible electronics
Smart Transportation	Conventional and flexible displays; Price point; Smart and adaptive skins and structures
Big Data	Security; Robust and ubiquitous information storage, access and processing; Deterministic systems; Quantum computation; Nature inspired information processing; Convergent neurosynaptic materials and systems
High performance, Sustainable, and Robust Materials, Chemistries and Manufacturing	Security; Functional DSA, Biocompatible (Healthcare/Pharma), Metamaterials, Adaptive Manufacturing; Multiple-life cycle methods
Energy Technology	Secure, low power, self-powered systems; power distribution systems; Low energy manufacturing; Integrated micro-fuel cells; integrated micro-batteries and super-capacitors
Medical/Health Care	Personalized diagnostics and ubiquitous monitoring; Prosthetics and implantable devices, with long term biotic/abiotic interfaces; Imaging [Intracellular to macroscopic]; Electronic physician and medical records; Telemedicine [HC], [HI]
Multi-functional Materials/Sensors	Convergent and monolithically integrated chemical, biological, physical, and NEMS platforms

7. Conclusions and Recommendations

The IRDS represents a strategic repositioning of the community's scope, needs, and set of emergent opportunities. In alignment with this new perspective, this edition of the ERM chapter represents a work in transition that has aligned difficult challenges with the needs of related IRDS working groups. Much of the information in the detailed tables comes from prior ERM chapters and current IRDS working groups. Future editions of ERM will provide additional detailed descriptions and continue to adapt its scope to engage with a new set of ERMs, many of which will be identified by the IRDS working groups.

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