INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

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CRYOGENIC ELECTRONICS AND QUANTUM INFORMATION PROCESSING

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ACKNOWLEDGMENTS

This report was prepared by the members of the Cryogenic Electronics and Quantum Information Processing (CEQIP) International Focus Team (IFT).

Name	Area	Organization
Cuthbert, Michael	Cryo, QIP	National Quantum Computing Centre, UK
DeBenedictis, Erik	QIP-QC	Zettaflops, USA
Fagaly, Robert L.	SCE-App	Honeywell (retired), USA
Fagas, Giorgios	QIP	Tyndall National Institute, Ireland
Febvre, Pascal	SCE-Fab	University Savoie Mont Blanc, France
Fourie, Coenrad	SCE-EDA	Stellenbosch University, South Africa
Frank, Michael	SCE-Logic, -Roadmap	Sandia National Laboratories, USA
Gupta, Deep	SCE, Cryo-Semi	SEACORP, USA
Herr, Anna	SCE-Logic, -Roadmap	IMEC, Belgium
Holmes, D. Scott [Chair]	SCE	Booz Allen Hamilton, USA
Humble, Travis	QIP-QC	Oak Ridge National Laboratory, USA
Leese de Escobar, Anna	SCE-App, SCE-Bench	Navy NIWC PAC, USA
Mueller, Peter	QIP-QC	IBM Zürich, Switzerland
Mukhanov, Oleg	QIP-QC, SCE-Logic	Seeqc, USA
Nemoto, Kae	QIP	National Institute of Informatics (NII), Japan
Papa Rao, Satyavolu	SCE-Fab, QIP	SUNY Polytechnic, USA
Pelucchi, Emanuele	QIP-QC	Tyndall National Institute, Ireland
Plourde, Britton	QIP	Syracuse University, USA
Soloviev, Igor	SCE	Lomonosov Moscow State University, Russia
Tzimpragos, George	SCE-Logic, -Metrics	U. of Michigan & UC Santa Barbara, USA
Vogelsang, Thomas	Cryo-Semi	Rambus, Inc., USA
Noboyuki Yoshikawa	SCE-Logic, -Bench	Yokohama National University, Japan
You, Lixing	SCE-Fab	SIMIT, CAS, China

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CRYOGENIC ELECTRONICS AND QUANTUM INFORMATION PROCESSING

1. INTRODUCTION

The goal of this International Roadmap for Devices and Systems (IRDS) chapter is to survey, catalog, and assess the status of technologies in the areas of cryogenic electronics and quantum information processing. Application drivers are identified for sufficiently developed technologies and application needs are mapped as a function of time against projected capabilities to identify challenges requiring research and development effort.

Cryogenic electronics (also referred to as low-temperature electronics or cold electronics) is defined by operation at cryogenic temperatures (below −150 °C or 123.15 K) and includes devices and circuits made from a variety of materials such as insulators, conductors, semiconductors, superconductors, or topological materials. Existing and emerging applications are driving development of novel cryogenic electronic technologies.

Information processing refers to the input, transmission, storage, manipulation or processing, and output of data. Information processing systems to accomplish a specific function, in general, require several different interactive layers of technology. A top-down list of these layers begins with the required application or system function, leading to system architecture, micro- or nano-architecture, circuits, devices, and materials. A fundamental unit of information (e.g., a bit) is represented by a computational state variable, for example, the position of a bead in the ancient abacus calculator or the voltage (or charge) state of a node capacitance in CMOS logic. A binary computational state variable serves as the foundation for von Neumann computational system architectures that dominated conventional computing.

Quantum information processing is different in that it uses qubits, two-state quantum-mechanical systems that can be in coherent superpositions of both states at the same time, which can have computational advantages. Measurement of a qubit in a given basis causes it to collapse to one of the basis states.

Technology categories covered in this report include:

- Superconductor electronics (SCE)
- Cryogenic semiconductor electronics (Cryo-Semi)
- Quantum information processing (QIP)

1.1. SUMMARY AND KEY POINTS

1.1.1. SUPERCONDUCTOR ELECTRONICS (SCE)

- As an emerging technology area with small current market size, important applications and technology areas do not align completely with those considered by the IRDS Application Benchmarking (AB) and Systems and Architectures (SA) teams. Applications and technology areas specific to superconductor electronics were added to improve technology roadmapping ability.
- Large-scale applications exist if the technology can overcome significant challenges.
- Logic approaches are numerous, and none is clearly scalable to larger applications.
- Memory is a weak point with less than 1 MiB currently demonstrated on a single chip.
- Roadmap status: Partial roadmaps are provided.

1.1.2. CRYOGENIC SEMICONDUCTOR ELECTRONICS (CRYO-SEMI)

- Some semiconductor electronic devices and circuits work at cryogenic temperatures without modification. Optimization of performance can require design or fabrication process modifications.
- Markets remain niche and focus on sensors or systems that must operate at cryogenic temperatures.

- Quantum computing control and readout applications are a current application driver.
- Roadmap status: Not yet ready for roadmaps.

1.1.3. QUANTUM INFORMATION PROCESSING (QIP)

- Emerging technologies with small current markets but large potential.
- Quantum computing is a key area of interest; however, several technical approaches are in competition and none has emerged as clearly scalable to useful size and capability.
- Roadmap status: Not yet ready for roadmaps, although superconducting quantum computing is close.

1.2. CROSS TEAMS

The Cryogenic Electronics and Quantum Information Processing (CEQIP) team interacts with other IRDS international focus teams.

- Application Benchmarking (AB) and Systems and Architectures (SA) provide applications and system architecture guidance.
- Outside System Connectivity (OSC) provides insight into system connectivity and interfaces with which systems covered by CEQIP will need to interact.
- Beyond CMOS (BC) provides insight into novel computation, memory, and communications approaches.
- Packaging and Integration (PI) provides insight into technologies that might be adapted for applications covered by CEQIP.

External organizations that CEQIP interacts with include the IEEE Quantum Initiative and the Quantum Economic Development Consortium (QED-C).

Historical note: In 2017, Cryogenic Electronics appeared as an emerging application within the Beyond CMOS chapter. In 2018, Cryogenic Electronics and Quantum Information Processing became an International Focus Team (IFT) responsible for preparing a separate IRDS chapter.

2. SUPERCONDUCTOR ELECTRONICS (SCE)

2.1. INTRODUCTION TO SCE

Superconductor electronics (SCE) uses circuits and components at least some of which are in the superconducting state. Some materials become superconducting below a critical temperature, T_c. Critical temperatures of known superconductors range from near absolute zero to about 203 K (–70 °C). The unique physics of superconductors, such as zero dc resistance for sufficiently small currents, allows construction of circuits that are otherwise difficult or impossible to realize. SCE applications tend to cluster in temperatures around the boiling point of liquid nitrogen (77 K, –196 °C), the boiling point of liquid helium (4.2 K, –269 °C), and the superfluid helium-4 temperature range below about 2.17 K.

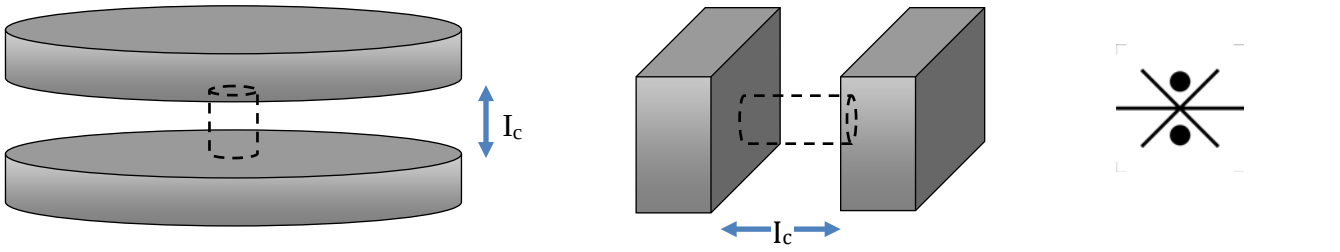
This report does not seek to explain the operation of superconductor electronic components or circuits except where necessary and consequential to technology roadmapping. Similarly, the focus is on applications that could benefit from technology roadmapping. Following is a very brief introduction. For those seeking to fill in the gaps, open access reviews of superconductor electronics can provide further information [1, 2].

Both passive (linear) and active (nonlinear) superconducting components exist. Examples of passive components are superconducting wires used as inductors, transmission lines, or resonators.

A superconducting loop with inductance L and circulating current I stores magnetic flux $\Phi = LI$. Unlike a loop made with normal, resistive material, the current can circulate for as long as it stays superconducting. The behavior is analogous to an ideal capacitor, but the loop stores magnetic flux instead of charge.

Only discrete values of magnetic flux are possible in a superconducting loop due to the quantum nature of the superconducting state. A simple description is that the superconducting state is associated with a wave function and that the superconducting phase change around a loop must be $2\pi n$, where n is the number of flux quanta in the loop. The value of the magnetic flux quantum is Φ_0 = 2.07 fWb. Expressed in practical units, 1 fWb is equivalent to 1 mA·pH or 1 mV·ps. Phase differences between points within superconductor circuits can be produced by magnetic flux, electric currents, and certain devices engineered to exhibit a strongly spatially dependent superconductor wave function. A procedure to determine the flux state in a superconducting loop is described by Fourie [3].

Josephson junctions (JJs) are active superconductor devices used for their nonlinear behavior and switching. Physically, JJs are 2-terminal devices typically made like a thin-film capacitor with superconducting plates or contacts. Common configurations are shown in Figure CEQIP-1. Quantum tunneling of Cooper pairs through the thin barrier layer allows a supercurrent to flow between the contacts with zero voltage drop. The maximum supercurrent is called the critical current, I_c.



a. Vertical orientation b. Horizontal orientation c. Electrical symbol

Figure CEQIP-1 Josephson Junction Device Structures

Superconductor electrodes are shown in gray. Contacts to other circuit elements are not shown. The space between the electrodes can be filled with an insulator, semiconductor, or metal. Dashed lines show an optional weak link, which can be made of the same material as the electrodes. Shown is the modern electrical symbol that includes two dots symbolizing a Cooper pair [4, 5].

When the current through a critically damped JJ exceeds the critical current, it switches (the superconducting phase difference across the junction jumps by 2π) and produces a single flux quantum (SFQ) output. Note that the time-dependent voltages and

currents produced by the SFQ output depend on the JJ and circuit characteristics, respectively. The switching energy $E_{sw} \sim I_c\Phi_0 = 2 \times 10^{-19}$ J = 0.2 aJ for I_c = 100 μA. Smaller values of critical current I_c are desirable for energy-efficient applications, within limits due to noise and required bit error rate or ratio (BER) [6].

Single flux quantum (SFQ) digital logic represents digital '1' and '0' by the presence, absence, polarization, or location of magnetic flux quanta within a circuit element. SFQ circuits switch magnetic flux using Josephson junctions and store flux as circulating currents in inductive loops. This is very different from semiconductor circuits, which switch electric charge using transistors and store charge in capacitors. For an explanation of how a simple SFQ gate operates, see [7]. Reviews and books provide further information [1, 8, 9, 10].

Current supplied to SCE circuits is used to both compensate for energy dissipated and to shift superconducting phase differences within the circuit, biasing operation in a desired direction. Supply current type (ac or dc) and magnitude depend on the circuit or logic family. Superconductor phase engineering is an important part of SCE circuit design without analogy in CMOS circuit design [11].

Phase shift elements set or change the superconducting phase φ between locations in a superconducting circuit. Currents through circuit elements can be used to shift the phase. The phase difference across an inductor is given by $\varphi_L = 2\pi IL/\Phi_0$, where I is the current, L is the inductance, and Φ_0 is the magnetic flux quantum. Using an inductor to provide a phase difference involves a tradeoff between current and inductance. Large inductances can require too much circuit area, whereas large dc external currents can become difficult to supply without creating magnetic fields that affect circuit operation. Other devices such as Josephson junctions have different current–phase relationships and present different tradeoffs.

2.2. Applications and Market Drivers for SCE

Few of the application areas and market drivers considered by the IRDS Systems and Architectures (SA) and Application Benchmarking (AB) teams [12, 13] are currently relevant for superconductor electronics. The reason is that cryogenic electronics must continue to serve niche and emerging markets until it can build the capability and capacity to address larger markets.

The initial list of application areas for cryogenic electronics is shown in Table CEQIP-1 along with technology areas specific to superconductor electronics. The SCE-specific technology areas were added to enable initial tracking prior to readiness for applications tracked by the SA and AB teams. The matrix of application and technology areas and market drivers shown in Table CEQIP-2. The example applications and drivers included here are preliminary and require further development. Starting points include a survey of applications and markets for superconductor electronics published in 2010 [14].

Table CEQIP-1 Initial Application and Technology Areas Considered for Superconductor Electronics (SCE)

Application or technology area	*Desired metric*	*Description*
Optimization	Solutions per second, feasible problem size	Integer NP-hard optimization problems
Media processing	Frames per second	Discrete processing, including the filtering, compressing, and decompressing of unknown streaming media
Cryptographic codec	Codons per second	Encrypting and decrypting of data at the edge of cryptographic science
Artificial intelligence	Accuracy, training and inference time and energy	Graphical dynamic moving image (movie) recognition of a class of targets (e.g., face, car). This can include neuromorphic or deep learning approaches such as DNNs.
Sensors *	Accuracy, resolution, rate	Sense physical quantities such as voltage, current, magnetic flux density, or magnetic flux gradient. Example sensors: superconducting quantum interference device (SQUID), superconducting nanowire single photon detector (SNSPD), transition edge sensor (TES), THz superconductor-insulator-superconductor (SIS) and superconducting hot electron bolometer (HEB) heterodyne detectors
Sensor array readout *	Rate, multiplexed inputs	Multiplex sensor arrays

Application or technology area	*Desired metric*	*Description*
Signal processing *	Digital clock rate, bit depth	Filters, analog to digital conversion (ADC), digital to analog conversion (DAC), digital signal processing (DSP) circuits operating either on streaming digital data or in conjunction with ADC and DAC
Digital computing *	Operations per second, energy per operation, circuit density	Digital computing using superconductor circuits
Quantum computing *	Coherence time, latency, energy per solution	Qubits, interface, error correction, and control circuits for quantum computing

* Technology areas specific to superconductor electronics

Applications can be divided into those that already require cryogenic temperatures for some part of the system and those that do not. Applications already requiring a cryogenic environment provide a much lower barrier of entry for cryogenic electronics. Examples where cryogenic environments are required include: cryogen storage and transport, superconducting magnets such as those in magnetic resonance imaging (MRI) machines and nuclear accelerators, cryogenic devices such as single photon detectors and Josephson junctions, and quantum computing. Note that Josephson junctions are key devices for superconductor electronics, metrology standards, THz detectors in radio astronomy, and for magnetic field sensors and gradiometers based on superconducting quantum interference devices (SQUIDs).

Other applications do not require cryogenic temperatures; however, use of cryogenic electronics can improve metrics such as sensitivity, resolution, or energy efficiency. Examples might include artificial intelligence, discrete event simulation, optimization, and media processing.

Following is further information about the market drivers included in Table CEQIP-2. Roadmaps will be considered to help provide the required technologies when needed by these market drivers.

Table CEQIP-2 Matrix of Application or Technology Areas and Market Drivers for SCE

Application or technology area	*Market Drivers*				
	*Measurement and calibration systems **	*Digital radio **	*Quantum computing **	*Cloud*	*Internet-of-things edge (IoTe)*
Optimization				X	
Media processing		X			X
Cryptographic codec				X	
Artificial intelligence		X		P	X
Sensors *	G	X			
Sensor array readout *	X	X			X
Signal processing *	X	G	X		X
Digital computing *	X	X	P	P	X
Quantum computing *			G		

* Technology areas specific to SCE. X: important application; G: critical gating application; P: power-sensitive application.

2.2.1. CLOUD

2.2.1.1. DIGITAL COMPUTING

Large-scale digital computing applications that require many parallel processors for high-performance computing or data centers might benefit from the energy efficiency and other potential benefits of superconductor computing [15]. While the market for digital superconductor computing could be large [7], a necessary first step is to develop small-scale systems and markets. Microprocessor units and memories are currently under development but not yet available as commercial products. Cryptocurrency mining is one application under consideration for superconductor computing as it requires relatively simple processors, limited memory, and energy efficiency [16].

2.2.1.2. ARTIFICIAL INTELLIGENCE (AI)

Artificial intelligence includes applications such as machine learning (ML). The power and energy required to train large machine learning models has been growing and could become an application area for superconductor computing. For current status, see § 2.3.5.4.

2.2.2. MEASUREMENT AND CALIBRATION SYSTEMS

Many of the systems in this section make use of quantum sensing, the use of a quantum system, quantum properties, or quantum phenomena to perform a measurement of a physical quantity [17]. Included is signal processing.

SQUID sensors utilize the Josephson and Meissner effects to create sensors that can detect magnetic flux changes at or below the $\mu\Phi_0$ level [18, 19, 20]. The use of flux transformers can allow SQUID sensors to detect field changes at the fT level. Additional circuitry can allow SQUID sensors to detect a wide variety of electromagnetic quantities [21, 22]. NanoSQUIDs, which have a flux capture area less than 1 μm^2, have high spatial resolution [20, 23, 24].

Table CEQIP-3 Typical Sensitivities of SQUID Instruments

Measurement	*Sensitivity*
Current	10^{-12} A/√Hz
Magnetic flux density	10^{-15} T/√Hz
dc voltage	10^{-14} V
dc resistance	10^{-12} Ω
Mutual or self-inductance	10^{-12} H
Magnetic moment	10^{-10} emu

A SQUID can also be used as a null detector in a cryogenic current comparator (CCC) [25] to achieve part-per-billion current resolution with < 0.1 fA/√Hz sensitivity. CCCs have applications in voltage standards (§ **2.2.2.2**), quantum Hall effect [26], and in particle accelerator beam diagnostics [27].

Superconducting quantum interference filters (SQUIFs) contain many SQUID loops with different areas in a series-parallel array [28]. SQUIFs have the potential to achieve < 0.1 fT sensitivity levels and have demonstrated >10 GHz bandwidths [29]. A combination of sub–fT/√Hz sensitivity levels and GHz bandwidths may allow SQIFs to be used a wide variety of yet to be discovered applications.

Alternatives to SQUID sensors include the superconducting quantum interference proximity transistor (SQUIPT) [30], and possibly Josephson tunnel junctions incorporating stacked structures of normal metal and ferromagnetic layers [31, 32].

Application frequency ranges vary from roughly 10^{-4} Hz to 10^5 Hz or higher [19 (Fig. 12)]. While SQUIDs can be made from either low temperature or high temperature superconductors (LTS, HTS), only LTS SQUIDs are enough sensitive to cover all applications. The bandwidth of commercially available electronics is typically dc to 100 kHz with flat frequency and flat phase response. Bandwidths of 10 MHz can be achieved by operating in an open loop configuration where the maximum signal does not exceed $\Phi_0/2$.

While laboratory applications of SQUIDs have been the springboard for significant commercial successes in the areas of biomagnetism, magnetic property measurement systems, and geophysics, the commercial market for laboratory systems is

typically at the 2 to 3 million USD level [33]. One potential use of SQUIDs with a significant commercial application is in the detection of low-field MRI signals [34].

Photon detectors such as superconducting nanowire single photon detectors (SNSPDs) have applications in quantum optics and quantum communication, primarily because of their low timing jitter and capability to detect individual low-energy photons with high quantum efficiency [35, 36, 37]. Josephson junctions can also function as single photon detectors [38].

2.2.2.1. BIOMAGNETISM AND MEDICAL MEASUREMENTS

The sensitivity of SQUIDs has allowed non-invasive measurements of electrophysiological activity that has led to the development of number of medical instruments [21]. The major use, responsible for over half a billion USD in sales to date, has been magnetoencephalography (MEG) for magnetic source imaging (e.g., focal epilepsy regions). Another area where SQUID-based methodologies offer diagnostic capabilities is magnetocardiography (MCG), particularly in fetal MCG to diagnose fetal heart rhythm abnormalities. Other uses of SQUID biomagnetometers include magnetoenterography (measurements of the stomach and intestines), magnetopneumography (magnetic remnance measurements of the lung), and magnetomyography and magnetoneurography (muscle and peripheral nerve studies). One disadvantage of ultra-sensitive SQUID biomagnetometers is the need for magnetically shielded rooms to reduce the effects of external electromagnetic noise.

The major drivers in the adoption of medical instrumentation are clinical acceptance, cost and safety. Clinical acceptance requires the demonstration of superior, rather than incremental, diagnostic capabilities in a modality that the physician can easily interpret. Medical equipment costing above 1 million USD is limited to medium to large hospitals. When instrument prices drop to the 250,000 USD level, the potential market expands to small hospital and medium to large clinics. Currently the per channel cost for high channel count SQUID biomagnetometers (e.g., MEG) is at or above a few thousand USD. Significant reductions in per channel cost or eliminating the need for expensive magnetically shielded rooms could significantly increase the market for SQUID biomagnetometers.

Improvements in high-temperature SQUID sensors, which are currently more expensive than low-temperature SQUID sensors, could also reduce the cryogenic requirements with a subsequent reduction in system cost.

2.2.2.2. VOLTAGE STANDARDS

Voltage standard systems based on superconducting Josephson junction arrays became commercially available in 1996 and have continued development [39, 40]. An economic impact assessment of NIST's Josephson volt program performed in 2001 found a net present value of 45 million USD in the year 2000 [41]. At least 16 Josephson voltage standard systems were in operation in the United States at that time. Current information is needed about markets and market drivers for voltage standard systems.

Two complementary types of Josephson voltage standards used today are the programmable Josephson voltage standard (PJVS) and the Josephson arbitrary waveform synthesizer (JAWS, also known as the ac Josephson voltage standard or ACJVS) [40]. The main dc application for PJVS systems is the direct calibration of secondary voltage standards. With the 2019 redefinition of base units in the International System of Units (SI), both PJVS and JAWS systems will become key components for the direct realization of the unit volt.

The push to improve ac voltage standards is presently a driver for cryogenic circuit development [42, 43]. One reason is that the output voltage of a JAWS is limited by the number of Josephson junctions (JJs) that can be driven by a single pulse-generator channel. In one paper [43] the number of JJs driven by one generator channel was doubled to 51,200.

2.2.2.3. MAGNETIC PROPERTY MEASUREMENT SYSTEMS

Since the discovery of high-temperature superconductors, SQUID based susceptometers have been a mainstay in magnetic property measurements. Gradient detection coils surround the sample region of a variable temperature (typically 1.8 to 400+ K) insert. Surrounding the detection coils is a moderately high-homogeneity (100 ppm) superconducting magnet (0 to 9 T). The sample is moved inside the detection coils, and the resulting changes in flux are used to calculate the magnetic moment of the sample. Some systems have both axial and transverse coils. AC susceptibility can be measured by adding ac coils, although the applied fields are much smaller (μT). The dynamic range can vary from 10^{-8} to 2 emu. To date, over 1,300 SQUID susceptometers (from all suppliers) have been delivered generating over 250 million USD in revenues. Commercially available since the late 1970s, this market segment is the premier example that needed a SQUID-based product in quantity. Commercial manufacturers include Quantum Design and Cryogenic, Ltd.

The variable temperature platform can be expanded (without SQUID detection coils) to a variable temperature physical property measurement system allowing a wide variety of measurements to be taken from 50 mK to 800 K in fields exceeding 14 T. The variable temperature susceptometer concept can be converted to remnant field geophysical measurements (§ **2.2.2.5**)

by removing the dc superconducting magnet and placing three orthogonal detection coils in a magnetically shielded region. Typically placed in a horizontal orientation, nearly 150 systems have been delivered generating nearly 30 million USD in revenues. Commercial manufacturers include 2-G Enterprises and Tristan Technologies.

Nondestructive evaluation (NDE) systems using SQUID sensors have been reviewed by [44].

2.2.2.4. MICROSCOPY

Microscopes with SQUID or magnetic tunnel junction sensors image surface magnetic flux density with micrometer-scale resolution [45, 46, 47, 48]. Recent developments include a vector-scanning SQUID microscope [49, 50] and a system for investigation of geological samples [51]. Commercial manufacturers include Neocera Magma [52] and Tristan Technologies [53].

2.2.2.5. GEOPHYSICS

Magnetic field gradiometers are used to prospect for magnetic ores [21]. The value of ore deposits discovered is reported to be several billion USD, however, the cost of the cryogenic electronics is a tiny fraction of that amount. These systems require only a few Josephson junctions and can use high-temperature superconductors operating at liquid nitrogen temperatures (~77 K). A survey of applications affecting the environment found additional applications such as the detection of unexploded ordinance (UXO) [54].

2.2.2.6. ASTRONOMY

Radio and Infrared Astronomy has played an essential historical role in superconductor electronics by pulling the developments of sensitive quantum-limited superconducting SIS and HEB heterodyne detectors for millimeter, then submillimeter/THz radio telescopes and infrared telescopes like the Herschel Space Observatory or the Planck satellite. Some astronomy applications using cryogenic sensor arrays [55, 56] are growing in array size to the point that multiplexing and signal processing is needed close to the sensors. The need to go from single pixel detection at THz frequencies to array sensors with thousands or more pixels also exists for THz detectors but suffers currently from technological limitations of back-end processing.

2.2.3. COMMUNICATIONS

Developed communications applications are covered in the following sub-sections. Proposed communication applications include chaos encryption using a circuit with a Josephson junction in parallel with a memristor [57].

2.2.3.1. WIRELESS COMMUNICATIONS

High-temperature superconductor (HTS) filters are used in wireless base stations to increase base station coverage area and data throughput. Superconductor Technologies Inc. has products that operate in over 10,000 base stations [58].

2.2.3.2. DIGITAL RADIO

Software-defined radios perform signal processing entirely in the digital domain. By contrast, traditional radios perform signal processing in the analog domain at a single frequency. Software-defined radios require both ultra-high-speed analog-to-digital converters (ADCs) and equally fast digital signal processing (DSP) of the converted signals, but do not require much memory. ADC and DSP circuits based on superconductor electronics have been demonstrated at speeds up to 40 GHz [59]. The commercial digital-RF receiver manufactured by HYPRES [60] performs ADC and DSP using superconductor electronics [61]. The superconducting components operate at about 4 K with a fully automated and cryogen-free refrigeration system. The application space extends beyond communications to many other uses of the radio frequency spectrum for surveillance, navigation, and spectrum management.

2.2.4. QUANTUM COMPUTING: CONTROL AND READOUT

Quantum computing systems operating at cryogenic temperatures below 10 K can benefit from local control and readout. Advantages include less energy dissipation in the cryogenic space and faster response times for control. Overviews of the needs are given in [744, 777, 793, 815]. The need for superconductor electronic control and readout is expected to grow with the scale of the quantum computer supported. The need for superconductors increases for systems requiring temperatures in the millikelvin range and decreases greatly for systems not requiring temperatures below about 10 K.

Current status is covered in section **2.3.5.5** and related applications of cryogenic CMOS are covered in section **3.3.3.2**.

2.3. PRESENT STATUS FOR SCE

The integrated circuit chip with the largest Josephson junction count is the 2020 D-Wave Pegasus P16 quantum annealing processor with 1,030,000 Josephson junctions [62, 746, 747]. Considering that state-of-the-art CMOS wafer-scale chips are available with more than a trillion transistors [63], superconductor electronics is still far behind the semiconductor industry in key metrics such as integrated circuit density and complexity. Prospects remain for higher operating speeds and improved energy efficiency, especially for applications requiring operation at cryogenic temperatures.

2.3.1. LOGIC

Several SCE digital logic families and some important characteristics are summarized in Table CEQIP-4 and further described in subsections below. Characteristics include:

- **SFQ count per logical '1' or per time interval**: Most of the logic families transfer one or more single flux quanta (SFQ) to communicate state values between gates. By contrast, quantum flux parametrons (QFP) use currents between gates.
- **Power type**: DC or AC.
- **Static power**: Qualitative indicator of static power dissipation.
- **Dynamic power per switch**: Power dissipated per switching device operating at frequency *f*.
- **Transformers**: **P** for power transformer usage and **G** for logic gate transformer usage.
- **Clocked gates**: Use of logic gates that require clocking. Logic depth is defined as the maximum number of logic operations between two subsequent clocked resources, such as a DFF in CMOS or any logic gate in RSFQ. Logic families with only clocked (synchronous) gates are limited to a logic depth of one, whereas unclocked (asynchronous) gates allow greater logic depths.
- **JJ count $\log_{10}(n)$**: Josephson junction or switching device count n in largest circuit demonstrated and displayed as $\log_{10}(n)$. Values in parenthesis () are designs only.

To be identified are additional parameters for future logic family monitoring and comparison. Candidates include average number of junctions or other resources per logic gate (e.g., area, number of layers), energy per operation, or overhead for clock and power supply.

Table CEQIP-4 Superconductor Digital Logic Families

Name	*Section §*	*SFQ*	*Power*	*Static Power*	*Dynamic power per switch*	*Trans-formers*	*Clocked Gates*	*JJ count $log_{10}(n)$*
RSFQ: rapid single flux quantum	**2.3.1.1**	1	– DC	High	$\alpha I_c \Phi_0 f$	-	Yes	4.4
LR-RSFQ: inductor-resistor RSFQ	**2.3.1.1**	1	– DC	Low	$\alpha I_c \Phi_0 f$	-	Yes	1.6
LV-RSFQ: low-voltage RSFQ	**2.3.1.1**	1	– DC	Low	$\alpha I_c \Phi_0 f$	-	Yes	3.7
ERSFQ: energy-efficient RSFQ	**2.3.1.2**	1	– DC	0 *	$I_b \Phi_0 f$	-	Yes	3.8
eSFQ: efficient SFQ	**2.3.1.2**	1	– DC	0 *	$I_b \Phi_0 f$	-	Yes	3.4
Self-timed SFQ	Error! Reference source not found.	1	– DC					2.8
DSFQ: dynamic SFQ	**2.3.1.4**	1	– DC	‡	‡	-	Some	0.7
TSFQ: temporal SFQ	**2.3.1.5**	1	– DC			-	No	(2.8)
xSFQ: alternating SFQ	**2.3.1.6**	2	– DC	‡	‡	-	No	
nTron: nanowire cryotron	**2.3.1.7**	1	– DC	~0	varies	-	Yes	1.5
hTron: heater-cryotron nanowire	**2.3.1.7**	1	– DC	~0	varies	-	Yes	1.2
HFQ: half flux quantum	**2.3.1.8**	0.5	– DC	Low		-	Yes	1.2
SFQ-AC: AC-powered SFQ	**2.3.1.9**	1	~ AC	‡	‡	P	Yes	5.9
RQL: reciprocal quantum logic	**2.3.1.10**	2	~ AC	~0	$\alpha I_c \Phi_0 f$ 2/3	P, G	Some	4.9
PML: phase mode logic	**2.3.1.10**	1	~ AC	~0	$\alpha I_c \Phi_0 f$ /3	P, G	Some	
AQFP: adiabatic quantum flux parametron	**2.3.1.11**	-	~ AC	~0	$\alpha I_c \Phi_0 2 f \tau_{sw}/\tau_x$	P, G	Yes	4.3
RQFP: reversible QFP	**2.3.1.12**	-	~ AC	~0	$\alpha I_c \Phi_0 2 f \tau_{sw}/\tau_x$	P, G	Yes	1.4

SFQ : count per logical '1'; JJ count : Josephson junction or switching device count in largest circuit demonstrated as $\log_{10}$(n); α : activity factor (fraction of JJs that switch in a clock cycle); I_c : average critical current; I_b : bias current; τ_{sw} : intrinsic switching time; τ_x : excitation rise/fall time; * : for I_b within the energy-efficient range; ‡ depends on whether powered like RSFQ or ERSFQ, with some additional loss in reset resistors

Gate set scaling trends are tracked in Table CEQIP-5. This report includes AQFP (MAJ+INV) and CMOS (NAND2) gate sets.

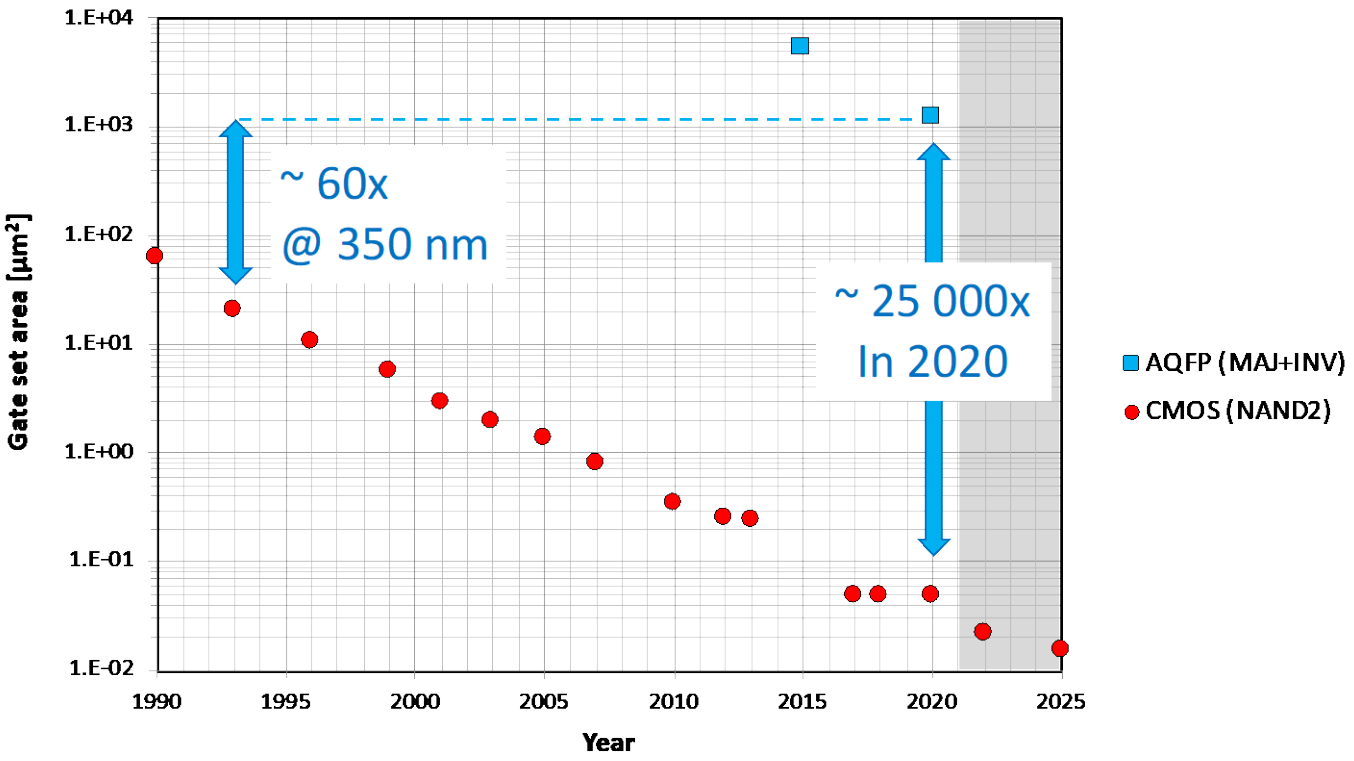


Figure CEQIP-2 Gate Set Scaling Trends

Note: The difference in gate set areas was a factor of about 25,000 in 2020 and about 60 when comparing gate sets at an equivalent feature size of 350 nm.

Table CEQIP-5 Gate Sets for SCE

2.3.1.1. RSFQ, LR-RSFQ, LV-RSFQ Logic

Single flux quantum (SFQ) digital logic was introduced in section **2.1**. Ordinary SFQ logic gates behave like state machines and require a clock signal to both logically evaluate and reset the gate. Such explicit use of clock signals in logic networks creates significant challenges with the application of the register transfer level (RTL) design paradigm, a cornerstone of VLSI digital design methodology. RTL subdivides large digital circuits into clocked registers and clock-free, state-free logic networks called combinational logic clouds. Specialized tools are required when most logic gates require clocking.

RSFQ: Rapid single flux quantum circuits use resistors to distribute dc supply currents (power) [64]. While the use of resistors simplifies superconducting circuit design and provides steady current supply, the static power dissipated is typically between 10 and 100 times the dynamic power [65].

Status: Several large-scale RSFQ integrated circuits have been demonstrated at high clock frequencies around 50 GHz, which include 8-bit microprocessors with memory [66, 67], single-precision floating-point units [68], FFT processors [69], and reconfigurable data paths [70]. An 8-bit ALU fabricated using the Nb 9-layer, 100 $\mu A/\mu m^2$ process had a computational efficiency of 40 TOPS/W [71]. An 8x8 bit multiplier with 20,251 JJs operated up to 48 GHz [72]. An 8-bit-wide, bit-parallel datapath composed of an arithmetic logic unit and register files operated up to 64 GHz [73].

LR-RSFQ: Inductor-resistor (LR) SFQ can reduce static power consumption to the same order as the dynamic power consumption through optimization of the circuit parameters in the current supply network [74, 75].

LV-RSFQ: Low-voltage operation of RSFQ circuits can improve energy efficiency [6, 76, 77] and can be implemented without shunt resistors for further energy and area savings [78]. An 8-bit ALU has been demonstrated at 30 GHz with energy

efficiency greater than 100 TOp/J [79]. A bit-parallel multiplier operated at 54 GHz [80]. Shift register operation at 83 GHz clock frequency was demonstrated using a 200 μA/μm^2 JJ process [81].

2.3.1.2. ERSFQ, eSFQ Logic

ERSFQ: Energy efficient RSFQ gates are similar to those in RSFQ, which reduces the work required to switch between these logic families. The main difference is that dc supply current (power) is distributed using a current-limiting Josephson junction in series with a large bias inductor as well as a clocked feeding Josephson transmission line (FJTL) to maintain adequate bias voltage and current stability [10, 65, 82, 83, 84]. Power distribution for energy-efficient operation adds about 30% to ERSFQ circuit area [85].

Status: ERSFQ has been used to make 8-bit parallel adders with 560 and 1360 JJs [86], a decoder for RAM [87], an 8-bit ALU [88], and fast parallel counters [89]. Proposed is a superconducting magnetic FPGA based on ERSFQ logic [90].

eSFQ: Efficient SFQ biasing networks are designed so that in each clock period the superconducting phase at all bias injection points goes through the same change [65, 91, 92]. Smaller bias inductors are required than for ERSFQ, however the gates must be designed differently, which limits compatibility with and reuse of RSFQ circuit designs.

Status: Demonstrations of eSFQ include asynchronous [93, 94] and wave-pipelined circuits [92]. The largest eSFQ circuit demonstrated is a 4 bit ALU with 2,569 JJs [94].

2.3.1.3. Self-timed SFQ

In the above-described SFQ approaches, logic gates are clocked. Traditionally, a clock tree is used to route a clock signal to each gate. Self-timing schemes, in which the clock is locally generated by the incoming data pulses, are a way to avoid clock trees without requiring development of clock-free gates. Proposed self-timing approaches include Data-Driven Self Timed (DDST) RSFQ, Dual-Rail RSFQ (DRRSFQ), RSFQ Asynchronous Timing (RSFQ-AT), and Delay Insensitive Dual-Rail (DI) RSFQ [95]. Demonstrated circuits include asynchronous eSFQ toggle flip-flops [93] and dual-rail eSFQ [94]. Proposed applications include asynchronous clock distribution networks [96].

Another way to eliminate clocking, this time without the need to create explicit clock, is by repurposing existing cells. This repurposing may happen by routing one of the data inputs to the clock port of the synchronous components. One such case is the recently proposed "clockless" RSFQ approach, where synchronous NDRO cells and delay elements are used to realize AND and NIMPLY functions [97]. These functions have been used in conjunction with synchronous components to construct a 4-bit carry look-ahead adder (CLA) and a 32-bit arithmetic logic unit (ALU) [98]. Note that although a clock signal may no longer be needed, the resulting system is prone to metastability and requires careful attention to timing.

2.3.1.4. Dynamic SFQ

DSFQ: Dynamic SFQ gates self reset using a nonlinear resistive leakage circuit that allows the usable hold time to be a large fraction of the self-reset time [99, 100]. For clocked SFQ gates, the clock signal both logically evaluates and resets the gate. The self-timed approaches presented in 2.3.1.3 avoid using a clock for gate evaluation but use just one of the inputs to reset, which leads to a risk of metastability. DSFQ gate inputs are functionally equivalent, which minimizes timing concerns. Additional benefits could come from DSFQ majority gates [101]. A challenge is that self-reset times can be sensitive to fabrication variations, especially for longer reset times. Partial path balancing can provide benefits without the need for longer self-reset times [102].

2.3.1.5. Temporal SFQ (TSFQ)

Computational temporal logic represents information in the time domain, for example as time between pulses or as delay lengths. A set of basic temporal logic operations—First Arrival, Last Arrival, Delay, and Inhibit—replaces Boolean logic operations such as OR, AND, and NOT [103, 104]. These temporal logic operators do not use binary inputs so there is no need to translate the presence or absence of data pulses to True or False statements as in Boolean logic. A consequence is that no clocking is required at the gate level. Resetting of TSFQ logic gates is required and can be performed using the same leakage techniques as in DSFQ. The set of temporal logic operators is functionally complete over natural numbers [105]. In other words, any arbitrary function that operates over non-negative integers is implementable.

2.3.1.6. Alternating SFQ (xSFQ)

xSFQ: Alternating SFQ leverages a duality between Boolean and temporal operators to repurpose the asynchronous First Arrival and Last Arrival TSFQ cells to realize Boolean OR and AND functions [106]. To achieve completeness, xSFQ relies on the theory of unordered codes, such as dual-rail codes, under which AND and OR alone are sufficient. To eliminate the need for external signals or leakage mechanisms for resetting, an alternating encoding is used. Clock-free combinational logic elements

are sandwiched between banks of storage elements. Potential advantages include significant reductions in clock networks and greater ability to use EDA tools developed for conventional CMOS circuits.

2.3.1.7. NANO-CRYOTRON LOGIC

Nano-cryotrons are multi-terminal devices, typically with three or four terminals. For device structure, see Figure CEQIP-4h. Logic based on nano-cryotrons is under active development [107, 108, 109, 110, 111, 112, 113, 114].

2.3.1.8. HFQ: HALF FLUX QUANTUM LOGIC

Half flux quantum circuits produce, transfer, and store half flux quanta [115]. Recall that single flux quantum (SFQ) circuits use Josephson junctions called 0-JJs with a current-phase relationship $I = I_C \sin(\varphi)$. HFQ circuits can be constructed from combinations of 0-JJs and either pi-JJs or 2φ-JJs. Pi-JJs have a current-phase relationship $I = I_C \sin(\varphi - \pi) = -I_C \sin(\varphi)$ and 2φ-JJs have a current-phase relationship $I = I_C \sin(2\varphi)$. HFQ circuits require little additional inductance, so should have scaling advantages [116, 117, 118].

LV-HFQ: Low-voltage, half flux quantum circuits incorporate pi-JJs in LV-RSFQ circuits and are expected to further improve energy efficiency, circuit density, and operating margins [115].

Interfaces between SFQ and HFQ circuits have been demonstrated [119].

2.3.1.9. SFQ-AC

AC-powered SFQ uses transformers in series to provide current to cells. Cells using AC bias require only a transformer; however, transformers do not scale well at feature sizes much below 1 μm. Cells requiring DC bias can be supplied by AC/DC converters [120, 121] or AC/SFQ converters [122]. Both AC/DC and AC/SFQ converters require additional circuit overhead. For best energy efficiency, the AC frequency should be greater than the clock frequency of the DC cells. Current supply to the chip can be decreased by a factor roughly equal to the biased cell count divided by the number of parallel AC supply lines on the chip.

SFQ-AC works best when most cells use AC or no bias current. A challenge is that few such cells exist, so more need to be developed.

2.3.1.10. RQL AND PML

Reciprocal quantum logic (RQL) [123, 124, 125] and phase mode logic (PML) [126] are related logic families. RQL encodes a digital 1 using two flux quanta of opposite sense and corresponds to wave pipeline operation. PML encodes digital data as high and low states of the superconducting phase, which dissipates less dynamic power. Both use energy-efficient ac resonator-based distribution for power and clock signals. The power is applied in parallel providing scalability to VLSI. Resonators also provide clock stability with zero jitter and skew. Both RQL and PML include combinational gates that allow 12 levels of logic per pipeline stage at 10 GHz. RQL and PML logic provide component-efficient superconducting gates with the same number of junctions as transistors in CMOS gates as well as full compatibility with standard RTL based synthesis design flow. Advantages include low error rates as the effective critical current of Josephson junctions in distributed networks of comparator-free RQL logic is about three times that of a single junction [127].

Design achievements include tile-based physical design to facilitate automated layout, mitigation of flux trapping, and a resonant clock network for chip-level power distribution with 50% power efficiency. A complete RTL-to-GDSII automated design flow has been developed and used to design a 16-bit CPU [128]. Circuit demonstrations include individual logic gates with a 7 dB clock margin; 3.5 GHz resonator powering a shift register with 72,800 JJs and 4 dB clock margin [129]; 16-bit ALU and 16-bit register file [130]; 0.25 MJJ resonator-based yield vehicle; and an 8-bit CPU with fully functional debug logic, register file, 8-bit CLA, and performance of write and read memory instructions [131].

2.3.1.11. QFP: QUANTUM FLUX PARAMETRON LOGIC

Adiabatic quantum flux parametron (AQFP) logic achieves extremely high energy efficiency by changing the potential shape adiabatically between double-well and single-well during switching [10, 132, 133]. Unlike SFQ logic families, current polarity and magnitude communicate state values between gates. Other distinguishing features include the use of AC power and current transformers. The typical switching energy is about 4.3×10^{-22} J at 5 GHz clock frequency assuming unshunted junctions with critical current density of 100 μA/μm^2 [134]. Determining the energy dissipation of an AQFP logic gate requires accounting for the data-dependent interactions between the gate and its environment [135]. The switching energy can be further decreased in proportion to the clock frequency and perhaps even below the Landauer thermal limit by using reversible quantum-flux-parametron (RQFP) gates (§ 2.3.1.12).

Operation at high frequencies with low bit energy and low bit error rate or ratio (BER) was confirmed experimentally [136, 137]. Multi-excitation circuits (ME-AQFP) can multiply the excitation current frequency, which typically has a maximum of about 5 GHz, by a factor of 2 or 4 to allow AQFP circuit operation up to about 20 GHz [138]. AQFP logic circuits are typically clocked by four-phase AC clocks; therefore, the logic depth per clock cycle is four. Delay-line clocking can increase both the number of phases and logic depth, possibly exceeding a clock depth of 20 for a 5 GHz clock frequency and 100 $\mu A/\mu m^2$ junction process [139, 140, 141]. Other low-latency excitation schemes have been proposed based on microwave power dividers [142] and n-phase clocking [143].

Digital logic AQFP circuit design uses a standard cell design approach with similarities to CMOS circuit design [144]. An AQFP NAND gate requires 6 junctions, whereas the corresponding CMOS gate uses 4 transistors. Transformers for supply and signal currents also add area and are difficult to scale to small sizes. Because a majority gate is a fundamental logic gate in AQFP logic, majority-based logic synthesis is desirable [145]. Several circuits have been designed and demonstrated by using an automated top-down design flow, which includes logic synthesis, and placement and routing [146, 147]. Functional operation has been demonstrated for 8-bit carry-lookahead (CLA) adders [148, 149] and 16-word, 1-bit register files [150]. An 8-bit CLA was demonstrated with energy dissipation of only 1.5 aJ per operation, or $24k_BT$ per junction switching [151]. The demonstrated MANA 4-bit AQFP microprocessor with 21,460 junctions is estimated to dissipate about 30 aJ/op at 5 GHz [152].

Directly coupled quantum-flux-parametron (DQFP) is an adiabatic superconductor logic that does not require signal transformers [153, 154]. While AC power transformers are still required, the nearly 40% reduction in gate area is significant. AQFP with π Josephson junctions also can operate without using signal transformers [155].

2.3.1.12. Reversible Logic Styles

There has been a long history of efforts to develop superconducting logic styles capable of approaching (logically and physically) reversible computation, starting with Likharev's work on parametric quantrons (PQ) in the 1970s [156], and reversible versions of the original 1987 quantum flux parametron (QFP) of Goto *et al.* [157]. These early efforts relied on adiabatic transformation of the potential energy function in one or more coupled SQUID loops, a theme which continues today in the recent work on negative mutual-inductance SQUIDs (nSQUIDs) [158, 159] and on reversible quantum flux parametron (RQFP) logic [160, 161, 162, 163, 164, 165], a variation on AQFP logic. In addition, several groups have investigated alternative *ballistic* styles of superconducting reversible logic, including groups in Hokkaido in 2008 [166, 167], Northrop Grumman in 2010 [168], the University of Maryland, [169, 170], and Sandia National Laboratories [171, 172, 173]. These efforts aim to surpass the energy efficiency of the existing irreversible logic styles such as those in Table CEQIP-4 and can potentially eventually push beyond the Landauer limit of ~kT energy dissipation per operation that applies to irreversible logic.

2.3.1.13. Quantum Phase-Slip Junction (QPSJ) Logic

Quantum phase slip junctions (QPSJ) are superconductor nanowire devices with a nonlinear I-V characteristic. QPSJs are a dual to Josephson junction devices, with the roles of phase and charge interchanged as well as current and voltage [174, 175, 176, 177, 178, 179, 180, 181, 182]. Adiabatic logic circuits based on quantum charge parametrons could be made from QPSJs [183]. Needed is demonstration of QPSJ-based circuits with at least 100 junctions to allow evaluation of their viability for complex applications.

2.3.1.14. Other SCE Logic

Spintronic superconductor electronics is a new field since about the year 2000. Like traditional spintronics, the approach is to utilize spin currents for information processing. Contrary to charge current, spin current does not conserve and is not always accompanied by charge transfer, so might be more energy efficient. Reviews of superconductor spintronics include [184, 185, 186, 187, 188]. This new field is at the stage of development and demonstration of device concepts rather than production. It is not easy to produce spin superconducting currents; however, when produced, they persist in superconductors much better in both equilibrium [189] and nonequilibrium transport [190, 191, 192]. The use of spin currents to switch memory devices is covered in § **2.3.2.2**.

Other superconductor logic families include those based on Josephson junction oscillators [193], and control of magnetic flux quanta using magnetic fields [194].

2.3.2. Memory

Superconductor electronic memory can be classified by memory device technology: 1) Josephson junction logic circuits, 2) magnetic devices, or 3) nanowire superconductor devices; and by use: (a) register, (b) cache, or (c) main memory.

The magnetic flux in a superconducting loop in steady state is quantized and thus can be used to provide the physical basis for a digital memory element. The absence or presence of a flux quantum in the loop represents binary ‘0’ or ‘1’. Superconducting memory cells have one or more Josephson junctions or nanowire superconductor devices in the loop to control and sense the number or location of flux quanta present.

For reviews, see [9 § “16.7 Memory for Cryogenic Supercomputer”, 195, 196].

Table CEQIP-6 Superconductor Memory Status

Name	*References*	*RAM*	*Bit Cell Area [μm^2]*	*Latency [ns]*		*Energy [fJ]*		*Static Power*	*Bits*
				Read	*Write*	*Read*	*Write*		
SR: shift register, ac-biased	[121]		300 (15×20)						202 280
SR: shift register	[339]			0.02	0.02	0.1	0.1	0.2 mW	64
VTM: vortex transition memory	[203 (VT2)]	✓	99 (9×11)	0.10	0.10	100	100		72
JJ-RAM: Josephson junction RAM	[199]	✓	484 (22×22)					4.5 mW	4096
RQL-RAM: reciprocal quantum logic	[200]	✓	1452 (33×44)						1024
PRAM: PTL-RAM	[201, 202]	✓	1452 (33×44)						512
SHE-MTJ: Spin Hall effect magnetic tunnel junction	[239]	✓	2470 (38×65)	0.10	2	1000	8000		16
SNM: superconducting nanowire memory	[107]	✓	26.5 (5×5.3)	0.10	3	10	10		8
Hybrid: JJ-CMOS	[659]	✓		2 ~ 4	2 ~ 4	100	100		65 536

2.3.2.1. JJ MEMORY

Shift registers consist of a series of bit cells that must be read or written in sequence. Applying a clock signal to the array of cells causes the data stored in each cell to shift to the next cell downstream. Examples of shift registers using SFQ logic include [120, 197, 339].

Random-access memory allows reading and writing of bits in any order. The largest demonstrated superconducting random-access memory (RAM) is only 4 Kibit (4096 bits) [198, 199].

RQL-RAM uses pure RQL logic and is under development by Northrop Grumman [200, 201, 202]. The unit cell consists of three RQL gates, including a single NDRO gate for state and readout and two gates to implement the multiplexer. A variant called PRAM combines NDRO storage with a SQUID-based readout multiplexer. Both RQL-RAM and PRAM read and write in a single clock cycle. PRAM is expected to achieve better density, speed, and power than RQL-RAM at sizes greater than 2 Kibit. RQL-RAM has been demonstrated as 128 bit (8×16) and 1024 bit (64×16) arrays [200]. PRAM with 44 μm × 33 μm bit cells has been demonstrated as a complete array (drivers, unit cells, sense amps) of 512 bits (16×32) [202]. The read path shared by JMRAM and PRAM has been demonstrated as a 16×32 array (decoders, drivers, unit cells, sense amplifiers, and test wrappers).

SFQ vortex transitional (VT) memory cells have been designed with sizes as small as 9 μm × 11 μm, fabricated in arrays using the MIT LL SFQ5ee process, and successfully demonstrated [203]. This demonstration was not a complete RAM as addressing and readout circuits were not included on the chip.

Lookup tables (LUT) have been demonstrated with 4 bits and designed with 16 bits using RSFQ circuits [204]. Multi-fluxon memory cells might allow increased storage density with an acceptable increase in circuit complexity [205].

A memory cell with 3 conventional Josephson junctions (0-junctions) and a Nb/PdNi/Nb magnetic junction (π-junction) has been demonstrated [206]. The π-junction eliminates the need to provide bias current to the memory cell. Bipolar SFQ pulse trains sent over a passive transmission line are intended to perform read and write operations. Optimization of the memory cell is required for use in arrays.

2.3.2.2. MAGNETIC MEMORY

Magnetic materials affect nearby superconductors and layers with aligned magnetizations have a stronger effect. The effects can be used for superconductor logic as covered in § **2.3.1.13**. Here the concern is only memory devices. One method to make a memory element uses two magnetic layers, one that can be switched (free) in direction and a second that is magnetically hard and serves as an unswitched reference. Switching the free layer so the two layers are either parallel or antiparallel changes the effect on nearby superconductors and can be read as memory states '0' and '1'. Magnetic memory devices for SCE have similarities to magnetoresistive RAM (MRAM) developed for conventional electronics, however, there are also significant differences. Several types of magnetic memory devices for superconductor electronics are shown in Figure CEQIP-3.

Memory cells can be based on changes in magnetic memory device (i) Josephson critical current [207], or (ii) superconducting phase difference in the ground state [8].

2.3.2.2.1. SUPERCONDUCTING SPIN VALVES (SSV)

Figure CEQIP-3a shows an example device structure. Two magnetic layers affect a single superconductive layer, changing the superconducting critical current. A similar device type with only one magnetic layer containing multiple domains works by changing the degree of domain alignment.

Status: Superconducting spin valves with magnetic control of superconducting critical temperature (T_c) require some effort to implement in SCE, nevertheless, they are actively developed in two main configurations: FSF [208] and SFF [209]. Parallel configuration of F-layers magnetization suppresses superconductivity and provides lower T_c, while antiparallel configuration provides higher T_c of a thin superconducting film. In the range between these two critical temperatures, the magnetization reversal of one free (F) layer switches between normal and superconducting states. Long-range triplet creation may provide an additional way to drain Cooper pairs from the superconductor, and thus produce an even larger T_c shift [210]. The use of a half-metallic ferromagnet in SFF spin valves produces a giant spin-valve effect with T_c shift ~ 1 K [211]. These structures require that the T_c shift at magnetization reversal be larger than the superconducting transition width to fully switch the superconductor, a challenge that appears manageable [208, 211, 212, 213].

2.3.2.2.2. SPIN VALVE JOSEPHSON JUNCTIONS (SVJJ)

Figure CEQIP-3b shows the basic superconductor-ferromagnet-superconductor (SFS) device structure. The superconducting critical current passes directly through the magnetic layers. Adding an insulator layer (SIFS) as shown in Figure CEQIP-3c increases the normal state resistance and can provide a larger characteristic voltage V_c if the combined barrier layers are sufficiently transparent for the device to have a large critical current. The tunnel current through the insulating barrier can be increased by sandwiching it between two superconductor layers (SIsFS) as shown in Figure CEQIP-3d. While spin valve JJs can be made using either spin-singlet or spin-triplet supercurrents [214], spin triplet devices are covered separately in section 2.3.2.2.4.

Challenges include sensitivity to magnetic layer thicknesses and quality, and the need to switch the free layer using magnetic fields produced by external control circuits.

Status: Spin valve Josephson junctions are under development by Northrop Grumman in collaboration with Michigan State University [215, 216], Hypres/SeeQC (USA) [217], University of Leeds [218], Lomonosov Moscow State University [207], Institute of Solid State Physics RAS (Russia), and others. Northrop Grumman is developing Josephson magnetic random-access memory (JMRAM) using a spin valve Josephson junction for state and a SQUID-based readout multiplexer. Unit cell size, set by the readout multiplexer, scales to 32 Mibit/cm^2 with 90 nm feature size. The projected read and write energies per 64-bit word at 4 K are 10 aJ and 50 fJ, respectively. Advantages of JMRAM are high density and reads that are fast and low energy. Writes are expected to take longer than 1 ns but could be tolerable using memory latency hiding techniques. The JMRAM unit cell and its write drivers have been demonstrated as stand-alone devices [219].

SIsFS junctions with a single ferromagnetic layer are under development experimentally [276, 277, 220, 221] and theoretically [278, 222]. These junctions include a soft ferromagnetic layer of PdFe with about 1% iron that changes magnetic state in a weak external field, thereby shifting the Josephson current Fraunhofer pattern and thus the current-phase relationship (CPR).

SF_1HF_2S junctions with a half-metal (H) layer are theorized to have a ground state phase ψ determined by the angle between the magnetic moments of ferromagnetic layers F_1 and F_2 [223]. Incorporation of a ψ-JJ into a superconducting loop could enable controlled switching between states with different vorticities without application of external magnetic flux, for example by microwave radiation.

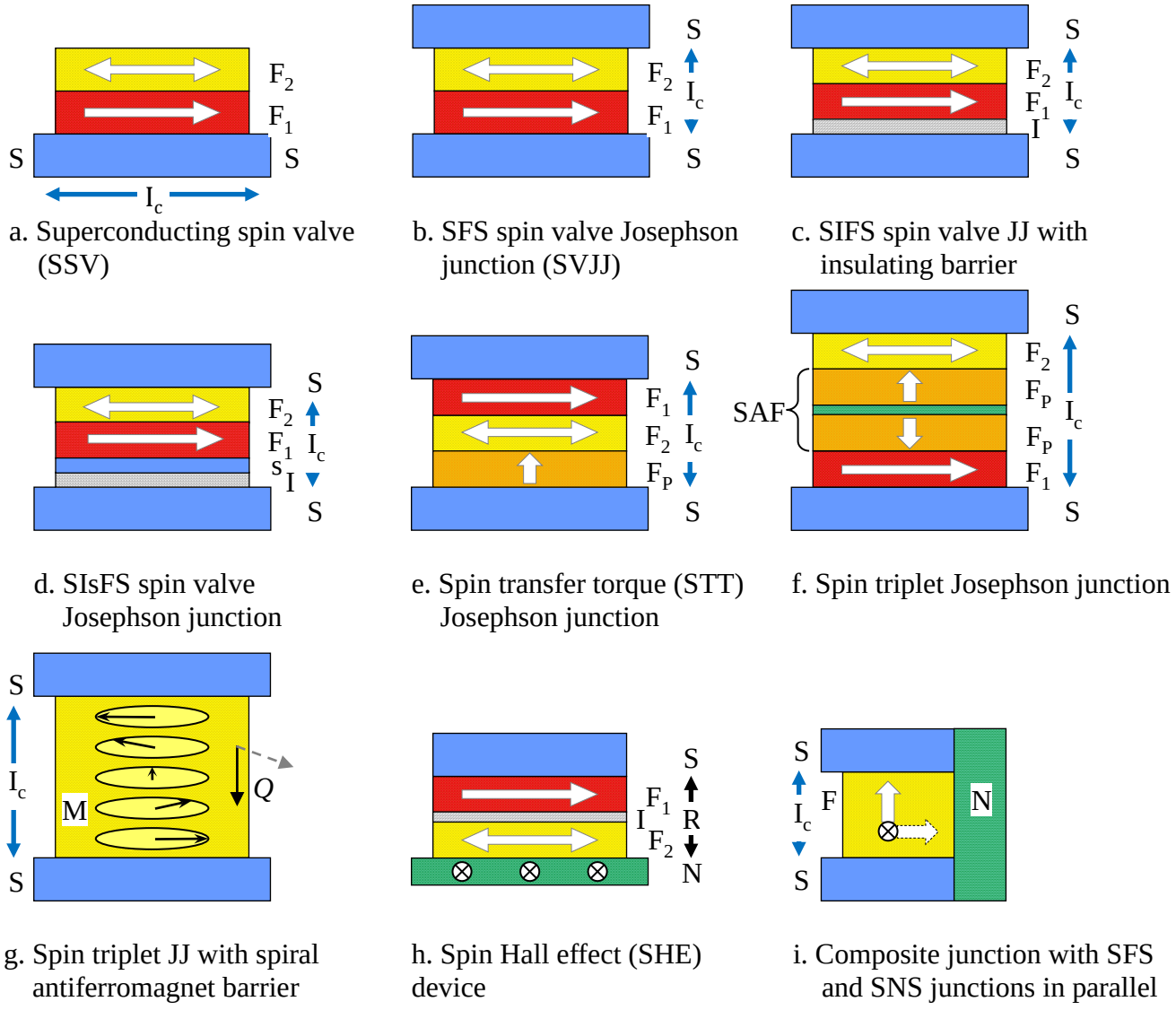


Figure CEQIP-3 Magnetic Memory Device Structures

Superconductors (S) are shown in solid blue. Ferromagnetic materials (F) are shown with magnetization direction either fixed (hard) or bidirectional (soft). Insulators (I) are speckled gray. Normal metals (N) are checkered green. Buffer layers are not shown except within a SAF.

2.3.2.2.3. SPIN TRANSFER TORQUE JOSEPHSON JUNCTIONS (STTJJ)

Figure CEQIP-3e shows an example device structure. Spin transfer torque (STT) devices use spin-polarized currents to switch the magnetization direction in one layer within the device. Switching the free layer is performed by passing current through a spin polarizing layer F_P. The resulting spin current produces a torque on the free layer that depends on current direction. Spin current production is covered in § **2.3.1.13**. STT junctions might scale to smaller sizes than SVJJs as they do not rely on magnetic fields produced by nearby control wires. Challenges include the need for bi-directional write currents, high current density required for switching, and difficulty fabricating the polarizing layer.

Status: STT switching has been observed in Josephson junctions with pseudo-spin-valve barriers $Ni_{0.8}Fe_{0.2}$/Cu/Ni, although the switching currents were high [224]. Spin-valve nanopillars with in-plane magnetized dilute permalloy demonstrated switching times ~ 0.5 ns and energies of 18–36 fJ, depending on direction [225]. CoFeB/MgO-based perpendicular magnetic tunnel junctions (pMTJs) have magnetoresistance >120% at 9 K [226]. Orthogonal spin-transfer (OST) devices with orthogonally magnetized layers have been demonstrated with switching times well below 1 ns; however, devices with greater magnetoresistance will be required to allow readout by superconductor circuits [227]. Mo-based pMTJs were fabricated and switching characteristics measured at temperatures down to 2 K [228]. At 4 K the switching energy in present devices can raise the junction temperature significantly and cause stochastic switching [229].

2.3.2.2.4. Spin Triplet Josephson junctions (S3JJ)

Figure CEQIP-3f shows an example device structure. The synthetic antiferromagnet (SAF) in the structure shown serves to fix the F_P layers in a perpendicular orientation. Noncollinear magnetization of the magnetic layers can create spin triplet Cooper pairs, which have a longer range than the ordinary spin singlet Cooper pairs [186, 230, 231]. Also required are nonmagnetic spacer layers to decouple magnetic layers while promoting high magnetic quality in the subsequent layer. An advantage is that the 0-π switching is caused by spin rotations rather than phase accumulation as in SVJJs, so device behavior is less sensitive to the exact thicknesses of the F_1 and F_2 layers. Challenges include getting sufficiently high critical current density in a structure with so many layers.

Status: Birge's group at Michigan State University is developing memory devices based on Josephson junctions with spin triplet supercurrent [214, 231, 232, 233]. The most recent work demonstrated controlled switching of the ground-state phase difference between 0 and π, but the critical currents were less than 10 μA.

Spiral (helical) antiferromagnets have been proposed as an alternative barrier material for superconducting spin triplet spin valves [234, 235, 236, 237] and spin triplet Josephson junctions [238]. Figure CEQIP-3g shows an example device structure that replaces multiple barrier layers with a single layer with spiral magnetization. Switching the spiral magnetization vector Q between stable states can change both I_c and the ground state (zero current) superconducting phase difference φ_0. MnSi develops helical magnetic order below a transition temperature of 29.5 K and might be a suitable material that could produce 0-π junctions with layer thickness in the range of 3.2 to 4.0 nm. The potential barrier separating spiral magnetic orientations might make these devices less susceptible to half-select problems. Challenges include demonstration of memory elements.

2.3.2.2.5. Spin Hall effect (SHE) devices

Figure CEQIP-3h shows an example device structure with current ⊗ going into the normal metal layer at the bottom. Spin-orbit torque (SOT) from the spin Hall effect in heavy metals can rapidly and reliably switch an adjacent ferromagnet (F) free layer of a nanoscale magnetic tunnel junction in a three-terminal configuration. Challenges include the need for bi-directional write currents and write voltages difficult to provide with SFQ circuits.

Status: Raytheon BBN (USA) together with Buhrman's group at Cornell University have demonstrated cryogenic spin Hall effect magnetic tunnel junction (SHE-MTJ) memory devices in a 4 × 4 array [239]. Heater-cryotron bit select devices were used to achieve writing times of a few nanoseconds, write energies ~ 8 pJ, and BER ~ 10^{-6}. Prospects for decreasing the bit energies include improved spin Hall materials, device structures, or lithography [239, 240]. Challenges include scaling to memory arrays with thousands of bits and lower read and write energies.

Quantum anomalous Hall effect (QAHE) devices have been proposed for non-volatile cryogenic memory arrays [241].

2.3.2.2.6. Composite junctions

Figure CEQIP-3i shows an example composite junction consisting of two parallel regions with different characteristics. In the structure shown, the SNS portion functions as a Josephson junction with 0 phase difference at zero current and the SFS portion can function as a π-phase junction. The composite junction functions as a SQUID consisting of the two junctions in parallel. The readout time of such memory elements is estimated as 10s of picoseconds. Writing by magnetization reversal requires times on the order of 10 ns [8]. Composite junctions with a non-single-valued current-phase relationship (CPR) might be able to switch between two logic states by changing the current through the device, which could occur on the picosecond timescale. Some of these theoretical predictions were based on nonuniform SF-FNS junctions with different structures [242, 243]. Recent theoretical work indicates that the structure shown in Figure CEQIP-3i is most suitable for practical realization among those considered [244]. Challenges are likely to include fabrication, scalability to small sizes, and incorporation into accessible memories.

2.3.2.2.7. Other magnetic memory devices

Josephson junctions with Si barriers containing Mn magnetic nanoclusters have been demonstrated to function as memristive elements capable of synaptic weight training using electrical pulses with energies as small as 3 aJ [245]. Anomalous or φ_0

Josephson junctions with a finite ground-state phase shift might provide switchable memory elements [246, 247]. Proposed is a memory element containing a magnetic EuS magnetic film on top of a NbN nanowire [248]. Proposed is a hybrid memory using Josephson junctions and Toggle MRAM [249].

2.3.2.3. OTHER CRYOGENIC MEMORY

Hybrid superconductor-CMOS memories are covered in section **3.3**.

Nanowire-based memory devices are under investigation by a few groups [107, 250, 251]. A memory array of 8 cells (2 bits × 4 words) has been demonstrated using heater-cryotrons [107].

Charge configuration memory (CCM) based on resistance switching between charge ordered phases of 1T-TaS_2 has demonstrated ps switching times with fJ switching energies [252, 253, 254, 255].

Quantum phase slip junction (QPSJ) memory devices have been demonstrated using Al nanowires at mK temperatures and promise very low error rates [256]. These memory devices are compatible with QPSJ logic (see § 2.3.1.5 and § 2.3.3.3).

Proposed but not yet demonstrated devices include ternary memory cells using Josephson junctions [257, 258], superconductor-ionic memory devices [259], superconducting memristors [260, 261, 262] and meminductors [263].

2.3.3. SWITCHING DEVICES

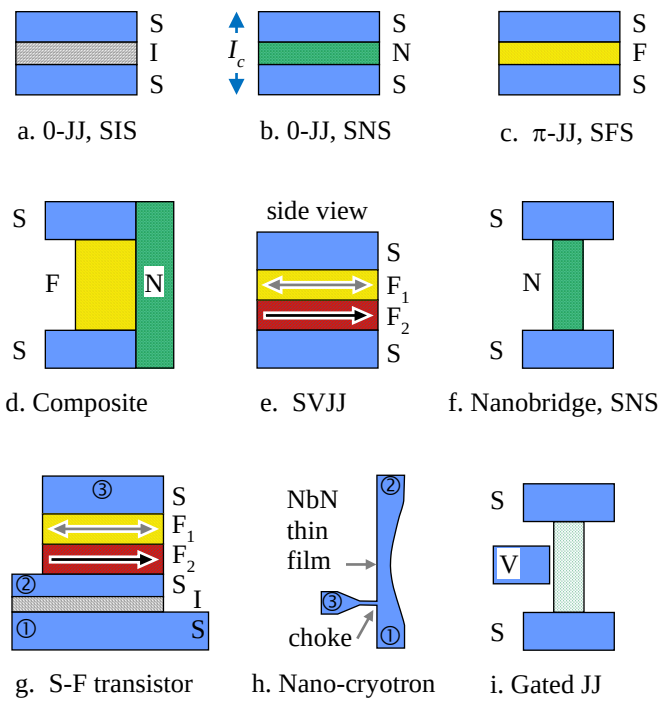


Figure CEQIP-4 Superconductor (S) switching devices

a. 0-JJ: Josephson junction with insulating (I) barrier, b. 0-JJ: Josephson junction with normal metal (N) barrier, c. π-JJ: Josephson junction with a ferromagnetic (F) layer creating a π phase shift, d. Composite: junction with SFS and SNS in parallel, e. SVJJ: spin valve Josephson junction, f. Nanobridge junction, g. S-F transistor: SVJJ on top of an SIS junction, h. Nano-cryotron with 3 terminals, i. Gated JJ: Nanobridge with control (V) electrode. Superconductors (S) are shown in solid blue. Ferromagnetic materials (F) are shown with magnetization direction either fixed (hard) or bidirectional (soft). Insulators (I) are speckled gray. Normal metals (N) are checkered green. Buffer layers are not shown except within a SAF.

2.3.3.1. JOSEPHSON JUNCTIONS (0-JUNCTIONS)

A Josephson junction consists of two superconducting electrodes connected by a weak link that has a critical current much lower than the electrodes. The most common junctions have a thin, insulating barrier material such as aluminum oxide (Figure CEQIP-4a).

Improvements are needed in standard Josephson junctions fabricated with insulating barriers. Consider the current process for fabricating Nb/Al-AlO_x/Nb 'trilayer' junctions. Niobium deposited on the bottom layer forms columnar grains with surface roughness of several nanometers, which is significant as the insulating barrier layer is only about 1 nm thick. An aluminum layer deposited on top of the lower Nb electrode greatly smooths out the surface, but Al is not superconducting at typical operating temperatures (~4 K), so the thickness variation contributes to tunneling current density variation across the junction. The Al layer is oxidized in a controlled atmosphere, typically at room temperature, before deposition of the Nb top electrode. The resulting amorphous aluminum oxide barrier has both structural and compositional defects that affect the conductivity over nanometer length scales. Supercurrent tunneling depends exponentially on barrier conductivity, which accentuates small variations.

Sputter deposition of Nb can't fill gaps smaller than about 100 nm. The superconducting properties of Nb are also sensitive to stress and to poisoning by oxygen or hydrogen, limiting fabrication temperatures to below about 180 °C, far below the ~400 °C temperature limit for CMOS processing at the back end of the line. A consequence is that standard CMOS processes require performance-limiting modifications for use with Nb junctions. SiO_2 deposited at low temperatures contains H and OH that comes out if heated too much. After etching to define the junction, wet anodization of the Nb is sometimes performed to seal the barrier region from contamination, although this is not a standard semiconductor foundry process.

Producing junctions with critical current variations less than 1% has been difficult for junctions with critical current densities greater than 100 μA/μm^2 and diameters less than about 1 μm. Junction critical currents must be about 100 μA at 4 K due to noise considerations. Combined, these constraints have limited minimum junction diameters to roughly 1 μm. Shrinking junction sizes would require greater control over formation of the barrier layer to achieve both higher critical current density and lower variation, which might be possible even with aluminum oxide barriers.

Replacing the barrier layer with a thicker, resistive material is an alternative and has the advantage of providing junctions that do not require shunt resistors, which often require more area than the junction itself [264]. Barrier replacement requires development of a process capable of yielding predictable, uniform, and stable properties using materials compatible with the Nb superconductor.

2.3.3.2. WEAK LINK JUNCTIONS

Shrinking the size of Josephson junctions below 90 nm might require significantly different devices. Josephson junctions can be produced using weak links in a variety of forms including nanobridges between the superconducting electrodes (Figure CEQIP-4f) [265]. The materials are typically metals or even superconductors weakened by the small size. Dimensions of conductive nanobridges must be on the order of the superconducting coherence length in the bridge material, which is ~40 nm for Cu in close proximity to a strong superconductor, ~10 nm for Nb, and ~5 nm for NbN or NbTiN.

Weak-link junctions include superconducting nanobridges [20, 266, 267, 268, 269], and SNS or composite devices (Figure CEQIP-4b, d) [270, 265, 271, 272].

Multi-layer or exotic materials might provide improved nanobridge properties. For example, topological insulators have conducting surface or edge states that might be less sensitive to dimensional variations.

Challenges include interfacial effects in composite junctions (e.g., SNS), sensitivity to operating temperature, additional materials (if required), and fabrication on nanometer scales with adequate control of variation.

2.3.3.3. QUANTUM PHASE-SLIP JUNCTIONS (QPSJ)

QPSJs are a dual to Josephson junction devices with the roles of phase and charge interchanged as well as current and voltage [182]. QPSJs have a critical voltage, V_C, above which an electron pair tunnels through the junction. A charge island consisting of two QPSJs and a capacitor is the main element in QPSJ-based logic circuits. Different connections between charge islands can be used to make different logic gates.

Advantages of QPSJs relative to JJs include voltage control, far less sensitivity to magnetic fields [175], and possibly lower switching energy. Nanowire QPSJ devices also might have some fabrication advantages over Josephson junctions, although fabrication experience with NbN nanowires indicates that challenges remain, particularly in device variability and operating temperature [177, 180, 181]. Voltage-biased superconducting rings have been proposed as a way to reduce the fabrication difficulty [273, 274].

2.3.3.4. MULTI-TERMINAL SWITCHING DEVICES

Both JJs and quantum phase-slip junctions (QPSJs) are two-terminal devices, which require more components to perform typical logic functions. Multi-terminal superconductor switching devices might reduce device count and increase circuit density.

One approach is to stack a spin-valve junction on top of a regular Josephson junction to make a JJ transistor (Figure CEQIP-4g). Magnetic elements are incorporated in switching devices such as SFIS junctions [275], SIsFS junctions [276, 277, 278], and superconducting ferromagnetic transistors with SISFIFS structures [279]. SIsFS junctions are promising due to their high-I_cR_n product, up to about 2 mV, that determines the maximum switching frequency of the device. Such junctions have non-single-valued current-phase relationships (CPR) as discussed in §**2.3.2.2**. Challenges include fabrication process complexity and development of new logic families.

Nano-cryotrons with three or four terminals (Figure CEQIP-4h) are a proven approach to making multi-terminal devices [111, 112, 114]. Advantages include Challenges include fabrication process complexity and development of new logic families.

Control effects based on current injection [280, 281], phonons [282], or voltage [283] could lead to development of multi-terminal, gated JJs (Figure CEQIP-4i). Challenges include reduction of the switching voltage to a level compatible with the overall circuit, avoidance of supercurrent tunneling from the control electrode, and development of a new logic family.

2.3.3.5. HIGH-TEMPERATURE SUPERCONDUCTOR (HTS) JUNCTIONS

High-temperature superconductors (HTS) have a critical temperature T_c greater than 30 K. Josephson junctions produced in $YBa_2Cu_3O_{7-\delta}$ (YBCO) films by helium-ion beam irradiation have been fabricated with junction widths down to 50 nm [284]. A step-edge HTS Josephson-junction mixer operated at 600 GHz and temperatures of 20–40 K with superior performance [285]. Progress on applications of high-temperature superconducting microwave filters has been reviewed [286]. Still, the large critical current spreads typical in HTS device characteristics are problematic for SFQ logic. The small coherence lengths typical of HTS materials cause junctions made of these materials to be very sensitive to fabrication variations.

2.3.4. OTHER CIRCUIT ELEMENTS FOR SCE

2.3.4.1. CURRENT SUPPLY

SFQ circuits typically supply a DC bias of about $0.7I_c$, or roughly 100 μA per switching Josephson junction. Large supply currents are undesirable as they can exceed the current carrying capacity of thin film lines and also produce magnetic flux that can affect circuit operation. DC powered circuits are thus limited to a few thousand junctions per supply pad on the chip. A technique called current recycling or serial biasing allows a smaller DC bias current to cascade through multiple circuit blocks and thus reduce the required supply current [287, 288, 289]. Disadvantages of current recycling include more difficult design and greater variation in bias currents. An approach called local magnetic flux biasing (LFB) reduces the supply current to a chip by passing the DC bias through transformers in series [290]. Ramping the supply current to the operating point induces persistent bias currents in superconducting loops within the transformer-coupled subcircuits. While circuits with tens of junctions have been demonstrated with encouraging results, further work is needed to apply the LFB approach at larger scales.

AC power has scaling advantages as it can supply both current and clocking to many more junctions using transformers in series, with each transformer supplying a single junction or subcircuit. AC power is used for RQL [124, 291, 292], PML, and QFP circuits [142]. Cells requiring DC bias can be supplied by AC/DC converters [120, 121] or AC/SFQ converters [122].

2.3.4.2. PHASE SHIFT ELEMENTS

As introduced in section 2.1, phase shift elements set or change the superconducting phase φ between locations in a superconducting circuit. Currents through circuit elements can be used to shift the phase. The phase difference across an inductor is given by $\varphi_L = 2\pi IL/\Phi_0$, where I is the current, L is the inductance, and Φ_0 is the magnetic flux quantum. Other devices such as Josephson junctions have different current–phase relationships. Achieving a given phase difference involves a tradeoff between current and inductance. Large inductances can require too much circuit area, whereas large dc external currents can become difficult to supply without creating magnetic fields that affect circuit operation.

Wires that produce magnetic fields are the simplest inductive devices. Note that magnetic inductance can depend significantly on the full geometry of the circuit, including ground planes that carry current return paths, which can reduce calculation accuracy [293]. Wire inductors are also susceptible to interference between inductors and from the external environment.

High kinetic inductance superconductors such as MoN_x or NbN can be used to fabricate smaller inductors [294]. The kinetic inductance in thin films of these materials can be many times larger than the inductance produced magnetically. Advantages of

kinetic inductors include less dependence on nearby circuits, which makes design easier. Kinetic inductors are also less sensitive than magnetic inductors to interference from external currents and magnetic fields.

Persistent current trap phase shift elements use trapped magnetic flux to provide phase shift [295, 296, 297, 298].

Ferromagnetic patterns placed close to superconducting loops have been used as reconfigurable phase shift elements [299].

Stacks of Josephson junctions can provide sufficient inductance to replace thin-film inductors [300]. Josephson junctions used to provide inductance must operate well below their critical current to avoid switching and to avoid the large inductance variation that occurs near the critical current. Stacks of 3 to 4 junctions can be fabricated as pillars with heights less than 200 nm. If fabricated with the same critical current density as the switching junctions, the stacked JJ inductors must be of larger diameter to avoid switching. Using different fabrication processes for switching and inductor junctions can provide denser circuits at the expense of greater process complexity. Tolpygo et al. [294] argue that fabrication of thin-film inductors is much simpler and expected to have a higher yield than stacked junctions, thus favoring the high kinetic inductance approach.

Anomalous junctions can provide a non-zero phase shift φ_0 without an applied bias current [246, 247]. Josephson junctions can be characterized by their current-phase relationships, particularly the ground state phase shift [115]. Junctions with zero phase shift in their ground state, like those typically used for switching, are called 0 JJs. Pi junctions (π JJs) have $\pm\pi$ phase shift in the ground state and can be used to create circuits that require little or no external bias current [115, 116, 301, 302, 303, 304, 305]. Junctions with other ground state phase shift are known to exist (e.g. 0–π, φ, 2φ) and might be fabricable [244, 306]. Advantages of using magnetic junction phase shifters can include reduction in bias current required, reduction in junction count, improvements in energy efficiency, increased circuit density, and increased operating margins [115]. Magnetic junctions not intended to switch do not require large *IcRn* products, so are relatively simple to fabricate. SF_1HF_2S ψ-junctions might allow tunable phase shifts [223].

A problem with pi junctions is that the direction of the ground state current is undetermined, which limits their application. True phase batteries have been demonstrated using φ junctions incorporating InAs nanowires [306]. A superconducting diode [307, 308, 309] in series with a pi junction might be another way to create a phase battery.

D-wave superconductors such as YBCO can also be used to produce phase-shift devices [310].

Phase shift elements needing near-term development include manufacturable high kinetic inductors, stacked junction inductors, and π-JJs.

2.3.4.3. TRANSFORMERS

Current transformers rely on magnetic coupling between inductors, which seems difficult to scale to very small dimensions. Shielding to prevent interference from external signals can also add to the difficulty in scaling transformers [288]. Transformers are most important in AC-powered logic families such as RQL, PML, and all forms of QFP. DC current recycling can also use transformers to couple signals between circuit blocks.

Miniaturization of transformers is addressed in [203, 311]. Needed are transformer alternatives or scaling approaches that allow significantly higher circuit density.

2.3.4.4. TRANSMISSION LINES

On-chip data interconnects can be either Josephson transmission lines (JTLs) or passive transmission lines (PTLs) [312, 313, 314, 315, 316]. JTL cells include 2 JJs, both of which switch when transmitting a digital ‘1’. Long JTLs consume too much energy and result in too much time delay and jitter, so PTLs are often preferred for distances longer than a few gate lengths.

Passive transmission lines transmit SFQ pulses over a stripline or microstrip. SFQ signals travel ballistically on PTLs at roughly one third the speed of light and can travel several millimeters before regeneration is required. Models for propagation must include losses and dispersion to accurately predict behavior [317, 318]. Minimizing reflections requires the impedance of a PTL to closely match both the driver circuit output impedance and the receiver circuit input impedance, which can be difficult to achieve. The effective output impedance of a Josephson junction is the resistance including any shunt. A challenge is that matching the stripline impedance to a Josephson junction driver, which typically has low impedance, can require a stripline with signal line width of 1 μm to 10 μm. Stripline and microstrip impedance scaling and matching are discussed in [312, 315]. Losses in Nb striplines of 250 nm width were found to be dominated by losses in the dielectric at low power and in the superconductor at high power [319]. Another challenge for scaling is that electromagnetic wave propagation can slow down significantly as Nb linewidth decreases below 1 μm due to increasing kinetic inductance and fringing capacitance [320].

2.3.4.5. Flux Traps and Moats

Magnetic flux trapped within superconducting circuits causes circulating currents that can cause the circuits to malfunction. Flux traps or moats attract magnetic flux during cooldown through the transition from normal to superconducting states and provide a location where the flux can be held without seriously affecting nearby circuits [321, 322, 323].

2.3.4.6. Through- Substrate Vias (TSVs)

Superconducting through-substrate vias (TSVs) enable stacking of more than the two chips possible using flip-chip bonding. Superconducting TSVs have been demonstrated using TiN (T_c = 2–3 K) [324, 325] and Al (T_c < 1.3 K) [326]. While these are sufficient for quantum applications at temperatures in the millikelvin range, TSVs with higher critical temperature are required for applications above 2 K.

2.3.5. Architectures and Applications

2.3.5.1. Traditional Computing Architectures

Von Neumann microarchitectures typical in CMOS microprocessors are also common in superconductor processors using SFQ logic. Recent examples include 8-bit microprocessors with memory [66, 67], a 16-bit bit-slice ALU for 32- or 64-bit RSFQ microprocessors [327], and design of a 16-bit RQL CPU [128]. Gate-level deep pipelining with bit-parallel architecture can be disadvantageous for CMOS due to pipeline register overhead but appears promising for SFQ processor designs [328]. The MANA 4-bit AQFP microprocessor was developed with a hybrid RISC-dataflow architecture using 21,460 junctions and is estimated to dissipate about 30 aJ/op at 5 GHz [152, 329].

2.3.5.2. Reconfigurable Computing Architectures

The small amount of SFQ-compatible memory available for microprocessors has driven alternative architectures such as reconfigurable data-path processors [70].

Superconductor field-programmable gate arrays (SFPGAs) were first proposed in 2007 using RSFQ logic circuits and RSFQ NDROs as memory elements [330]. Proposed is an RSFQ SFPGA using magnetic Josephson junctions (MJJs) for implementation of area-efficient switches [90]. An all-SFQ FPGA design that allows both combinational and sequential logic is analyzed for chip sizes from 5 mm × 5 mm to 50 mm × 50 mm [331]. An AQFP SFPGA with a cryo-CMOS memory has been designed and a 2×2 unit system demonstrated [332]. FPGAs can provide significant benefits to users in flexibility and reconfigurability, but at a cost of significant circuit overhead. Challenges for superconductor FPGAs include switch matrix overhead using SFQ logic and the low density of superconductor circuits, which does not yet allow sufficient functionality in a single-chip SFPGA. Still, work is needed to prepare for the time when sufficient circuit density and complexity is available.

2.3.5.3. Temporal SFQ (TSFQ)

TSFQ has been primarily applied for the implementation of dataflow accelerators and networks on chip (NoC). Example designs include a genome sequencer [103], decision trees [103, 104], and a rotary NoC [333]. Moreover, temporal codes and operators have been used in conjunction with stochastic codes for the implementation of dot-product-units and FIR cores [334].

2.3.5.4. Neuromorphic Architectures

Neuromorphic approaches to computing and artificial intelligence using superconductor electronics are under investigation. In the fields of machine learning and artificial intelligence, superconductor electronics is one of many emerging device technologies [335]. As intrinsically nonlinear elements, Josephson junctions might have advantages for artificial neural networks due to behavioral similarities to biological neural circuits, high speed, and energy efficiency. For example, an artificial synapse based on ferromagnetic Josephson junctions demonstrated a spiking energy per pulse less than 1 aJ [245].

Neuromorphic approaches include those based on switching Josephson junctions [336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347], QFP circuits [348, 349, 350, 351], magnetic Josephson junctions [245, 352, 353, 354], nanowires [111, 112, 177, 355, 356, 357], quantum phase slip junctions (QPSJs) [179, 358], and superconducting qubits [359]. Hybrid approaches include optoelectronic using photons for communication and superconductor electronics for computation [360, 361, 362], analog-digital hybrids [363], and SFQ-quantum hybrids [344]. Recent reviews include [364, 365].

Challenges for superconductor electronics include high fanout requirements and the low circuit density currently available. While neuromorphic architectures appear promising, only small circuits have been demonstrated to date.

2.3.5.5. Quantum Computing: Control and Readout

The D-Wave 2000Q released in 2017 includes a superconducting chip with 128,472 Josephson junctions, of which 75% are in classical SFQ digital control circuitry to program the processor and read out the results and the remainder are either directly in

qubits or in the analog coupling elements that allow qubits to interact in a programmable way. The D-Wave Pegasus P16 chip in the Advantage QA system released in 2020 includes a superconducting chip with 1,030,000 Josephson junctions, 40,484 couplers, and a maximum of 5,640 qubits [702].

SFQ pulses have been demonstrated to control superconducting transmon qubits [366, 367]. A Josephson arbitrary waveform synthesizer (JAWS) using an array of 102 Nb/Nb-Si/Nb JJs successfully generated control signals at 4 K [368].

QC control architectures are under study [369, 370]. AQFP appears promising for qubit control circuits at temperatures below 1 K due to its extremely low energy dissipation [370].

2.3.5.6. OTHER COMPUTING ARCHITECTURES

Compute-in-memory architectures proposed include a non-volatile memory system based on the quantum anomalous Hall effect [371] and so-called MAGIC (Memory And loGIC) cells perform the functions of both memory and logic [372, 373].

An amoeba-inspired problem solver for a small-scale Boolean satisfiability problem (SAT) has been demonstrated using stochastic AQFP gates in a scalable architecture [374].

Memcomputing uses logic elements containing memory. Digital memcomputing machines with self-organizing logic gates have been simulated with promising results [375, 376, 377]. Needed is replication of the results reported.

2.3.5.7. SENSOR READOUT APPLICATIONS

A high-sensitivity and energy-efficient AQFP readout interface has been developed for an array of NbTiN superconducting nanowire single-photon detectors (SNSPDs) [378]. Improved timing information is possible with hybrid AQFP-RSFQ circuits [379].

2.3.6. FABRICATION FOR SCE

Josephson junctions are typically made by forming a barrier layer sandwiched between two superconducting electrodes, a structure like a thin-film capacitor shown in Figure CEQIP-1a and in Figure CEQIP-4a. A variety of materials can be used, but most common for SFQ logic operating in the 4 K temperature range are junctions made with niobium electrodes separated by a thin aluminum oxide barrier layer (for details, see § 2.3.6.1). The horizontal orientation shown in Figure CEQIP-1b is also possible, although less common as the barrier is more difficult to fabricate.

Weak link or nanobridge junctions consist of a small filament of superconductor or normal metal between larger electrodes. The diameter and length of the weak link need to be around the superconducting coherence length, which is about 10 nm for Nb and 5 nm for NbN (see Table CEQIP-8). Such dimensional control was difficult until recently and sandwich junctions were easy to produce, so processes for making weak link junctions have not been refined to the extent necessary for fabrication of complex circuits. For further information, see § **2.3.3.2**.

Acceptable process variations are typically tighter for Josephson junctions than for CMOS transistors, which presents fabrication challenges, especially as the push for greater energy efficiency drives designers toward smaller junctions. On the positive side, superconductor electronics has less need to reduce device sizes as Josephson junction switching speed does not depend directly on device size and superconducting interconnects reduce the penalty for sending signals over a distance. Still, there are significant advantages to increasing the number of devices on a chip, so the push to smaller device and feature sizes continues.

Table CEQIP-7 Fabrication Processes for SCE

Organization	*Process*	*Wafer sizes*	*F [nm]*		*Wire material, layers*	*Barrier material*	*J_c [$\mu A/\mu m^2$]*
			JJ	*Wire*			
AIST, Japan	ADP2	3 inch	☐ 1000*	1000	Nb, 9	Al-AlO_x	100
AIST, Japan	DGP	3 inch	☐ 1000*	1000	Nb, 7	Al-AlO_x	(2x) 100
AIST, Japan	HSTP	3 inch	☐ 1000*	1000	Nb, 4	Al-AlO_x	100
AIST, Japan	PHSTP	3 inch	☐ 1000*	1000	Nb, 4	Al-AlO_x	100
AIST, Japan	STP2	3 inch	☐ 2000	1500	Nb, 4	Al-AlO_x	25
D-Wave Systems,	SFQ	200 mm	○ 600	250	Nb, 6	Al-AlO_x	100

Organization	*Process*	*Wafer sizes*	*F [nm]*		*Wire material, layers*	*Barrier material*	*J_c [$\mu A/\mu m^2$]*
			JJ	*Wire*			
USA/Canada							
Leibniz-IPHT, Germany	RSFQ1H	100 mm	● 3800	2500	Nb, 3	Al-AlO_x	10
Leibniz-IPHT, Germany	SQUID	100 mm	● 3800	2500	Nb, 2	Al-AlO_x	0.7–3.5
MIT LL, USA	SC2	200 mm	○ 600	150	Nb, 8	Al-AlO_x	100, 200, 600
MIT LL, USA	PSE2 (2 JJ layers)	200 mm	○ 600 ○ 500	350	Nb, 8	Al-AlO_x, Ni	100, 200, 600 > 3000
MIT LL, USA	SC1	200 mm	○ 600	250	Nb, 8; MoN_x, 1	Al-AlO_x	100, 200
MIT LL, USA	SFQ5ee	200 mm	○ 600	350	Nb, 8; MoN_x, 1	Al-AlO_x	100
MIT LL, USA	SFQ4ee	200 mm	○ 700	500	Nb, 8	Al-AlO_x	100
NGC, USA	RQL25	150 mm	○ 600	250	Nb, 7	Al-AlO_x	100
NIST, USA	SFQ	3 inch	○ 1500	1000	Nb, 4	Nb_xSi_{1-x}	40
NIST, USA	SQUID	3 inch, 150 mm	○ 1500	600	Nb, 3	Al-AlO_x	10
NIST, USA	Voltage std	3 inch, 150 mm	○ 1500	600	Nb, 2	Nb_xSi_{1-x}	200
PTB, Germany	Voltage std	3 inch	○ 250	500	Nb, 4-5	Nb_xSi_{1-x}	40–200
Royal Holloway U. of London, UK	Qubit and Josephson junction	100 mm	> 50	> 50	Al, 2	AlO_x	0.2 to 10
SeeQC, USA	SeeQC-C2SL.d	150 mm	–	250	Nb, 2; AlMn, 1	–	–
SeeQC, USA	SeeQC-C4SL	150 mm	○ 600	250	Nb, 4, 5	Al-AlO_x	1, 10, 45, 100
SeeQC, USA	SeeQC-Q5SL, -C6SL, -9SL	150 mm	○ 600	250	Nb, 4, 5, 8; NbN_x, 1	Al-AlO_x	10, 45, 100
SIMIT, China	Nb03	100 mm	○ 1400	1600	Nb, 3	Al-AlO_x	60
SkyWater Technology, USA		200 mm	○ 600	250	Nb, 6	SiO_2	10
STAR Cryo-electronics, USA	Delta-1000	150 mm	○ 3500	1000	Nb, 3	Al-AlO_x	1
SUNY Polytechnic, USA	Qubit Rev.0	300 mm	○ 140	140	Al, 2	Al-AlO_x	0.2–2

F : feature size, minimum; J_c : JJ critical current density; □●○ : JJ layout shapes; * 700 for AQFP

Planarized processes for superconductor integrated circuit fabrication have been developed by AIST [429, 380, 381, 382, 383, 384, 385, 386], MIT Lincoln Laboratory [387, 388, 389, 390, 391], NIST [392], and SeeQC, which spun out of Hypres in 2019 [393, 394]. Unplanarized processes are in use at IPHT, Star Cryoelectronics, and SIMIT [395, 396, 397]. Development of 300 mm Josephson junction fabrication processes includes Al/AlOx/Al [398, 399] and Nb/Al-AlOx/Nb [400] for qubit applications, which typically require small junction sizes and low critical current densities. A few processes include MoN_x superconductor layers with high kinetic inductance [294, 401], self-shunted Josephson junctions [391, 402, 403], or π junctions [390].

SCE fabrication processes are summarized in Table CEQIP-7, with additional information available in the linked spreadsheet. The barrier material Al-AlO_x indicates formation by thermal oxidation of an aluminum layer that is only partially consumed. To be identified are key process parameters for future monitoring. Candidates include variability of I_c and J_c, R_n and I_cR_n product, sub-gap resistance R_{sg} or R_{sg}/R_n ratio, inductance per square, metal layer thickness, dielectric thickness, and yield.

While a variety of materials exhibit superconductivity [404], only a few are used in electronic circuits due to property, fabricability, and compatibility requirements. Superconductor materials and properties most relevant to superconductor electronics are included in Table CEQIP-8. The status of superconductor electronics is summarized in following subsections organized by superconductor material.

Table CEQIP-8 Superconductor Properties for SCE

Material	*T_c [K] Bulk*	*T_c [K] Thin Film (thickness)*	*Band gap $2\Delta_0$ [meV]*	*Coherence length, ξ [nm]*	*Mag. Pen. Depth, λ_L [nm]*	*J_c [GA/m^2]*	*Crystal structure*	*T melt [K]*
Al	1.18		0.34	1600	16		fcc, A1	933
In	3.41		1.0				tetragonal	430
MgB_2	39	close to bulk	1.8-7.5	3.7-12 ab 1.6-3.6 c	85-180		C32	1100
MoGe	7.4	4.4 (7.5 nm) [405]	2.2			12 (250 mK)	amorphous	
MoN	12						hexagonal	
$Mo_{0.6}Re_{0.4}$	15	12 (20 nm) [406]					A15	
MoSi	7.5	4.2 (4 nm) [405]				11–25 (1.7 K)	amorphous	
Nb	9.2		3.0	30–38 bulk 10–12 film [409]	41 bulk ~90 film		bcc, A2	2750
NbN	16	8.6 (3 nm) [405]	4.9	5	270	20–40 (4.2 K)	cubic, B1	2846
NbTiN	12–16	10–14 (50 nm) [407]				9.7–20.8 (2.5 K)	cubic, B1	
NbSi	3.1	2 (10 nm) [405]	0.94			0.14 (300 mK)	amorphous	
Nb_3Sn	18.3		7	4	30		A15	
NbTi	9.0		3	5	150			
Pb	7.2						fcc, A1	601
TiN	5.5						cubic, B1	3200
WSi	5	3.7 (4.5 nm) [405]	1.52			8 (250 mK)	amorphous	
$Yba_2Cu_3O_7$	92		50-60	1.5 ab ~0.3 c	140 ⊥ 700 ‖		perovskite	> 1270

⊥ : magnetic field perpendicular to the layers; ‖ : magnetic field parallel to the layers; Strukturbericht symbols for crystal structures

Note: Blank entries do not necessarily indicate lack of available information.

2.3.6.1. NIOBIUM-BASED JUNCTION FABRICATION

Josephson junction fabrication for non-quantum applications (T > 1 K) typically involves formation of the junction layer stack, commonly called the trilayer, followed by junction definition [408]. The layer stack is typically formed as a series of steps without exposure to atmosphere. Key layers include base superconductor, barrier, and top superconductor (or counter electrode). While the barrier can be any non-superconductor or weak link, most common for superconductor electronics are insulator or semiconductor barriers are as they produce higher switching voltages and speeds. The critical current through a Josephson junction depends on the quality of the superconducting electrodes, especially near the barrier layer.

2.3.6.1.1. BASE SUPERCONDUCTOR FORMATION

Nb (niobium) has a critical temperature T_c of about 9.2 K and is the most common superconductor for electronic applications at liquid helium temperature, near 4 K.

Nb films used for superconductor electronics typically have a columnar grain structure. The superconducting coherence length ξ and penetration depth λ are significantly different from single-crystal, bulk Nb values [409, 410], as shown in Table CEQIP-8. The superconductive properties of Nb are strongly dependent on purity [411]. Degradation of Nb films can occur by exposure to hydrogen [412, 413] or oxygen [414, 415]. Properties can also change over time by diffusion through the Nb and between adjacent materials such as Ti [416]. A smooth Nb surface is desired as junctions fabricated on a rough surface under the thin barrier layer show increased property variations [417]. One way to reduce Nb surface roughness is to deposit the base electrode using Nb/Al/Nb multilayers [409]. Nb surface morphology also can be controlled by bias target ion beam deposition (BTIBD) [418]. Other factors affecting Nb quality include residual stress in sputtered Nb films, film thicknesses, surface morphology, deposition rate, substrate temperature during deposition, electrical stress, and substrate preparation [419, 420, 421].

2.3.6.1.2. Barrier Layer Formation, AlO_x

As seen in Table CEQIP-7**,** aluminum oxide is the most common barrier for SCE with Nb electrodes. The usual process involves deposition of 5 to 10 nm of Al on the base Nb layer, exposure to oxygen gas to form ~ 1 nm of AlO_x on top of the Al, and deposition of the Nb top electrode [388, 422]. Control of the critical current density becomes increasingly difficult for J_C > 100 μA/μm^2. The Al layer wets Nb well, reduces roughness in the underlying Nb surface, and provides a relatively flat surface for growth of the oxide layer. The Al layer is only partially consumed during oxidation. Formation of the Al/AlO_x barrier is a complex process and conduction through the barrier can depend on many factors. Simulations are providing insight into the relationships between barrier processing, structures, and properties [423, 424, 425, 426, 427]. Plots of critical current density J_c as a function of oxygen exposure show regions with different slopes at low and high J_c [388]. Very thin barriers with high J_c shows evidence of conduction through numerous, small channels, perhaps related to defects or impurities in the oxide. As the oxide thickness increases, the number of high-conductivity channels decreases and conduction transitions to percolation between high-conductivity regions. Thicker oxide layers are dominated by tunneling of Cooper pairs (supercurrent).

Critical current densities below 10 μA/μm^2 are useful for applications at millikelvin temperatures such as superconducting qubits. The range from 10 to about 200 μA/μm^2 is typically used for digital and high-speed circuits. Junctions with critical currents above about 500 μA/μm^2 have barriers with sufficiently low resistance to be self-shunting, meaning that they do not require shunt resistors in SFQ logic circuits.

Self-shunted junctions for use in SFQ circuits can be made by various methods reviewed in [264]. Methods with AlO_x barriers include very thin barrier layers [388] or increasing the Al thickness so that the barrier includes a thicker normal metal layer in series with the insulating oxide layer [428].

Although remarkable progress has been achieved using Al/AlO_x barriers, several challenges will need to be addressed for scaling circuits to higher complexity, integration density, or speed. Perhaps the most serious challenge is the thermal stability of the amorphous aluminum oxide barrier, often designated AlO_x as it is not necessarily Al_2O_3. Many groups have observed a significant degradation of junction properties when processing temperatures exceed 200 °C. The necessity to keep processing temperatures low limits the temperature allowed for the interlayer dielectric deposition (typically SiO_2), which has been optimized for Si-based microelectronics above 200 °C. The low processing temperature limit for AlO_x also complicates integration of these junctions with other circuit components such as magnetic memory elements and CMOS devices.

Variation in high critical current density, self-shunted junctions is another concern. The properties of junctions are expected to be exponentially dependent on the thickness of the oxide layer, so that as the oxide thickness is reduced below 1 nm, high yield requires limiting thickness variations to less than a monolayer across large wafers, which is extremely challenging. Junction variation measurements reported for Nb/Al/AlO_x/Nb junction fabrication processes include those with J_C = 100 μA/μm^2 [388, 389] and 200 μA/μm^2 [429]. Double-barrier junctions were proposed as a way to reduce variations across a junction and achieve self-shunted behavior at modest critical current densities but have so far yielded devices with unfavorable characteristics for high-speed operation [430]. Recent fabrication improvements have dramatically reduced the number of junctions with properties outside the design range (“outliers”), but the mechanism responsible for the remaining outliers is not yet completely understood. If related to non-uniform oxide thickness or the presence of a non-uniform defect population, new approaches will be needed to achieve high yield upon further scaling [431]. Barrier formation by atomic layer deposition (ALD) shows promise but needs to be demonstrated in a production process [432, 433, 434].

2.3.6.1.3. Barrier Layer Formation, Alternatives to AlO_x

Nb-Si barriers are deposited as amorphous silicon with niobium in solid solution. Other designations for this barrier material include Nb_xSi_{1-x} and a-Si-Nb. Nb-Si films of interest for SFQ circuits are on the insulating side of the metal-insulator transition, which means less than about 11% niobium [435]. Nb-Si has lower resistivity than AlO_x, so greater thickness is required. Nb-Si barrier Josephson junctions have been used for several years in commercial voltage standard chips containing many thousands

of Josephson junctions (see § **2.2.2.2**). The potential for application of Nb-Si barriers in SFQ circuits that operate at higher clock frequencies is under active investigation [402, 403, 436]. Advantages include a thicker barrier layer and thus less sensitivity to small changes in thickness. Disadvantages include low thermal stability [437], high dielectric constant [402], and difficulty in achieving uniformity across a wafer by co-sputtering [438].

Si-W barriers are deposited as amorphous silicon with tungsten in solid solution [439].

Aluminum nitride (AlN_x) tunnel barriers have good characteristics up to high current densities, although formation by plasma nitridation of an Al layer is more difficult than the formation of AlO_x barriers [440]. Although nitride barriers are expected to have higher thermal stability than AlO_x above 200 °C, statistical studies on the stability of junction properties fabricated with higher processing temperatures have not yet been performed.

Halfnium oxide (HfO_x) was investigated as an insulating barrier material, but fabrication of good junctions was found to be difficult [441]. Hf-Ti self-shunted resistive barriers have been made with critical voltages up to 70 μA and J_c from 500 to 6000 $\mu A/\mu m^2$ [442].

Two-dimensional (2D) barriers of graphene have been demonstrated using CVD compatible with wafer-scale fabrication [443]. Other 2D barriers include twisted layers of graphene [444] and $NbSe_2$ [445]. Josephson diodes, which superconduct in only one direction, have been demonstrated in $NbSe_2/Nb_3Br_8/NbSe_2$ heterostructures [307]. Challenges include fabrication of devices at wafer scale, especially in cases requiring rotational alignment of atomically thin layers.

Needed are further studies of alternative barriers to determine whether they have significant advantages over AlO_x.

2.3.6.1.4. Top Superconductor Formation

The top Nb layer is typically deposited directly on top of the AlO_x barrier using the same deposition parameters for other Nb layers. There is some concern that the thin AlO_x layer could be damaged by energetic deposition of Nb atoms or that chemical reactions could occur at the AlO_x/Nb interface. A thin layer of Al deposited on top of the barrier and under the Nb top layer can improve junction properties [446].

2.3.6.1.5. Junction patterning and definition

After deposition of the junction trilayer, individual junctions are defined by photolithography, historically followed by wet anodization of exposed Nb and Al [447]. Wet anodization is not a common process in semiconductor foundries, and junction fabrication processes have been developed that do not use anodization [395, 419].

2.3.6.2. NbN and NbTiN Junction Fabrication

NbN (niobium nitride) and NbTiN (niobium titanium nitride) each have bulk T_c of about 17 K, which can be approached for films thicker than about 100 nm. Both materials have a crystal structure that does not match well with Si or SiO_x, but the superconducting properties can be improved by using buffer layers [448, 449, 450, 451] or III-nitrides [452, 453]. NbTiN films just 4 nm thick have been fabricated with a T_c of about 10 K [454]. NbN and NbTiN films can be deposited at room temperature by reactive magnetron sputtering [449, 451, 455], by reactive bias target ion beam deposition (RBTIBD) for lower surface roughness [456], or by plasma enhanced atomic layer deposition (PEALD) [457]. NbN is less chemically reactive than Nb and is much less sensitive to oxygen as a contaminant. Advantages of NbTiN can include better uniformity and surface properties as well as smaller kinetic inductance.

Josephson junctions have been fabricated with insulating barriers of deposited AlN [455, 458, 459,460, 461, 462, 463], AlN formed by nitridation of an Al layer [464], thermally oxidized Al [465], deposited MgO [455, 466, 467, 468, 469, 470], deposited MgO-AlN-MgO [471], thermally oxidized HfO_x [472], and He-ion beam damage [473]. Note that pure Al is far more difficult to nitridize than to oxidize, which is one reason that directly deposited barriers are more common on NbN and NbTiN. Another reason is that pure Al pulls N from adjacent NbN or NbTiN, which degrades the superconducting properties of both layers. Using a Hf diffusion barrier along with tunnel junction barriers of either HfO_x or Al-AlO_x showed limited success and sensitivity to the thickness of the Hf layer [474].

Self-shunted junctions can be made using conductive barrier materials such as a-Si [455], Ti-N [475], TaN_x [471, 476, 477, 478, 479, 480], or NbN_x [481].

Epitaxial junctions promise better properties, uniformity, and scalability to small sizes. Suitable substrates include single-crystal MgO or buffer layers such as TiN on silicon wafers. Epitaxial nitride junctions have been fabricated with AlN insulating barriers [458, 462, 462] and with conductive barriers of TaN_x [476, 480] and NbN_x [481]. Needed is a process to make uniform, epitaxial nitride self-shunted junctions with sufficiently high critical current density for rapid switching (J_C > 100 $\mu A/\mu m^2$) with a silicon wafer as the base substrate.

Fabrication processes for NbN integrated circuits are under development [459, 482] but are not yet available as a foundry service. Wafer-to-wafer bonding between NbN films has been demonstrated at 500 °C [483]. Needed for 3-D integration is a compatible through-substrate-via (TSV) technology.

Phase shift pi Josephson junctions have been fabricated using NbN with barriers of CuNi [484, 485, 486] and PdNi [487]. GdN can function as a spin filter in NbN junctions [488].

Needed is work on magnetic shielding and flux trapping in NbN and NbTiN circuits. The magnetic penetration depth of these materials (λ_L > 200 nm) is large, which means that much greater thickness might be required for shielding than in pure Nb (λ_L ~ 90 nm). One approach might be to include separate layers of a superconductor such as Nb to provide magnetic shielding. More advantageous would be to develop circuit families that require less magnetic shielding due to avoidance of magnetic inductors [116].

2.3.6.3. Al Junction Fabrication

Aluminum (Al) has a critical temperature T_c of about 1.1 K. Applications include superconducting qubits and associated circuits, typically operating at temperatures below 500 mK. Qubit applications typically require small junction sizes and low critical current densities. Shadow evaporation of Al/AlOx/Al junctions avoids lithographic processing of the junctions but the junction area is sensitive to shadow layer thickness [489]. A fully CMOS compatible overlap Josephson junction fabrication process has been demonstrated [490]. Development of 300 mm Josephson junction fabrication processes includes [398, 399, 490].

2.3.6.4. MgB_2 Junction Fabrication

Magnesium diboride (MgB_2) has a critical temperature T_c of about 39 K and exhibits s-wave superconductivity, which implies that it can be used to make three-dimensional materials and devices more easily than with the d-wave, planar superconductors. MgB_2 films of good quality have been fabricated using hybrid physical-chemical vapor deposition (HPCVD) on Si wafers coated with a boron buffer layer to prevent chemical reactions between Mg vapor and the Si substrate, however deposition and growth temperatures are high (~700 °C) [491]. Josephson junctions fabricated in sandwich geometry with MgO barriers have some attractive properties, but also unacceptably large critical current distributions [492, 493]. In-plane Josephson junctions with barriers formed by helium ion beam irradiation show reduced parameter spreads, but work is needed to increase the I_cR_n product of the junctions [493, 494, 495]. Additional challenges include degradation of MgB_2 on exposure to atmosphere, which makes patterning more difficult, and lack of multi-layer interconnects.

2.3.6.5. YBCO Junction Fabrication

Yttrium barium copper oxide (YBCO) is a family of crystalline compounds with a defect perovskite structure consisting of layers. $Yba_2Cu_3O_{7-x}$ (Y123) can have a superconducting critical temperature around 90 K, although the superconducting properties are much better in the a-b plane than in the c direction. The small coherence length (ξ ~ 1.5 nm in the ab plane) makes YBCO sensitive to grain boundaries and makes fabrication of Josephson junctions difficult [496]. Challenges include high-synthesis temperatures (> 700 °C), poor conductivity across high-angle grain boundaries, brittleness, lack of multi-layer interconnects, and large scatter in Josephson junction critical currents.

Grain boundary junctions in YBCO have been used to make small RSFQ circuits [497]. Large numbers of step-edge junctions have been fabricated by argon ion milling steps into an MgO substrate before deposition of the YBCO film, although I_c variation was high (1σ = 20 to 30%) [498]. In-plane Josephson junctions with barriers formed by helium ion beam irradiation show promise [284]. Applications tolerant of Josephson junction variation seem most promising, including junction arrays for magnetic sensors and amplifiers, microwave generators, and vortex-flow transistors [499]. Applications without junctions might include superconducting interconnects between environments below 10 K and intermediate temperatures in the 20 to 80 K range where semiconductor circuits can operate with less refrigeration penalty.

2.3.6.6. Other Superconductor Fabrication Processes

Re (rhenium) is a superconductor with a relatively weak tendency to oxidize, which is advantageous in superconducting quantum circuit and qubit applications. Re/Al-AlO_x/Re Josephson tunnel junctions have been fabricated with a T_c of 4.8 K [500].

Mo–Re (molybdenum–rhenium) alloys exhibit superconducting transition temperatures up to 15 K in bulk and up to about 9 K in thin films [406]. Mo–Re thin films can be sputter deposited at room temperature and are stable even under typical carbon nanotube CVD growth conditions that require a hydrogen-methane atmosphere at 900 °C. Josephson junctions have been fabricated with barriers of Si(W) that form tungsten nanorod or nanocluster weak links in Si [501, 502, 503,504, 505, 506, 507, 508], and graphene [509]. Challenges include the cost of Re, which is roughly 100 times that of Nb.

TiN (titanium nitride) with a T_c of 5 K has been used to make TiN/AlN/TiN junctions for use as qubits [510] and photon detectors [511].

High-temperature superconductors (HTS) have a critical temperature T_c greater than 30 K, which includes MgB_2 (section 2.3.6.4) and YBCO (section 2.3.6.5). As noted in section 2.3.3 Switching Devices, HTS Josephson junctions have not proven fabricable with the uniformity necessary for large scale circuits. Without adequate switching devices, HTS applications are limited to passive RF components and interconnects to higher temperatures.

Amorphous superconductors such as MoSi and WSi can be useful when grain boundaries or grain growth are problematic. Fabrication of thin film devices on flexible substrates is possible [512].

Other superconducting materials (e.g., high- T_c oxides, 2D, topological) could have applications in novel devices [513].

2.3.6.7. Fabrication Facilities and Equipment

The IC Insights forecast for 2018 is that 300 mm wafers represented about 70% of worldwide integrated circuit capacity, 200 mm wafers represent about 25% of capacity, and almost all the remainder is for wafers of 150 mm or smaller diameter [514]. The choice of wafer size is important for SCE fabrication as fabrication processes and yield depend on the tooling available. Processes developed for one wafer size can require significant changes when migrated to a different wafer size. SCE fabrication on 300 mm wafers has begun and should help inform when or whether the benefits justify the cost [398, 399].

Magnetic layers in superconductor circuits can be fabricated using equipment developed for the general electronics and MRAM industries [515].

2.3.7. Electronic Design Automation (EDA) for SCE

EDA tools developed for semiconductor circuits require modifications to be useful for designing superconducting circuits. For example, inductance—whether self or mutual—is critical in superconducting circuits. Connecting wires must have inductance values within a specified range to allow either pulse transmission or quantized flux storage. Mutual inductance within tight margins is required for the successful operation of logic gates that contain transformers, such as AQFP and RQL, while parasitic inductance and coupling must be minimized to maintain acceptable circuit operating margins. Standard EDA tools have poor inductance extraction capability, ignore the kinetic inductance important in superconductors, and cannot route wiring subject to inductance limits. Numerical inductance solvers are needed, and InductEx [516] is one three-dimensional inductance extraction tool developed for superconductor integrated circuit structures such as logic gates [517].

Pulse-based logic natural to SFQ circuits is not the same as the voltage-state logic for which most EDA tools have been developed. For example, timing parameters in SFQ circuits are state-dependent, and critical timings can exist between any pair of inputs that may exclude the clock [3, 518]. EDA tools for SCE must thus include timing extraction and hardware description language (HDL) model generation tools that handle state-dependent, pulse-based timing characteristics. PyLSE (python language for superconductor electronics) is under development to precisely define the functional and timing behavior of SCE circuits [519]. PyLSE can support traditional SFQ logic (pulse = '1', no pulse = '0') as well as other pulse-to-value mappings such as those used by temporal computing (§ 2.3.1.5) or xSFQ (§ 2.3.1.6).

Quantum flux parametron (QFP) logic circuits have slightly different EDA requirements and tools. One difference is the need for equal currents at the inputs to a gate, which requires path balancing. A semi-custom EDA flow has been developed for QFP logic circuits [520] and a fully-automated flow is under development [521, 522].

EDA for SCE must also address phenomena that do not affect semiconductor circuits. Device-level design and simulation, part of what is traditionally called technology computer-aided design (TCAD), has focused on devices and processes specific to SCE such as Josephson junction devices and Nb sputter deposition [523, 524]. Faults in SCE circuits are different and require fault model development [525]. Flux trapping analysis and mitigation is another important area. Moats in the ground planes of superconductor circuits provide low-energy locations for magnetic flux to trap during cool-down, but flux trapping analysis tools are required to calculate optimal moat positions and analyze the detrimental effects of persistent currents in superconducting loops induced by nearby trapped flux [321]. There has been recent progress on developing the basics of flux trapping analysis tools [526] and the compact model extraction required to incorporate phenomena such as flux trapping and external magnetic fields into simulation and verification tools [322].

The status of EDA for SCE has been reviewed [527, 528, 529, 530] and recent work includes [293, 531, 532, 533, 534, 535, 536, 537]. The ongoing IARPA SuperTools program seeks to develop a complete EDA tool chain for SCE [529, 538, 539, 540] that includes back-end capabilities for device and gate design, and front-end capabilities for behavioral-to-logic and clock tree synthesis and automated placement-and-route methods. Models for Josephson junctions are fundamental to circuit simulation. The RCSJ model is easy to implement in circuit simulators like SPICE, but the accuracy can be inadequate for high-

J_c, self-shunted JJs [541]. Microscopic tunneling models [542] are more accurate but easier to implement in simulators based on superconducting phase like PSCAN2 [543] than in simulators based on voltage levels like SPICE, which has resulted in the rise of dual-capability superconductor circuit simulators such as JoSIM that allows both voltage and phase-based simulation [544]. Phase-based simulation is unique to superconductor electronic circuits and is required for simulations such as trapped flux and its coupling to superconductor circuit structures.

The superconductor EDA tools most used for analog and digital integrated circuit design today are listed in Table CEQIP-9.

Future development needs include the following, by area. **Process TCAD**: sputter and reactive sputter deposition; and Nb/Al-AlO_x/Nb junction fabrication. **Device TCAD**: ferromagnetic junction barriers; nonuniform junction barriers; and large junctions (diameter > 1 μm). **Synthesis**: Sequential and combinational logic cell mixtures; majority-gate logic; ac-power distribution; current recycling in dc-power distribution; asynchronous circuits such as used in temporal logic; mixed-signal circuits; and neuromorphic circuits. **Placement and Routing**: Non-uniform gate height support; and passive transmission line optimization. **Timing**: Sequential and combinational logic cell mixtures; process variation effects. **Multi-chip**: Design tools for 2.5D and 3D integration of homogeneous or heterogeneous technologies. **Design technology co-optimization (DTCO)**: Complete and automated tool chain to enable rapid optimization.

Table CEQIP-9 Superconductor EDA tools

Domain/level	*Application*	*Tool name*	*Highest maturity and scale*	*References*
Physical	Technology CAD	FLOOXS	Academic – 1 device, 2D	[539, 523, 524]
Physical	Parameter/compact model extraction	InductEx, TetraHenry, lmeter, 3D-MLSI	Commercial – 10^3 devices	[516, 322]
Physical	Electrical simulation	JSIM, JoSIM, WRSpice, HSPICE	Commercial – 10^5 devices	[544]
Physical	Layout-versus-schematic verification	SpiRA	Academic – 10^3 devices	
Digital system	Logic simulation	iVerilog		
Digital system	Synthesis, place and route	qPALACE, unnamed tools for AQFP	Academic – 10^4 logic cells	[520, 533, 539]

2.3.8. PACKAGING AND TESTING FOR SCE

Superconductive multichip module (S-MCM) technology has been developed for superconductor chips [545, 546, 547]. The most advanced process can make S-MCMs up to 96 mm × 96 mm using interposers with 4 layers of Nb and 0.8 μm to 1 μm minimum linewidth fabricated on 200 mm silicon wafers [547]. The S-MCM roadmap is summarized in Table CEQIP-18.

Packaging for cryogenic optoelectronic devices is reviewed by [548].

Semiconductor chips are typically tested before wafer dicing and packaging of good die. Systems capable of wafer testing at cryogenic temperatures can greatly reduce testing time while increasing throughput [549, 550]. Thermally induced voltage alteration (TIVA) is a room-temperature failure analysis technique recently found useful with SCE circuits [551, 552]. Needed is research on the extent to which TIVA at room temperature can take the place of circuit testing at cryogenic temperatures.

Failure analysis (FA) techniques for SCE are largely similar to those for other nanoelectronic technologies, but with some different materials and concerns [553].

2.3.9. INTERCONNECTS FOR SCE

Within the cryogenic environment, superconductors can be used for both power and data. Niobium has a superconducting critical temperature T_c of about 9 K and has been used to make coaxial cables [554] as well as flexible ribbon cable transmission lines on thin film polyimide [555, 556]. NbTi has a similar critical temperature, but lower thermal conductivity, and has also been used to make coaxial cables [557] and microstrip ribbon cables [558]. Electroplated rhenium (Re) in multilayers with noble metals has an enhanced critical temperature of about 6 K and could have fabrication advantages [559]. YBCO on Kapton has low losses up to about 60 K [560].

On-chip communication using Josephson transmission lines (JTLs) or passive transmission lines (PTLs) is covered in section **2.3.4.4**.

Chip-to-chip communication using SFQ pulses has been demonstrated at data rates up to 117 Gbit/s over microstrip lines 6.4 mm long [561] and up to 82 Gbit/s over microstrip lines almost 20 mm long [546]. Double-flux-quantum pulses can be used for longer distances or improved signal-to-noise ratio [317]. ERSFQ circuits for 16-bit parallel data transmission have been demonstrated [562]. Board-to-board communication has been demonstrated using Nb flex cable [556].

Power and data need to move between the cryogenic and room temperature environments with very low heat load to the cryogenic environment. Most challenging is movement of data from a cryogenic environment due to the small energy in an SFQ pulse and the refrigeration penalty on any energy dissipated in amplifying or converting signals at cryogenic temperatures [563]. Placing signal amplifiers at multiple temperature stages can reduce total power dissipation [564, 565, 566, 567]. Electro-optical approaches proposed or under development include direct conversion [568, 569] and modulation [570, 571]. Nanowire cryotrons can produce electrical signals at the ~ 1 V level necessary to drive conventional semiconductor electronics [572].

Hybrid superconductor-semiconductor digital data links are covered in section 3.3.3.3.

The interconnect roadmap is summarized in Table CEQIP-19.

2.3.10. REFRIGERATION

Cryogenic cooling technologies have developed steadily over the past few decades based on various well documented thermodynamic heat engine cycles moving the industry away from a reliance on liquid cryogens towards new cryogen-free closed cycle apparatus [573, 574]. This has been beneficial for the research community and is increasingly being adopted for industrial and medical applications. It is estimated that helium usage for low-temperature physics is approximately 4% of global helium consumption and declining [575]. Not only does this enable greater access to cooling technologies through reduced operating costs, ease of use, reduced safety considerations and reduced reliance on access to liquefiers and gas supply chain it has also introduced a change in design considerations. Gone are the constraints placed on vessel size and shape considerations due to optimal cryogenic consumption performance such as neck diameter for services, cabling, cryoelectronics thermalization and staging. New considerations include available cooling powers at intermediate temperatures, the interdependence of the available cooling power at these stages, mechanical vibrations, electrical & acoustic noise, and utility & power requirements. Furthermore, applications with ‘ride through’ or ‘duty cycle’ requirements such as MRI and gyrotron beamline injection magnets have already demonstrated that hybrid structures utilizing a helium bath with integrated closed cycle cooler continuously recondensing the boiling liquid can maintain steady state operation for long term continuous operation.

Cryogenic technologies require refrigeration, unlike most other beyond CMOS technologies. Comparison at room temperature, taken as 300 K, requires accounting for the power cost of cryogenic refrigeration. The specific power of a refrigerator is defined as the input power divided by the cooling power. Note that specific power is the inverse of the coefficient of performance (COP). The specific power of an ideal Carnot refrigerator varies with temperature as $(T_H - T_L)/(T_L)$ where T_H is the high temperature at which heat is rejected and T_L is the low temperature at which cooling takes place. Cryogenic refrigeration system efficiency, and thus specific power, varies depending on cold-end temperature, refrigeration capacity and design [576, 577].

The approach taken is to use box plot statistics for specific cooling powers of commercial refrigeration systems at cold-end temperatures of interest. The effect of refrigeration can be presented using a simple whisker plot using only the minimum, median, and maximum specific power values rather than a full box plot. Specific powers for benchmarking and metrics use are summarized in Table CEQIP-10 and plotted in Figure CEQIP-5. The empirical fit shown in the figure (specific power ~ T_{cold}^{-2}) has no known basis, but does show that refrigeration cost tends to grow rapidly as the operating temperature decreases. Details are in Table CEQIP-11 through Table CEQIP-13. Note that refrigeration at T ~ 4 K is split into high- and low-power groups as their performance characteristics too different to combine. Low-power refrigerators for T ~ 4 K are often called cryocoolers. Cryogenic refrigeration systems for T ≤ 1 K are listed in Table CEQIP-13 and are typically dilution refrigerators [578].

Needed is a model for specific power values at other temperatures, perhaps using cryogenic refrigeration performance models [579, 580]. Such a model might be used to produce nominal values that are less sensitive to the collection of existing refrigerators. Improvements in efficiency are desirable and seem possible, although higher efficiency approaches are likely to cost more [581].

Table CEQIP-10 Specific Power Ranges for Cryogenic Refrigeration

T cold	*Cooling Power Range*	*Specific Power * [W/W]*			
		Average	*Low*	***Median***	*High*
80 K	1.4 W to 190 kW	5.40E+01	7.18E+00	**3.76E+01**	1.50E+02
40 K	1.1 W to 61.5 kW	1.69E+02	2.17E+01	**9.31E+01**	7.50E+02
20 K	2 W to 320 W	4.56E+02	1.17E+02	**3.82E+02**	1.30E+03
4.5 K	(≥ 10 W) 120 W to 1000 W	4.87E+02	3.15E+02	**5.14E+02**	6.88E+02
4.2 K	(< 10 W) 0.08 W to 2.7 W	9.24E+03	3.82E+03	**7.40E+03**	3.75E+04
100 mK	0.25 mW to 1.0 mW	3.22E+07	1.27E+07	**2.78E+07**	6.25E+07
20 mK	6 μW to 30 μW	1.09E+09	4.56E+08	**1.00E+09**	2.08E+09

* Specific power: (W at 300 K)/(W at T cold)

Table CEQIP-11 Cryogenic Refrigeration Systems for T > 10 K

Table CEQIP-12 Cryogenic Refrigeration Systems for 1 K < T ≤ 10 K

Table CEQIP-13 Cryogenic Refrigeration Systems for T ≤ 1 K

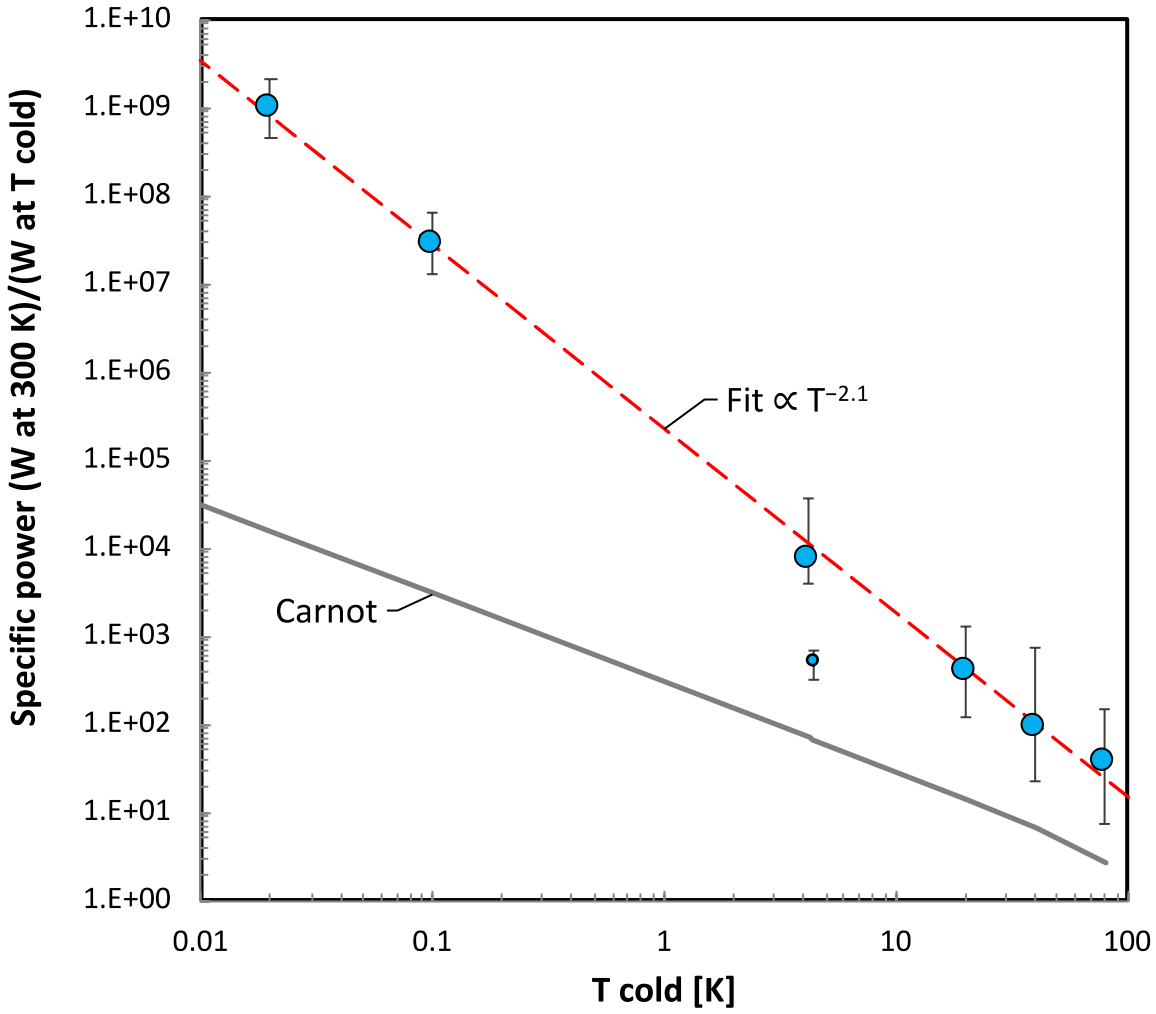


Figure CEQIP-5 Specific Power versus Cold Temperature for Cryogenic Refrigeration

At T ~ 4 K, • is for large systems (>10 W cooling power) and ● is for small systems.

2.4. Benchmarking and Metrics for SCE

Beyond-CMOS electronics must consider new devices, circuits, and architectures. Determining which emerging or novel technologies are most promising and thus most deserving of development effort can be difficult, especially for significantly non-conventional technologies such as cryogenic electronics. Fair and effective metrics and figures of merit are needed for comparison.

2.4.1. Device and Circuit Benchmarking

Recently, there have been efforts to benchmark a variety of beyond-CMOS technologies [582, 583, 584, 585]. Nikonov and Young [582] included in traditional energy-delay comparisons some state variables other than voltage (e.g., magnetization, polarization, spin current, orbital state) and extended comparisons from switching devices alone to logic circuits as large as an arithmetic logic unit (ALU). Still, the existing benchmarks and metrics did not consider superconductor electronics and are limited as computing also requires interconnects and memories, not just logic circuits.

First, consider intrinsic device switching energy versus switching time (delay) and how to add superconductor electronics to existing comparisons. Nikonov and Young include data for beyond-CMOS devices fabricated at the 15 nm scale in Table 5 of

their supplemental material [582]. For Josephson junctions in RQL technology with critical current density J_c = 100 μA/μm^2 and device current I_c = 100 μA, the intrinsic switching energy $E_{sw} = I_c\Phi_0/3$ = 69 zJ [123, 134]. The intrinsic switching time is taken as the SFQ pulse width, roughly FWHM [586, 587], $t_{sw} = (\pi\Phi_0 C_s/2J_c)^{1/2}$ = 1.5 ps with specific capacitance C_s = 70 fF/μm^2 typical of junctions with this J_c.

AQFP-based logic is a benchmarking challenge as the switching device is a circuit that moves between two states semi-adiabatically. The switching energy depends on ramp rate as $E_{sw} = 2I_c\Phi_0\, t_{sw}/t_x$, where t_x is the excitation time [134, 160] The intrinsic switching time is $t_{sw} = (2\pi\Phi_0 C_s/\beta_c J_c)^{1/2}$ = 0.21 ps for the AIST, Japan ADP2 junction fabrication technology with J_c = 100 μA/μm^2, specific capacitance C_s = 63 fF/μm^2, and unshunted junctions with damping parameter β_c = 190. For a 5 GHz clock frequency with t_x = 100 ps and I_c = 50 μA, E_{sw} = 0.43 zJ. For AQFP gates, the delay is given not by the intrinsic junction switching time t_{sw} or by the excitation time t_x, but by the clock period divided by the number of phases. For 4-phase clocking at 5 GHz, the delay is 50 ps. Multi-excitation AQFP (ME-AQFP) [138] could increase clock frequency to 20 GHz and reduce the delay to 12.5 ps, however the energy-delay product remains constant, so the energy would increase by a factor of 4 to 1.7 zJ.

Figure CEQIP-6 shows the energy versus delay for several switching devices including RQL and AQFP. The energy-delay product for these superconducting logic technologies is seen to be competitive, even including the cost of cryogenic refrigeration. This is due to the fact that the energy-delay product is the ratio of the consumed power by the square of the speed (clock frequency) of the circuits. Since the power is fixed by external constraints (cost, volume, mass, etc.) this factor is fixed for a given application, independently from the technology that is used. Then speed, hence superconductors, come into play.

Next, consider interconnects. The energy versus delay for beyond-CMOS interconnects of 10 μm length is plotted in Figures 7 and 8 of Pan and Naeemi [585]. For RQL, Dorojevets, et al. [588] give data transfer energies for 32-bit Josephson transmission lines (JTL) and passive transmission lines (PTL) with I_c = 38 μA in their Figure 1. On a per-bit basis and removing the refrigeration allowance, the transmission energies for a 1 mm distance are (6.3 fJ)(1000 μm)/[(50 μm)(96 bit)(1000 W/W)] = 1300 zJ/bit for 100 μm by JTL and (12.5 fJ)/[(96 bit)(1000 W/W)] = 130 zJ/bit for up to 20 mm by PTL. The delay for a JTL is about an SFQ pulse width times the number of JTL cells t_{JTL} = (1.5 ps)(1000 μm)/(25 μm) = 60 ps. A PTL consists of 2 JTL cells on each end of a ballistic transmission line, so the delay for a PTL is t_{PTL} = (4)(1.5 ps) + (1000 μm)/(100 μm/ps) = 16 ps, where c/3 ≈ 100 μm/ps is the approximate speed of propagation on the PTL. Note that JTLs and PTLs have different characteristics beyond energy and delay. For example, the repeater distances are 25 μm for JTL versus 20 mm for PTL, and area is required from different layers. For JTLs and PTLs in the RSFQ logic family, see [313].

AQFP gates output currents, not SFQ pulses, and have different interconnect characteristics. Buffer (repeater) cells have the energy and delay of a single AQFP gate with a maximum drive distance of about 1 mm [589]. AQFP (5 GHz) interconnect energy and delay are thus 0.43 zJ and 50 ps for distances of 0 to 1 mm. For 20 GHz operation the delay decreases to 12.5 ps, and the energy increases to 1.7 zJ.

Figure CEQIP-7 shows the energy versus delay for interconnects of 1 mm length including RQL and AQFP. The energy-delay product for these superconducting logic technologies is seen to be better than the alternatives, even including the cost of cryogenic refrigeration. This plot for interconnects of a single length does not show that the energy remains the same for AQFP out to 1 mm and for PTL (RQL) out to 20 mm. Note that an error was made in the equivalent 2017 figure (BC4.1b) that made the differences appear smaller: the alternative technologies were plotted for 10 μm length and the superconductor technologies for 100 μm length, 10 times longer.

Some applications require the electronics to operate at cryogenic temperatures. Examples include some digital-RF receivers, focal plane arrays for astronomy, quantum computing, and magnetic resonance imaging (MRI). For operation at 4 K, all technologies would require refrigeration, in which case RQL and AQFP have a clear advantage.

A generalized methodology for comparing superconductor electronics with other technologies will require several developments. To avoid the effort of full-circuit simulations, performed in [588], models must be developed for energy, delay, and circuit area for a variety of superconductor technologies. The effort can start from previous work such as [134, 590, 591], but will need to be extended considerably. Metrics are needed that allow comparison of technologies at very different feature sizes. Interconnect benchmarking is needed as a function of transmission distance. Clocking delay must be included for logic families such as RSFQ that require clocking of each gate.

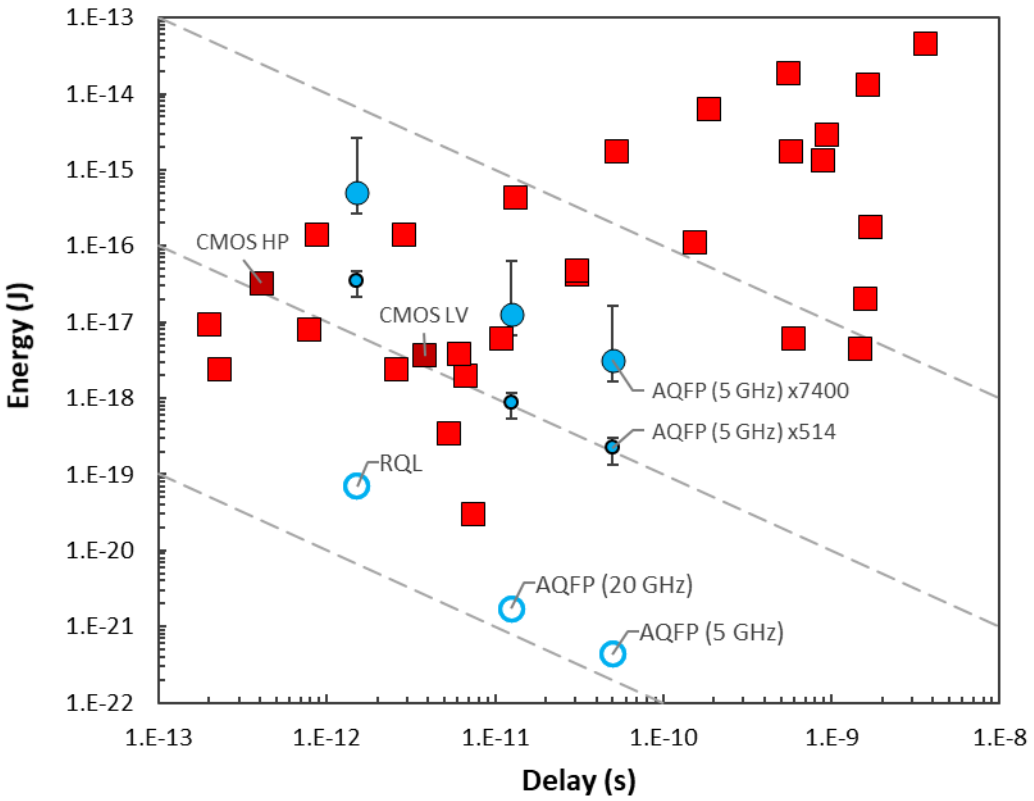


Figure CEQIP-6 Energy versus Delay for Intrinsic Elements

Note: Superconductor devices (AQFP, RQL) have open circles ○ for operation at ~4 K and solid circles with whiskers showing ranges including refrigeration power from Table CEQIP-10. The ● is for large refrigeration systems (>10 W cooling power) and ● is for small systems (cryocoolers). All other devices are from [585]. Dashed lines show constant energy-delay products.

Table CEQIP-14 Energy versus Delay for Intrinsic Elements

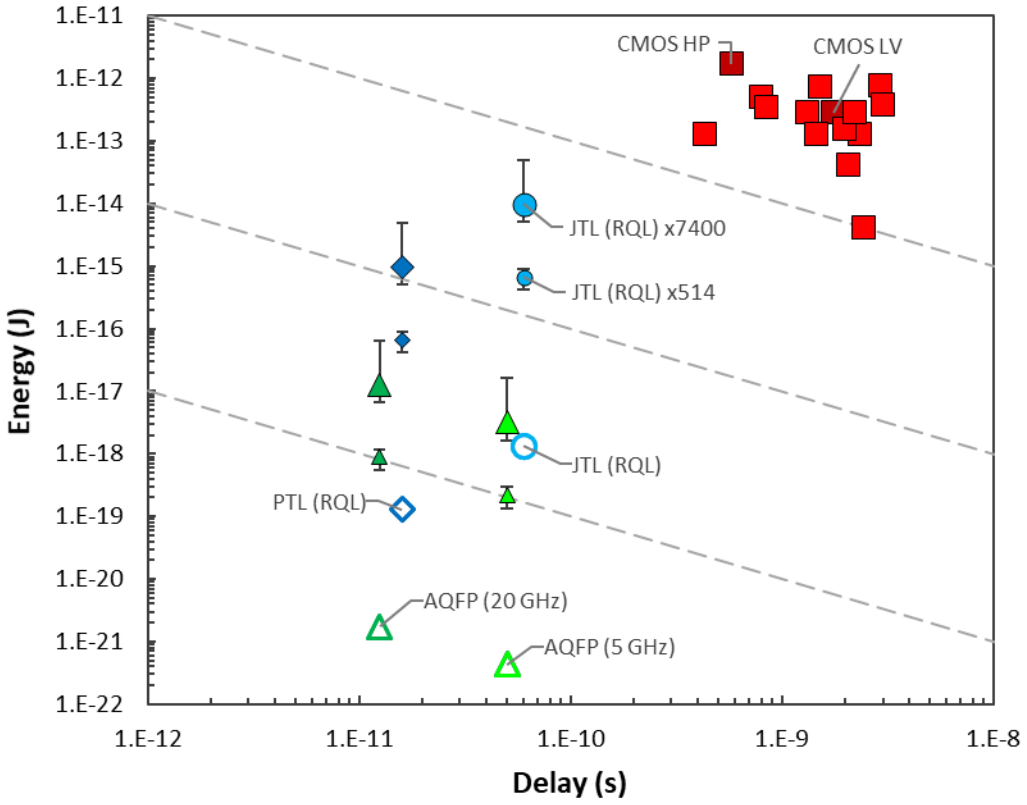


Figure CEQIP-7 Energy versus Delay for Interconnects of 1 mm Length

Note: Superconductor devices (AQFP, RQL) have open symbols (e.g., ○) for operation at ~4 K and solid symbols with whiskers showing ranges including refrigeration power from Table CEQIP-10. Small, solid symbols (e.g., ●) are for large refrigeration systems (>10 W cooling power) and large, solid symbols (e.g., ●)are for small systems (cryocoolers). All other devices are from [585]. Dashed lines show constant energy-delay products.

Table CEQIP-15 Energy versus Delay for Interconnects of 1 mm Length

Table CEQIP-15b Energy versus Delay for Interconnects of 0.01 to 1 mm Length

2.4.2. SCALING OF DEVICES AND CIRCUITS

As introduced in section 2.1, single flux quantum (SFQ) digital circuits use superconducting loops. The superconducting phase must be continuous and single valued at any point around the loop, which requires that the phase change around the loop must be an integer multiple of 2π. For a superconducting loop with inductance L and circulating current I, the requirement is that the loop contain magnetic flux $n_{fq} \Phi_0 = LI$, where n_{fq} is an integer and Φ_0 is the magnetic flux quantum. Josephson junctions in the loops limit the circulating supercurrent to I_c, thus the required inductance is $L = n_{fq} I_c/\Phi_0$, where the value of n_{fq} is between about 0.5 and 1.5, depending on whether a loop is intended to store a flux quantum ($n_{fq} > 1$) or not (< 1). Scaling the loops to smaller sizes depends on scaling both the inductive elements and Josephson junctions. Phase shift can be provided by devices other than inductors, as noted in section **2.3.4.2**.

Scaling of phase shift elements should consider system-wide effects. For example, the bias current supply network can more than double the power, energy, or area required by the functional portion of the circuit. A study of phase shift element scaling, costs, and benefits is needed to construct a technology roadmap.

2.4.3. SYSTEM AND APPLICATION BENCHMARKING

Pan and Naeemi [584] make the case that some beyond-CMOS devices offer fundamentally different or unique characteristics best suited to novel circuit implementations not well evaluated by traditional metrics and benchmarks. Needed are methods to more accurately predict the performance of computing systems based on emerging technologies or approaches to computing. Metrics for cryogenic electronics are expected to start with figures of merit comparing performance (e.g., computation, data movement, memory capacity) against required resources such as chip area.

2.5. ACTIVE RESEARCH QUESTIONS FOR SCE

Difficult challenges for SCE are described in Table CEQIP-16. Future work includes identification of key challenges and tracking of active research.

Table CEQIP-16 Difficult Challenges for SCE

Near-Term Challenges: 2022–2028	*Description*
Logic (current implementations)	Many competing approaches. Sensitivity to magnetic fields and fabrication variation. Supply current is mostly spent biasing junctions. Power and clock pulse distribution add complexity and jitter. Josephson junctions: • Range of sizes needed ~ 4:1 • Requires critical current variation Ic < 2% AC powered using transformers in series: • RF distribution (5 to 20 GHz) • Transformers don’t scale well DC powered: • Parallel junction biases add up to large supply current • Resistors dissipate too much static power (~ 10x dynamic) or large inductors take too much area • Clock pulse distribution adds complexity and jitter
Current supply	Thermal noise requires junction critical current Ic ≳ 100 μA at 4 K. DC supply current is ~ 0.7 I_C per junction, so chip supply current becomes too large for > 1 million junctions. AC powered using transformers in series requires RF distribution (5 to 20 GHz) and transformers don’t scale well.
Integrated circuit fabrication processes	Foundries for commercial production now process 200 mm or smaller wafers using equipment lacking state-of-the-art capability. Achieving the yield and throughput for large-scale applications will require process improvements and, possibly, a move to 300 mm wafers. Temperatures are currently limited to < 200 °C, which requires different processes than CMOS technology, which has a limit of 400 °C. Circuit approaches and fabrication processes are interdependent, requiring co-development. Planarization and thickness control are challenging in stacks of multiple superconductor layers when the layer thicknesses remain the same, rather than increasing with layer number as in CMOS back-end processes. Magnetic materials might be needed.

Near-Term Challenges: 2022–2028	*Description*
Temperature limits compatible with CMOS fabrication processes	Nb/Al-AlO_x/Nb Josephson junctions are sensitive to temperature. Fabrication processing temperatures are currently limited to less than 200 °C, which requires different processes than those used in CMOS technology, which has a limit of 400 °C. A different barrier to allow use of standard CMOS processes would allow access to existing processes used to make fine features and reduce process development costs, but requires new barrier development.
Device variability	Variation in device parameters reduces the operating margins of circuits. Needed is better process control, better device designs, or circuit designs that tolerate or compensate for device variability.
Memory	Multiplexing is difficult for single-flux-quantum logic New materials and processes add cost
High critical current density junctions (J_c > 100 μA/μm^2)	The AlO_x barrier in Josephson junctions with J_c = 100 μA/μm^2 is now approximately 1 nm thick. Thinner barriers increase J_c, allowing smaller and faster JJs. For J_c > 500 μA/μm^2 the sub-gap resistance can be sufficiently low to eliminate the need for shunt resistors. Uniformity control will be challenging as defects typically dominate conduction through thinner barrier layers and thickness control is also difficult. Materials and process development is needed to improve uniformity and control of devices with high J_c.
Superconducting materials with higher critical temperature (T_c)	Higher T_c materials would allow operation at higher temperatures, which would significantly reduce the required cooling power, or would make circuits less sensitive to self heating at temperatures well below T_c. Niobium (Nb) is the superconducting material most common for 4 K applications. Changing the superconducting material would require significant development and might also require changes in the junction barrier. Processes for large-scale integrated circuit fabrication require multiple superconductor layers, vias, and high-uniformity junctions. Changes in other materials-dependent properties such as magnetic penetration depth λ, superconducting coherence length ξ, and kinetic inductance would require redesign of devices and circuits.
Magnetic materials fabrication process integration	Magnetic materials are desired to make both memory and passive devices and can enable compact high-value inductors and high-coupling factor mutual inductances. Integrating magnetic materials into foundry processes will be difficult. Materials and device geometries with lower magnetization are needed to reduce switching energy. Magnetic properties at room and cryogenic temperatures do not seem to correlate, so measurement is required until adequate theory can be developed. Better fixed magnetic layer materials are needed as nickel has problems that will prevent scaling to small sizes. Interface roughness and morphology must be controlled for good magnetic properties.
Electronic design automation (EDA) tools	EDA tools for SCE need to support logic styles that use few or no clocked gates. Technology CAD (TCAD) is needed for junctions containing magnetic materials.

Near-Term Challenges: 2022–2028	*Description*
Switching devices	Fan-in or fan-out greater than one requires additional circuitry due to the low gain and low isolation provided by Josephson junctions (in contrast to semiconductor transistors). SFQ-compatible devices with greater gain and isolation are under development, but not yet proven in large-scale fabrication.
Transformer miniaturization or replacement	Current transformers rely on magnetic coupling between inductors, which seems difficult to scale to very small dimensions. Needed are transformer alternatives or scaling approaches that allow significantly higher logic gate and memory cell density.
Shrinking devices and interconnects at dimensions of tens of nanometers	State of the art superconductor circuits have Josephson junctions with diameters down to 200 nm and some feature sizes down to about 90 nm. These dimensions are much larger than state-of-the-art CMOS but are limited by the superconductor coherence length (~45 nm for Nb) required for good properties. Shrinking dimensions below the coherence length of Nb will require either operation at reduced temperatures or alternative superconducting materials.
Switching device scalable below 200 nm	Nb/Al-AlOx/Nb Josephson junctions are almost good enough. Alternatives will require different materials and fabrication processes, possibly including magnetic materials. AlOx barriers: • Smaller sizes require critical current density $Jc > 100\ \mu A/\mu m^2$ • Device property variation increases for barrier thickness < 1 nm • Temperature limits < 200 °C make gap fill difficult Nb electrodes: • Superconducting coherence length requires dimensions $\gtrsim$ 45 nm • Large grain size causes variability • Getter material with superconducting properties sensitive to O, H • Several oxides with different properties Nanobridges are sensitive to dimensional variations
3-terminal switching device	Small available flux ~ 2 mA·pH or voltage ~ 1 mV. Fabrication more difficult than the traditional tri-layer device.
Interconnects, on-chip and chip-to-chip	Superconducting passive transmission lines (PTLs) used for ballistic transport of SFQ pulses must have low impedance to match the low impedance available from Josephson junction drivers. Grounded shields are also required to reduce crosstalk, which require more area and reduce circuit density. Also needed are higher-impedance Josephson junctions or methods for making smaller transmission lines with lower impedance.
Interconnects between cryogenic and room temperature environments	Interconnects for both digital and analog signals require careful optimization to balance electrical and thermal properties. Use of cryogenic semiconductor and photonic components in data links require further development.
Packaging for SCE	Operation at cryogenic temperatures requires different materials, packaging, testing, and cooling systems, much of which will require new development. State-of-the art systems package a few superconductor ICs in a commercial cryostat. Scaling up to systems with higher complexity chips and multi-chip modules will require further reduction of power consumption by all components. Josephson junctions are extremely sensitive to magnetic fields and require shielding, which becomes more challenging as system volumes grow.

Long-Term Challenges: 2030–2037	*Description*
Develop circuit approaches scalable to applications with significant markets	Digital signal processing, high speed (> 10 GHz) Neuromorphic computing Quantum computing control Digital computing at large scale
Cryogenic refrigeration	The cost of refrigeration can be prohibitive for small systems that do not require a cryogenic environment for some other reason. Cryogenic refrigerators have improved immensely, driven in part by the requirement for the trouble-free operation of MRI systems in hospitals. Still, improvements in the efficiency of small refrigerators (less than 1 W at 4 K) would reduce the system size for which superconducting computing becomes competitive. More efficient or lower cost refrigeration systems for temperatures below 10 K would help to reduce operating costs.
Optical input/output (I/O)	Heat budget in the low-temperature environment is very low. Optical data links require development of efficient SFQ-to-optical converters.
Cost	Costs of superconductor electronic devices, circuits, and systems are presently high, partly due to low fabrication volumes and low circuit density.
Higher temperature (T_c) superconductors	The energy-delay product of a digital gate is given by the power consumption divided by the square of the speed. It gives a good advantage to superconductors, counterbalanced by the fact that the integration density is currently much smaller than for CMOS. Moreover, interconnects are necessary for complex multi-chips systems and their limitations between chips and between temperature stages will dominate the ultimate system performances. The use of self-shunted Josephson junctions with T_c above 30 K and with R_nI_c products in the 5-10 mV range is very challenging, but would open the range of applications and increase circuit performance significantly, for example: clock frequencies close to 1 THz, reduced need for signal amplification for transmission to room temperature environments, much more energy-efficient refrigeration above 20 K, and higher circuit density in absence of external shunt resistors.

2.6. ROADMAPS FOR SCE

Of the areas covered by this report (SCE, cryo-semi, QIP), the largest market potential and need for improved capability are in the SCE and QIP areas. A roadmap for SCE will be developed first as the technology and needs are better understood. Past SCE roadmapping efforts provide a base for future efforts [14, 527, 587, 592, 593, 594, 595, 596, 597, 598].

The roadmap for fabrication of digital SCE circuits is summarized in Table CEQIP-17, with additional information in the linked spreadsheet.

Foundry and fabrication are key technology areas for SCE and face some challenging decisions. Foremost is identification of suitable foundries. Of the facilities currently capable of producing complex superconductor circuits (> 100,000 Josephson junctions), some are not allowed to produce commercial products, and others have limited access. Preferred are multiple foundries that can handle the materials specific to SCE and produce commercial products with sufficient yield. Multi-project wafer (MPW) service is desirable and will require well-characterized processes and more complete process design kits (PDKs) than currently available.

New materials, processes, and devices will need to be developed. Approaches to increase circuit density and complexity include: smaller feature sizes, stud vias, high sheet resistance layer, increase critical current density J_c, self-shunted JJs, increase wiring layers, multiple JJ layers, high kinetic inductance layers, magnetic JJs, stacked JJ inductors, or ac-to-dc rectifiers. How

these will be developed and incorporated into the foundries is an open question. The achievable rate of progress must be considered.

Table CEQIP-17 Fabrication Roadmap for Superconductor Electronics (SCE) – Digital Circuits

Year	2022	2023	2024	2025	2026	2027	2028
Digital SCE Fabrication							
"Node Range" label (nm)	**"250"**	**"250"**	**"150"**	**"150"**	**"150"**	**"150"**	**"90"**
Substrate material, maximum size (mm)	Si, 200	Si, 200	Si, 200	Si, 200	Si, 200	Si, 200	Si, 300
Wiring							
Superconductor	Nb	Nb	Nb	Nb	Nb	Nb	Nb
Superconductor layers	**8**	**8**	**10**	**10**	**10**	**10**	**12**
Linewidth, minimum (nm)	**250**	**250**	**150**	**150**	**150**	**150**	**90**
Ic, minimum (μA/)	**200, 1200**	**200, 1200**	**100, 580**	**100, 580**	**100, 580**	**100, 580**	**50, 290**
Junctions, Switching							
Junction materials	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx
Junction layers	**1**	**1**	**2**	**2**	**2**	**2**	**2**
Junction critical current densities, Jc (μA/μm^2)	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**
Minimum junction diameter (nm)	**500**	**500**	**350**	**350**	**350**	**350**	**250**
Minimum junction critical current, Ic (μA)	**20, 118**	**20, 118**	**10, 58**	**10, 58**	**10, 58**	**10, 58**	**5, 29**
Killer defect density per layer (1/cm^2)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**
Jc wafer-to-wafer variation	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
Maximum relative spread (σ/Ic) at minimum Ic	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
Junctions, Magnetic (Pi)							
Junction materials			Ni	Ni	Ni	Ni	Ni
Junction layers	0	0	1	1	1	1	1
Junction critical current densities (μA/μm^2)			**3000**	**3000**	**3000**	**3000**	**3000**
Junction diameter, minimum (nm)	**500**	**500**	**350**	**350**	**350**	**350**	**350**
Resistors							
Resistor material	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx
Resistor layers	1	1	1	1	1	1	1
Resistor sheet resistance (Ω/□)	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**
HKI (high kinetic inductance) Layers							
HKI material	MoNx	MoNx	NbNx	NbNx	NbNx	NbNx	NbNx
HKI layers	1	1	1	1	1	1	1

The superconductor multi-chip module (S-MCM) roadmap is summarized in Table CEQIP-18. Future packaging and integration roadmaps might include parameters such as contact count and layout, or memory interface specifications. A goal of this roadmap is to avoid duplication of roadmaps for conventional electronics and to maintain compatibility where possible [599].

Table CEQIP-18 Fabrication Roadmap for Superconductor Electronics (SCE) — S-MCM

Year	2022	2023	2024	2025	2026	2027	2028
MCM Substrate Fabrication							
Substrate material, maximum size (mm)	Si, 48x48	Si, 96x96	Si, 96x96	Si, 200	Si, 200	Si, 200	Si, 300
Superconductor	Nb	Nb	Nb	Nb	Nb	Nb	Nb
Superconductor layers	**4**	**6**	**6**	**6**	**6**	**6**	**8**
Linewidth, minimum (nm)	**800**	**800**	**800**	**800**	**800**	**800**	**800**
Superconductor	Nb	Nb	Nb	Nb	Nb	Nb	Nb
Impedance, single-ended (Ω)	**50**	**50**	**50**	**50**	**50**	**50**	**50**
Loss (dB/m), crosstalk (dB)	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**

The interconnect roadmap is summarized in Table CEQIP-19, with additional information in the linked spreadsheet. Interconnects can be in forms such as wires or ribbon cables and the materials can be superconducting, normal metal, or optical.

Table CEQIP-19 Interconnect Roadmap for Cryogenic Electronics

Year	2022	2023	2024	2025	2026	2027	2028
Cables, Superconducting, < 5 K							
Cable type	Flex Cable, Microstrip	Flex Cable, Microstrip	Flex Cable, Microstrip	Flex Cable, Stripline	Flex Cable, Stripline	Flex Cable, Stripline	Flex Cable, Stripline
Superconducting material, Tc (K)	NbTi, 9	NbTi, 9	NbTi, 9	NbTi, 9	NbTi, 9	NbTi, 9	NbTi, 9
Data rate per lane (Gb/s)	**15**	**15**	**15**	**15**	**30**	**30**	**30**
Lanes per cable	**10**	**10**	**10**	**10**	**20**	**20**	**20**
Pitch (mm)							
Edge data rate (Gb/s-mm)	**100**	**100**	**100**	**100**	**400**	**400**	**400**
Impedance (Ω)	**5 to 50**	**5 to 50**	**5 to 50**	**5 to 50**	**5 to 50**	**5 to 50**	**5 to 50**
Loss (dB/m), crosstalk (dB)	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**
Connector type							
Cables, 4 to 60 K							
Cable type	Flex Cable, Microstrip	Flex Cable, Microstrip	Flex Cable, Microstrip	Flex Cable, Stripline	Flex Cable, Stripline	Flex Cable, Stripline	Flex Cable, Stripline
Superconducting?	Partial	Partial	Partial	Partial	Yes	Yes	Yes
Superconductor	ReBCO	ReBCO	ReBCO	ReBCO	ReBCO	ReBCO	ReBCO
Data rate per lane (Gb/s)	**15**	**15**	**15**	**15**	**30**	**30**	**30**
Edge data rate (Gb/s-mm)	**100**	**100**	**100**	**100**	**400**	**400**	**400**
Impedance, single-ended (Ω)	**50**	**50**	**50**	**50**	**50**	**50**	**50**
Loss (dB/m), crosstalk (dB)	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**	**< 2, < −40**

3. CRYOGENIC SEMICONDUCTOR ELECTRONICS (CRYO-SEMI)

3.1. INTRODUCTION

Reasons for operating semiconductor electronics at cryogenic temperatures include: 1) performance improvement (e.g., lower noise, higher speed, increased efficiency) or 2) to support a sensor, actuator, or other device in a cryogenic environment. For a brief introduction, see [600].

In the 1980s ETA Corporation built several computers with as many as 2000 CMOS chips operating in liquid nitrogen [601]. More recently, commercial cryogenic electronic components were evaluated for suitability at 4.2 K and used successfully to build a complete digital to analog multiplexer [602].

In addition to cryogenic CMOS circuits, bipolar technologies (e.g., SiGe heterojunction bipolar transistors) offer advantages in higher operating speeds when cooled to lower temperatures. While standalone cryogenic semiconductor circuits may not offer a compelling advantage over their room-temperature counterparts due to the higher power consumption required for cryogenic refrigeration, they might in applications requiring cryogenic devices and circuits. Since cryogenic semiconductor devices operate over a wide range of temperatures, one can optimize the overall power consumption of a hybrid-temperature system by selecting the appropriate operating temperature of different cryogenic semiconductor circuits and subsystems. In combination with superconductor electronics, a wide range of cryogenic semiconductor circuits have potential use. These include memory, processor, and amplifiers for digital data links [564, 565, 566], as well as microwave analog signals.

General references include [603, 604]. A review by Valentine and McCluskey covers cryogenic semiconductor devices and packaging [605].

3.2. APPLICATIONS AND MARKET DRIVERS FOR CRYO-SEMI

Advances in cryogenic semiconductor capabilities historically have been driven by the needs of sensors such as low-bandgap semiconductor detectors operated at cryogenic temperatures. Applications tended to be in the medical, scientific and aerospace/defense markets. In recent decades, the rapid improvement of semiconductor performance following to Moore's law and Dennard scaling made development of cryogenic semiconductors for higher performance too difficult to justify. However, as Moore's law nears its end and new paradigms are being explored for high-performance computing, cryogenic semiconductors could play an enabling role.

Quantum computing research and development is driving increased investment in cryogenic electronics, including cryogenic semiconductors. Quantum computers that operate at cryogenic temperatures require communication with and control by classical (non-quantum) electronic systems. The closer the classical systems can operate, both in distance and temperature, the better. Cryogenic semiconductor electronics developed for quantum computing is also finding applications elsewhere. For example, Rambus initially started development of cryogenic semiconductor memory in support of quantum computing efforts at Microsoft, but more recently has been pursuing broader applications that benefit in power/performance metrics [606].

Application areas and market drivers considered by the IRDS Systems and Architectures (SA) and Application Benchmarking (AB) teams [13] are shown in Table CEQIP-20. Current status of applications in operating temperature ranges above and below 10 K are covered in § **3.3.2** and § **3.3.3**, respectively.

Table CEQIP-20 Matrix of Application Areas and Market Drivers for Cryogenic Semiconductors

Application Areas	Market Drivers			
	Aerospace/Defense	Cloud	Scientific	Medical
Sensors & Sensor Interfaces	G		G	G
ADC/Mixed Signal	G		X	X
Digital Logic	X	P	X	
Memory	X	X, P		

X: important application; G: critical gating application; P: power-sensitive application.

3.3. Present Status for Cryo-Semi

3.3.1. Transistor Characterization and Modeling

While some semiconductor devices and circuits have been found to function at cryogenic temperatures, design and optimization specifically for cryogenic operation will require further device characterization and model development.

Early work showed that MOSFET models covering a large temperature range from cryogenic to room temperatures need to consider incomplete ionization in addition to the usual expressions for temperature dependence in compact models [607, 608]. As a first step to a full compact model ranging from 4.2 K to 300 K, long channel equations covering the full temperature range were developed and verified against experiment [609]. Recent work includes [610].

Transistor characterization was extended over time to more modern technologies, either down to 77 K [611, 612, 613] or to near 4 K [614, 615, 616, 617]. One publication studies behavior at 4 K and at 100 mK and discusses compact modeling, while showing that the region both < 40 nm and < 4 K remained unexplored [618]. On-chip microwave passive components have been characterized and modeled in 40 nm CMOS up to 30 GHz at 4 K [619]. Advanced semiconductor device physics and performance down to 20 K has been reviewed, including fully depleted ultrathin film SOI devices, tri-gate, FinFETs, omega-gate nanowire FETs, and 3D-stacked SiGe nanowire FETs [620].

Research needs for high-energy physics applications presented in 2013 included cryogenic CMOS device models for technology nodes 130 nm and below [621]. Since that time, considerable advances have been made in cryogenic modeling, driven by both digital and sensing applications. Compact models supporting 4 K operation have been developed and validated nanometer scale technologies (160 nm, 40 nm, 28 nm) [618, 622]. It has been experimentally demonstrated for a 40 nm CMOS process that variability increases at cryogenic temperatures, and that the conventionally-used Pelgrom and Croom models for mismatch continue to apply at higher temperatures [617]. A study of 28 nm FDSOI MOSFETs at cryogenic temperatures down to 100 mK found that they outperformed 40 nm bulk MOSFETs in all aspects, including variability [623].

Development of unified models that offer accuracy across the deep cryogenic to room temperature range is an area of active research [609, 624, 625]. Reliability studies for cryogenic CMOS have focused on hot carrier degradation, which is generally accepted as the dominant failure mechanism at low temperatures [626]. Nevertheless, bias temperature instability (BTI) stress could play a role at cryogenic conditions, especially in modern CMOS devices, and should be addressed.

3.3.2. Applications ≥10 K

In the late 1980s DRAM at 77 K was evaluated for performance improvement giving the shortest access latencies at the time [627, 628]. More recently, DRAM at 77 K was proposed as a memory system for computers using superconducting electronics [629]. Several commercial DRAM chips have been found to work at temperatures as low as 77 K [630] and their retention behavior between 77 K and 360 K was studied [631]. Memory types that work at 77 K include SRAM, GC-eDRAM, STT-MRAM [632], and 3-D flash [633]. CryoGuard is a proposed DRAM for operation at 77 K with almost no refreshing [634].

Charge-trapping memory (CTM), recognized as one of the most promising non-volatile memories in the industry, has good retention and endurance performance, low power consumption, and compatibility with standard CMOS processes. Silicon–oxide–nitride–oxide–silicon (SONOS) is one of the most representative and widely studied CTMs. Recently, CTM has been developed and characterized in the 300 K to 10 K temperature range [635].

Evaluation of a cache architecture with SRAM and DRAM caches operating at 77 K shows 2 times faster cache access and 2 times larger capacity compared to conventional caches running at the room temperature [636]. A fully cryo-CMOS computer operating at 77 K is projected to achieve 3.4 times higher performance or 37% power reduction at the same performance [637]. Computing in cryogenic MRAM could also improve performance and power usage [638].

Power semiconductor devices can also work in cryogenic environments [639, 640].

3.3.3. Applications < 10 K

3.3.3.1. Sensors and Systems

Cryogenic multi-channel readout systems using gallium arsenide junction field-effect transistor (GaAs JFET) integrated circuits (ICs) were developed for a multipixel camera for astronomical observation [641].

3.3.3.2. Quantum Computing: Control and Readout

Quantum computing applications of cryogenic CMOS have been under development recently. Overviews of the needs for cryogenic CMOS in quantum computing are given in [642, 643]. Further work includes FPGA based approaches [644, 645,

646] and CMOS-based circuit designs of cryogenic low noise amplifiers and oscillators [647]. CMOS control chips have been demonstrated to operate at T ~ 4 K for superconducting transmon qubits [648] and for spin qubits [649, 650]. Specially-developed CMOS chips with digitally multiplexed input lines can operate at mK temperatures to reduce the number of control lines coming from higher temperatures [651, 652, 653].

3.3.3.3. Hybrid Semiconductor – Superconductor Circuits

Hybrid circuits combining semiconductor and superconductor elements operating at cryogenic temperatures have been developed [654, 655, 656]. Van Duzer et al. [657] demonstrated a hybrid RSFQ-CMOS memory operated at 4 K. The 64 Kibit CMOS memory chip was fabricated by TSMC using 65 nm technology. The power dissipation of 12 mW at 1 GHz operation at 4 K is acceptable for small to medium circuits. Konno, et al., [658] improved the design, reducing the power by 54%. Proposed is an even more energy-efficient hybrid memory using superconductor nanocryotron (nTron) drivers and CMOS memory arrays [659].

A superconductor field-effect transistor might be useful as an interface between CMOS and SFQ circuits [660].

Hybrid superconductor-semiconductor digital data links using cryogenic SiGe heterojunction bipolar transistors (HBTs) are being developed. In these links the gain and the corresponding power consumption are distributed over the 4 K to 300 K temperature range for overall optimization of the link figure of merit (energy per bit) [564, 565, 566, 567].

Optoelectronic devices combining superconductors with semiconductors are under development and might have applications in quantum information processing or interfaces between cryogenic electrical and optical communications [661]. Devices under development include thin film lithium niobate cavity electro-optical converters [662], VCSELs [663], and silicon photonic modulators [664, 665]. Packaging for cryogenic optoelectronics is reviewed in [666]. Proposed are hybrid semiconductor-superconductor neural networks for neuromorphic computing [360].

Superconductive multichip module (S-MCM) technology has been developed to support integration of superconductor and semiconductor circuits [547].

3.4. Active Research Questions for Cryo-Semi

One critical impediment to effective utilization of these cryogenic models is the lack of integration into foundry process design kits. This has historically been a captive effort within the organization performing circuit design activities, and hence has been a barrier to entry for newer design teams.

A review paper has recently been published by IMEP-LAHC comparing the physics and performance of various nanoscale devices at cryogenic temperatures [620]. In addition to research oriented towards the cryogenic utilization of semiconductor devices, observation of cryogenic operation also has general utility in understanding and measuring the physics of carrier transport [667].

4. QUANTUM INFORMATION PROCESSING (QIP)

4.1. INTRODUCTION

Quantum information is the information of the state of a quantum system. While quantum effects tend to become important at the scale of atoms, they also can affect the behavior of macroscopic systems such as superconducting circuits at extremely low temperatures, typically below 0.1 K. Quantum information processing (QIP) involves encoding, transforming, and decoding quantum information.

Areas of QIP covered in this section include quantum computing and simulation, quantum communication, and quantum sensing. Each is introduced briefly in the following subsections.

4.1.1. QUANTUM COMPUTING AND SIMULATION: INTRODUCTION

Quantum computing and simulation use quantum phenomena of superposition (existence in multiple states at once) and entanglement (correlation between qubits) to solve problems. For a deeper introduction to quantum computing than provided here, material is available spanning the range from basic and easy to follow [668, 669, 670, 671] to suitable for those undertaking serious study [672, 673].

Whereas conventional digital computing uses bits with values of either ‘0’ or ‘1’, quantum computing uses qubits that can have a quantum-mechanical *superposition* of ‘0’ and ‘1’ at the same time. The probability of being in either state can range from 0 to 1 (100%), but the probabilities always sum to 1 for a truly two-state system. *Entanglement* of multiple qubits allows the computational power to grow exponentially with the number of qubits, rather than linearly with the number of bits as in a conventional digital computer. A quantum computer performs a series of operations (a quantum algorithm) to modify qubit superpositions (probability of being in a particular state) and entanglements to increase some probabilities and to reduce others. Measurement of a qubit causes its state, and the states of entangled qubits, to collapse to either ‘0’ or ‘1’ with a probability dependent on the state of the qubit at the time of measurement. The goal is to maximize the probability of measuring the correct answer.

The way quantum computers use superposition, entanglement, and probabilities makes them very different from classical computers. For example, digital computers are deterministic and cannot generate truly random results. Randomness is inherent in quantum computing, so could have advantages in modeling systems in which randomness is important. Another fundamental difference is that an unknown quantum state cannot be copied perfectly, a consequence of what is called the no-cloning theorem. Transferring a quantum state from one qubit to another is possible, but only with destruction of the state in the initial qubit. The only way to create multiple copies of the same data is to perform the state preparation multiple times on separate qubits.

Frameworks or models for quantum computing [674] are varied and include the following approaches of practical importance.

- Analog or adiabatic quantum computation, typically based on quantum annealing, which performs processing by initialization of the system followed by slow, global control of the qubits towards a final state and readout.
- Gate-based quantum computation uses a sequence of few-qubit quantum gates performing logical operations, followed by measurement.
- Measurement-based or one-way quantum computation [675] first prepares a highly-entangled resource state and then performs single qubit measurements in a specific order to perform an algorithm. The computation is "one-way" because the measurements consume the resource state.
- Topological quantum computation performed by physical braiding of non-Abelian anyons, which are quasiparticles that occur only in two-dimensional systems and have less restricted properties than fermions and bosons.

Physical implementations for quantum computing [676] are also varied and include the following approaches of greatest relevance.

- Superconducting qubits are made from superconducting circuits with Josephson junctions as nonlinear elements.
- Trapped ion qubits use atomic transitions of ions trapped by electromagnetic fields.
- Neutral atom qubits trapped in an optical lattice formed by counter-propagating laser beams.
- Quantum dot qubits based on spin states of electrons trapped on nanometer-scale semiconductor islands.

- Double quantum dot qubits based on the location of electrons that can move between tiny semiconductor islands.
- Nitrogen-vacancy (N-V) center qubits in diamond.
- Photons.

Quantum computers will serve as accelerators within larger computer systems for the foreseeable future. Reasons include the large overhead to implement fault-tolerant quantum computation and the fact that quantum computation has not shown any advantages over classical digital computation for many applications.

Making a quantum computer is challenging because qubits face requirements pulling in opposite directions. On the one hand, qubits require isolation from the environment to avoid unintentional changes to their quantum states. Whereas digital circuits have only two states with a significant energy difference between the two, qubits have an infinite number of states with infinitesimal energy differences, thus the state is easily changed. On the other hand, interaction between components is required for qubit manipulation and readout. Some systems can adjust the coupling between components as needed, increasing the coupling only when needed and decreased to provide isolation at all other times.

Hardware components for a quantum computer generally consist of 4 layers [677]: 1) the "quantum data plane," where the qubits reside; 2) the "control and measurement plane," responsible for carrying out operations and measurements on the qubits as required; 3) the "control processor plane," which determines the sequence of operations and measurements that the algorithm requires, potentially using measurement outcomes to inform subsequent quantum operations; and 4) the "host processor," a classical computer that handles access to networks, large storage arrays, and user interfaces. This host processor has a high data rate connection to the control processor and runs a conventional operating system, which facilitates user interactions.

Components in the first two layers need to satisfy the 5 DiVincenzo criteria [678] for a physical implementation of quantum computing (scalable array of qubits, initialization, universal gate set, low error rate, qubit-specific readout). Later added were 2 criteria relating to the communication of quantum information (ability to convert between stationary and mobile qubits, and ability to transmit mobile qubits between specified locations). Moving quantum information using mobile or "flying" qubits is called *quantum teleportation*. Modern quantum computer architectures do not necessarily satisfy all 7 conditions. Even if all 7 conditions were satisfied, achieving either noisy intermediate-scale quantum (NISQ) or fault tolerant quantum computing would require further development.

Following are introductions to the main frameworks or models for quantum computing.

4.1.1.1. Analog Quantum Computing: Introduction

Analog quantum computers directly manipulate the interactions between qubits without breaking actions into individual gate operations. Hamiltonian-based quantum computation is another term for analog approaches including universal adiabatic quantum computing, quantum simulation, and quantum annealing.

In physics terminology, the Hamiltonian, or energy state, of a quantum system is used to encode or model a problem. In Hamiltonian-based approaches, the energy landscape starts flat and changes slowly and continuously to a final state with the energy peaks and valleys representing the problem to be solved. In adiabatic quantum computation (AQC), the system evolves adiabatically, i.e. without exchanging energy with its environment. Quantum annealing refers to systems that are not completely adiabatic.

Quantum annealing can model some problems using a set of qubits with programmable states and interactions. The system of qubits is initialized in a simple ground state, commonly by adjusting all qubits and all interactions to be the same and then applying a sufficiently strong effective magnetic field perpendicular to the problem basis, to randomize their quantum states into an equiprobable superposition of '0' and '1'. In ideal AQC, turning off the effective magnetic field sufficiently slowly while simultaneously adjusting the qubit weights and interactions toward the model values allows the system to remain in ground state as it evolves. Quantum tunneling through energy barriers helps the system to stay in the lowest energy state. The final state of the system at zero effective magnetic field represents the solution for the problem modeled. For implementation details in a superconducting system, see [679, 680].

The probability of finding the optimal solution using quantum annealing depends on factors such as qubit quality, rate of change of the applied magnetic field, and interactions with the environment. If the magnetic field changes too rapidly, the quantum system might not be able to track the lowest state as it moves. If the magnetic field changes too slowly relative to the characteristic qubit coherence time, too many qubits lose coherence and thus the ability to tunnel through energy barriers to stay in the lowest energy state. Always ending in the optimal (lowest energy) state is not critical because the computation can be repeated multiple times to find an optimal result.

The complexity or scale of problems solvable using quantum annealing depends on factors such as the number of qubits and their connectivity. Applications include optimization (§ 4.2.1), quantum simulation (§ 4.2.3), and quantum machine learning (§ 4.2.4).

Qubit quality factors such as coherence times are believed to be less important for quantum annealing than for gate-model quantum computing.

For the status of quantum annealing, see § 4.3.2.

4.1.1.2. GATE-BASED QUANTUM COMPUTING: INTRODUCTION

Another approach to quantum computing, the quantum gate model, uses a series of quantum logic gates to perform computations [681, 682]. The process begins with a state initialized to the computational basis, i.e. '0' or '1', applies a sequence of quantum logic gates, and measures the qubits on the computation basis to read out the result. Unlike many classical logic gates, quantum logic gates are reversible. A complete, or universal, set of quantum gates is needed to achieve the full capability of quantum computation [670]. Different physical implementation used to make quantum gates can have different gates that are natural or easiest to implement [683].

Qubit manipulations performed in the lowest hardware levels include initialization, universal gates, and readout. For fault-tolerant quantum computation, the error rates for qubit manipulations must be below threshold error rates that depend on the error correction approach used. Noisy intermediate-scale quantum (NISQ) computers make use of qubits without quantum error correction, and while not fully fault-tolerant, are expected to be realizable in the near term and to have some applications [684, 685].

Potential applications include classically challenging computational problems, such as factoring large numbers. Recent advancements include a theoretical proof that the number of steps needed to solve certain linear algebra problems using parallel quantum circuits is independent of the problem size, whereas the number of steps grows logarithmically with problem size for classical circuits [686]. Further applications include simulation of physical systems, database search, portfolio optimization, machine learning, artificial intelligence, and combinatorial optimization [687]. This so-called quantum advantage comes from the quantum correlations present in quantum circuits, but not in classical circuits. Known classical supercomputers cannot simulate quantum computers more than about 50 sufficiently coherent qubits.

For the status of gate-based quantum computing, see § 4.3.3.

4.1.1.3. TOPOLOGICAL QUANTUM COMPUTING: INTRODUCTION

Topological quantum computation with non-Abelian anyons in the ideal conditions of zero temperature and infinite anyon separation would heavily suppress errors at the hardware level, avoiding the need for resource intensive quantum error correction [688, 689, 690, 691]. Ideal conditions cannot be met in reality, resulting in some decoherence of the encoded information [692], although the requirements for error correction could be far less than for other qubits [693]. An accurate assessment of the scalability of topological quantum computing requires the development and characterization of actual topological qubits, which has not yet been achieved.

For the status of topological quantum computing, see § 4.3.5.

4.1.2. QUANTUM COMMUNICATION: INTRODUCTION

Quantum communication involves the generation and distribution of quantum states and resources. Primary applications include provably secure communication, long-term secure storage, cloud computing, and other cryptography-related tasks. In the future, a "quantum web" might allow remote devices and systems to securely share quantum resources such as entanglement, nonlocality, and randomness.

Quantum key distribution, which is a quantum communication protocol for two parties, involves a sender (Alice) and a receiver (Bob), who share one-time pad material (a shared classical random bit string). The simplest implementation requires only the superposition state of a photonic qubit with no entanglement required at all. This advanced technology has reached the stage where successful field trials have been performed and left running for several years. Future applications will be determined by the distance at which secure keys can be established. Current QKD implementations have a limitation on both the distance and rate at which shared keys can be established, for instance the best performance currently is ~ 1 Mbit/s over 50 km. As the communication distance increases further, the rate rapidly decreases, and a few hundred kilometers is considered the limit. To go farther and maintain the level of key security, the current QKD implementations require quantum repeaters to be added, which is also the key technology needed to distribute quantum entanglement over long distances.

For the status of quantum communication, see § 4.3.6.

4.1.3. QUANTUM SENSING: INTRODUCTION

Quantum sensing is the use of a quantum system, quantum properties, or quantum phenomena to perform a measurement of a physical quantity [17]. Quantum sensors enable measuring a physical quantity to a precision beyond the quantum standard limit (shot noise limit) possible with classical technology. Intermediate sensing applications to exploit quantum effects are also possible.

Quantum-enabled sensing that cannot achieve sensitivities beyond the standard quantum limit (SQL) nonetheless can provide advantages in comparison to conventional sensing by manipulating a sensor's quantum nature. Examples include functional NMR and non-classical light spectroscopy and sensing. It is the most relevant approach for commercial development at the current stage.

Quantum sensing beyond the SQL requires the manipulation of quantum information on the probe state. Hence it requires control of quantum-phase information and the ability to read it out. One of the most advanced technologies utilizes quantum correlated light. Matter-based sensors are under development using NV centers in diamond and hybrid quantum systems.

Quantum imaging is based on similar technology; however, this focuses on a different aspect of sensing. Using quantum-mechanically correlated light, imaging is possible with limited probing of the object under consideration. Important applications are in medical and biological applications where avoiding damage caused by the sensing is regarded as a vital factor.

Quantum global sensing uses quantum coherence to measure large-scale global properties with high accuracy. Application examples include natural-resource searching and crustal-movement imaging. The core technologies required for global sensing are quantum sensors combined with quantum repeater networks.

For the status of quantum sensing, see § 4.3.6.4.

4.2. APPLICATIONS AND MARKET DRIVERS FOR QIP

Quantum computing applications include secure computation, trusted data storage, and efficient applications [694, 695].

The publications of Shor's algorithm providing an exponential speed-up for factorizing a number [696] and Grover's algorithm providing polynomial speedup for unstructured search [697] gave theoretical grounding to the concept of using quantum mechanics to enhance computing performance. Many algorithms are currently available [698, 699]. Proposed are algorithms on machine learning, optimization based on the quantum approximate optimization algorithm (QAOA), and notably applications in theoretical chemistry and materials science [700].

Application areas and market drivers considered by the IRDS Systems and Architectures (SA) and Application Benchmarking (AB) teams [13] are shown in Table CEQIP-21 and described in following subsections.

Table CEQIP-21 Matrix of Application Areas and Market Drivers for Quantum Information Processing (QIP)

Application Areas	*Market Drivers*		
	Cloud	*Communications*	*Sensing*
Optimization	G		
Cryptographic codec	X	X	
Physical system simulation – Quantum simulation	X		
Artificial intelligence	X		X

* Technology areas specific to QIP. X: important application; G: critical gating application; P: power-sensitive application.

4.2.1. OPTIMIZATION

Optimization involves selection of a best choice among many and is important for solving a variety of practical problems in fields such as engineering design, logistics, manufacturing, and finance [701]. The difficulty of solving optimization problems increases with the number of elements, possible interactions, and constraints. Quantum computers are expected to provide the greatest benefit with complex optimization problems.

Quantum-annealing processors are designed to solve NP-hard logistics and scheduling problems with applications in industry, military, government, and science. Optimization is a core subproblem in machine learning applications and requires many samples of optimal and near-optimal solutions. Quantum-annealing processors based on superconducting flux qubits are commercially available from D-Wave Systems [702]. For details, see § **4.3.2**. Systems have been commercially available since 2011 at a cost of about 10 million USD each [703]. These systems can also be accessed online in a cloud computing model. Quantum computing approaches that require cryogenic temperatures are likely to need RF signal processing and control as well as digital computation within the cryogenic space.

Note that no general physical computing method (including analog and quantum approaches) has yet been clearly demonstrated to be capable of solving NP-hard problems without requiring exponential physical resources (energy or time) to be invested in the physical process performing the computation. The prevailing view among computational complexity theorists [704] is that solving NP-hard problems in polynomial time would require uncovering new physics (i.e., beyond standard quantum mechanics).

Quantum algorithms are known for gate model quantum systems and could be applied to problems in optimization and machine learning on sufficiently large systems.

4.2.2. CRYPTANALYSIS

It is conjectured that quantum computers (gate model and/or annealing-based processors) of sufficient size could be used to break current cryptographic protocols (notably RSA encryption). Quantum devices for secure key exchange have been developed that would be necessary to support certain post-RSA cryptographic methods.

Quantum communications has applications in secure communications and also has applications for movement of quantum information [705].

4.2.3. QUANTUM SIMULATION

Simulators model systems to give information about their behavior. Quantum simulators use quantum effects and are expected to scale better than classical simulators and thus to allow simulation of systems beyond the capabilities of classical simulators [706, 707]. Research and Markets projects that the global simulation software market will grow from USD 6.26 billion in 2017 to USD 13.45 billion by 2022 [708]. Quantum simulation is currently a tiny fraction of the overall simulation market.

Quantum simulators can be classified as analog and digital simulators [709]. In analog simulators, a controlled physical system described by the model to be investigated is built and investigated. In the context of cryoelectronics, this has a long tradition from the Josephson junction arrays studied since the 1990s to modern cavity areas. In digital simulators, the model to be simulated is encoded into a quantum computer algorithm that allows to extract the desired property. The required compilation is often very economical, making these the first expected applications of quantum computers.

Digital quantum simulation can have a major impact on the investigations of molecules and materials, allowing their electronic structure to be simulated even in the case of strong correlations. Techniques to take this to disruptive levels on gate-based quantum computers are known [710, 711, 712] and small instances have been demonstrated [707, 713, 714]. A long-term goal of this activity is the simulation of nitrogenase [715].

Quantum annealing can be applied to problems in quantum simulation by querying the qubit superposition states mid-anneal. Quantum annealing processors have been applied to problems in quantum simulation and materials simulation, e.g., for spin systems [716, 717, 718]. In 2019 a photonic quantum information processor was used to experimentally simulate a stochastic process with 16 possible outcomes [719]. Quantum simulators with 1D interactions have been demonstrated with up to 51 neutral atoms in Rydberg states [720] and up to 53 ions in linear traps [721]. Desired for simulations are multi-dimensional quantum interactions [722].

4.2.4. QUANTUM MACHINE LEARNING

Machine learning assisted or enhanced by quantum computing is a relatively new application area under evaluation and development [723, 724, 725, 726]. Quantum annealing can be useful in discrete optimization and sampling, in particular Boltzmann sampling, which is a core technique in machine learning. Known applications contain image recognition and pattern inference for vehicles and healthcare, neural networks, and recommendation systems. Advances in algorithms for quantum machine learning have also resulted in improvements to classical algorithms, which has reduced the potential benefits [727]. The Journal Quantum Machine Intelligence began publication in 2019 [728].

4.3. PRESENT STATUS FOR QIP

For a list of companies worldwide engaged in the development of quantum computing or quantum communication, see [729, 730]. While there are few commercial products or services based on quantum information processing, research and development activity continues to ramp up. A striking development during recent years has been an informal competition to produce circuits for quantum computing with the highest qubit count. The competition shows tantalizing improvement, although the results are announced by press releases without independent verification and benchmark results are not comparable from one qubit type to another.

Quantum communications requires different technological elements such as quantum memory and quantum optical interface. These fundamental elements for quantum communications are still under development. The most matured quantum communication application is quantum key distribution (QKD), which is still limited to relatively short distances. Implementing QKD on a network over practical distances still requires a quantum repeater, which has not been demonstrated to date.

4.3.1. REGIONAL EFFORTS IN QIP

Announcements of additional funding for quantum computing or QIP have been made by Australia, Canada, China, the EU, Germany, India [731], the Netherlands, Singapore, the UK, and the USA.

4.3.1.1. AUSTRALIA

A CSIRO roadmap report released in 2020 outlines Australian and global opportunities in QIP [695].

4.3.1.2. CHINA

China is building a new multi-location quantum information laboratory and investing over 100 billion RMB in QIP [732]. Commercial projects of large scale are also underway [733].

4.3.1.3. EUROPE

European quantum technologies roadmap reports have been published since 2005 [700, 734]. The European Commission started a quantum technologies flagship program and will begin selection of research and innovation projects in 2018 [735, 736, 737]. Initial quantum computing grants funded two of the leading approaches: superconducting circuits and trapped ions. Project MATQu, short for *Materials for Quantum Computing*, started in June 2021 with the goal to support the creation of a pan-European research infrastructure for advanced computing technologies.

In addition to EC-wide efforts, there are notable national programs. These include German studies of the status of quantum computing [738] and commitment of 650 M€ for quantum technologies [739]. The UK Quantum Technology Hubs are going into their second round, and the Netherlands published a National Agenda for Quantum Technology in 2019 [740].

4.3.1.4. JAPAN

Quantum computation in Japan is focused almost entirely on superconducting implementations. Examples of this emphasis include a flagship project within Q-LEAP (2018–2027) funded by MEXT as well as the ERATO project (JST 2016–2021, 1.5 billion yen) for macroscopic quantum machines. The architecture is based on the topological surface code. The goal of this effort is to implement a quantum computer using 100 qubits by 2028. Architectural development is quite advanced in Japan with architectures also being developed for distributed, optical-based and ion-trap based quantum computing systems. Hardware development has started for those approaches where the current focus is on realization of the necessary hardware building blocks.

Japan has also been putting significant effort into quantum annealing systems with AIST being the core research institute involved. The hardware is based on superconducting qubits hardware using double-bonding technique. The current coherence time is on the nanosecond scale, which is three orders of magnitude smaller than the computational time. The software development in this area has focused on mappings between the problem to be solved and the chip design.

The unique situation in Japan for computation is the development of non-quantum unconventional computers. These are often referred as quantum stimulated computers. These are in effect dedicated single purpose machines using conventional technology, and hence there is no quantum coherence involved during the computation. These developments are mainly done in industry sector with government funding. (Example projects: ImPact 2014–2018, 3 billion yen; NEDO 2016–)

Japan has two further strengths in quantum communications research. One is quantum key distribution (QKD) and the second is quantum repeaters. Japan has a long history in QKD development, centered at NICT. After 20 years of fundamental research development, the project has involved industries to run field experiments for a trusted node based QKD network and has now reached an implementation stage where it will be used for commercial purposes. A national project funded by MIC for satellite

based QKD has recently started in 2018 which aims to integrate the satellite and trusted node approaches together to explore the feasibility of physical layer security. (Projects: MIC 2018–, satellite, 5 years; SIP 2018–, commercial development, 2.5 billion yen)

Quantum repeater research has been led by theory development and combined with optical and CQED technologies. The architectural designs are advanced in nature, though their implementation is still in the fundamental research phase. The key technology to be developed is the light matter interface. As the architectural design is well established, a breakthrough would provide a scalable growth for quantum communication networks.

The current implementations within the quantum sensing arena are mostly a quantum enhanced technology. The sensitivity is still within that achievable with conventional approaches, however these new technologies show several real advantages. These technologies are based on variety of quantum systems including nitrogen vacancy (NV) centers in diamond, nuclear spin ensembles, low-dimensional quantum systems and nano- or opto-mechanical systems to highlight a few main examples. Hybridization of these systems is also quite popular to control those systems as well as to generate new applications and physical phenomena. (Projects: MEXT 2015–2019, 1 billion yen; JST-CREST 2016–2023, 4.5 billion yen; a Flagship Q-LEAP 2018–2027)

Quantum sensing beyond the standard quantum limit and current sensitivities is still a challenge to realize. The main obstacle is the noise effect on the probe. Error control mechanisms and applications are currently investigated. Further, the principle of a number of these schemes has been demonstrated; however, it will take more time to realize true sensing prototypes.

4.3.1.5. USA

US gate-type quantum computers lead the world in qubit count, with benchmarked results of Google at 53 qubits for their quantum supremacy experiment described below, IBM at 53, and an announcement of Intel at 49. For ion trap qubits, IonQ has announced 160 qubits, of which 79 are functional and the others are for storage. These are all US companies, although Intel had a non-US partner. While these systems were top-in-class worldwide when announced, qubit count is widely regarded as only being one component of a more complete metric.

The latest new US activity is the National Quantum Initiative Act (NQI), passed by the US government in December 2018 (1.2 billion USD over 5 years). While the new NQI funding is substantial, overall US government investments are even larger. US industrial investments are difficult to assess exactly, but a speaker in the NQI Senate hearing estimated them to be in the billions but probably less than 10 billion USD [741].

The NQI includes the expected funding for science and engineering research, but additionally includes government support for an industry-government consortium intended to increase the efficiency of the human enterprise that will develop quantum computing. The consortium is called the Quantum Economic Development Consortium (QED-C) and currently includes over 60 voting member companies and a board including large companies, small companies, and key government agencies [742]. QED-C is like the semiconductor consortium SEMATECH when it was started in the 1980s. QED-C will identify common needs and communicate them to the US government with the intent of better aligning government R&D with industrial needs. These needs include research funding for the most crucial science and technology, yet also include indirect albeit crucial areas such as workforce development, the supply chain, and standards.

The US Department of Energy (DoE) is establishing several centers for quantum computing. Of those, both Berkeley Quantum and the Chicago Quantum Exchange include programs of cryoelectronic qubits. The DOE Office of Science has established a Quantum Computing User Program at Oak Ridge National Laboratory. This program provides access to commercially available quantum computing resources through the Oak Ridge Leadership Computing Facility. In 2020, the DOE Office of Science announced a Funding Opportunity Announcement for National Centers for Quantum Information Science as part of the NQI. Up to five centers are expected to be established under this funding opportunity. In 2020, the DOE Office of Science announced a Quantum Internet Blueprint as part of a planned effort to connect all 17 DOE national laboratories by a quantum network.

While quantum computing is still very much in the research stage, US companies are beginning to offer access via the Internet as well as offering machines for purchase [729]. Access typically includes software that abstracts the underlying qubit operations into a form more easily learned by programmers—or in some cases into an application-specific framework that offers a “turnkey” solution within a limited problem domain.

4.3.2. ANALOG QUANTUM COMPUTING: STATUS

Quantum-annealing processors based on superconducting flux qubits have been developed by and are commercially available from D-Wave Systems [7, 702, 743, 744, 745]. The D-Wave 2000Q released in 2017 includes a superconducting chip with 128,472 Josephson junctions, of which 75% are in classical SFQ digital control circuitry to program the processor and read out

the results and the remainder are either directly in qubits or in the analog coupling elements that allow qubits to interact in a programmable way. The D-Wave Pegasus P16 chip in the Advantage QA system released in 2020 includes a superconducting chip with 1,030,000 Josephson junctions, 40,484 couplers, and a maximum of 5,640 qubits [746, 747]. Differences between the 2000Q and Advantage systems include an upgrade from Chimera to Pegasus hardware graph topology [748].

Quantum annealing algorithms are reviewed in [749] and evidence for advantages are presented in [750]. A method to factorize integers using quantum annealing was developed and demonstrated using the D-Wave 2000Q [751]. An error suppression and correction scheme known as quantum annealing correction (QAC) has been used with D-Wave systems [752]. Portfolio optimization has been used as a case study to benchmark quantum annealing controls and their relative effects on computational accuracy [753]. Benchmarking results remain generally controversial.

Theoretically, any algorithm for gate-based quantum computing can be performed by error-free AQC [754, 755]; however, as with all quantum computing models, achieving perfect error-free operation in practical systems is not possible [756]. Many theoretical questions about efficient computation in the AQC model are open; for a survey of current status see [750]. Quantum annealing systems with up to 2000 qubits have been implemented and deployed, and hundreds of different problems have been demonstrated to work on these systems. In terms of performance, existing quantum annealing systems has been shown to break even with, and sometimes outperform, classical alternatives in some use scenarios [757, 758, 759, 760].

4.3.3. GATE-BASED QUANTUM COMPUTING: STATUS

Many types of qubits have been proposed or demonstrated for use in quantum computing, including trapped ions, cold atoms in optical lattices, liquid and solid-state spin resonance, photons, quantum dots, nanowires, superconducting circuits, and NV centers. Reviews include [706, 738, 761, 762, 763]. Following subsections cover status of qubits and associated hardware most relevant to gate-based quantum computing.

Quantum architectures based on quantum gates and circuits are in active research. Architectures and considerations specific to qubit type are covered in the following subsections. All platforms suffer to different degrees from errors including decoherence. Scaling to large systems will require the application of error correction techniques such as surface codes [764]. The classical electronic controllers used to manipulate and read out qubits also must be designed to minimize the introduction of errors [765] and will likely need a quantum-specific instruction set architecture (ISA) [766, 767]. Qubit control using cryogenic semiconductors or superconductor electronics is also covered in sections **3.3.3.2** and **2.2.4**. Quantum computers will be used as accelerators or co-processors within larger computing systems, and the architecture for such systems is under development [768].

Table CEQIP-22 gives details of quantum computing component status. Table CEQIP-23 summarizes the status of major quantum computing development approaches with the best values for a variety of approaches. Quantum volume [769] is a metric for the number of quantum circuits that can be implemented. Computing capability grows exponentially with qubit count, although the rate of growth depends on the implementation. Qubit connectivity is the average number of qubits that can be made to interact with a given qubit, with higher connectivity being advantageous [770]. The 2-qubit gate depth is an indication of the number of logic gates that can be performed before loss of coherence significantly increases the error. Quantum teleportation is useful for moving quantum information around larger systems. Qubit function and system scalability are subjective ratings. Note that while some aspects of quantum dot and topological approaches seem favorable to scaling, difficulties making reproducible qubits and 2-qubit remain challenging. Needed are better metrics for comparison of quantum computing systems.

Industry has started to integrate quantum devices and to scale up towards computing systems. For a list of companies worldwide engaged in the development of quantum computing or quantum communication, see [729, 730]. Several cloud-based quantum computing platforms are now available to users [771, 772].

Notably, Google reported a demonstration of quantum supremacy, i.e., the claim to outperform the largest currently known supercomputers in one task [773]. The devices consist of a 9 by 6 array of nearest-neighbor coupled superconducting qubits, of which one was not used. The task was the execution of a random algorithm whose output, in the quantum case, is described by the Porter-Thomas distribution and it was certified that the device worked well enough to approach this result. A key factor in this achievement is two-qubit gate error ratios less than 1% across the chip. There is debate about the computational claim [774, 775], which does not detract from the hardware achievement.

The overall picture is that no approach has emerged as most likely to scale to the millions of qubits needed. One possibility is that a hybrid approach using different qubit types could best satisfy the range of requirements for a large-scale gate model quantum computer.

Table CEQIP-22 Quantum Computing Component Status

Table CEQIP-23 Gate-Based Quantum Computing Status Summary

Qubit type	*Quantum volume, (circuit size)*	*Qubit count*	*Qubit connectivity*	*2-qubit gate depth*	*Quantum teleportation*	*Qubit function*	*System scalability*
Superconducting	512 (9×9)	127	3.25	667	0.42 m	fair	fair
Trapped ion	4096 (10×10)	12	10	> 100 000	yes	fair	fair
Quantum dot	–	4	1	104	–	poor–fair	fair–good
Photonic	–	4			1400 km	poor	fair

2-qubit gate depth: ratio of coherence time divided by 2-qubit gate time (T_2^*/t_{2q})

4.3.3.1. SUPERCONDUCTING QUBITS AND DEVICES

Superconducting qubits are artificial atoms of macroscopic size made from thin-film inductors, capacitors and Josephson junctions. There are many ways to implement, control, couple, and read out superconducting qubits [761, 776, 777, 778]. Common materials used to build superconducting qubits are aluminum, and aluminum oxide, and niobium [763, 779, 780]. Josephson junctions are critical components in superconducting qubits, and their uniformity can be improved by fabrication control or by individual laser annealing after fabrication [781]. Controlling devices with voltages rather than currents has advantages in some cases and has motivated development of a voltage-tunable transmon qubit with graphene-based Josephson junctions, although the coherence time needs improvement [782]. Other voltage-controlled devices include the gatemon qubit [783] and a superconducting quantum bus [784]. For status reviews of superconducting qubits, see [785].

One- and two-qubits gates can be implemented in various ways. A common method applies microwave pulses tuned to specific frequencies for driving the needed actions [776, 786]. A general issue in the required control and readout processes are the decoherence effects on the qubit. Qubit decoherence is caused by interactions between the qubit and its surrounding environment [787, 788, 789]. To mitigate errors caused by various decoherence sources, including fluctuations of magnetic and electric fields, various low-level strategies such as optimum working points are applied, with the goal of reaching the error correction threshold.

Error corrected superconducting qubit devices will allow systems with higher complexity, which is required for future quantum information processing architectures [681, 790, 791, 792, 793, 794, 795, 796, 797, 798].

System achievements include demonstration of quantum volume 64 [799], and significant reductions in processing time [800].

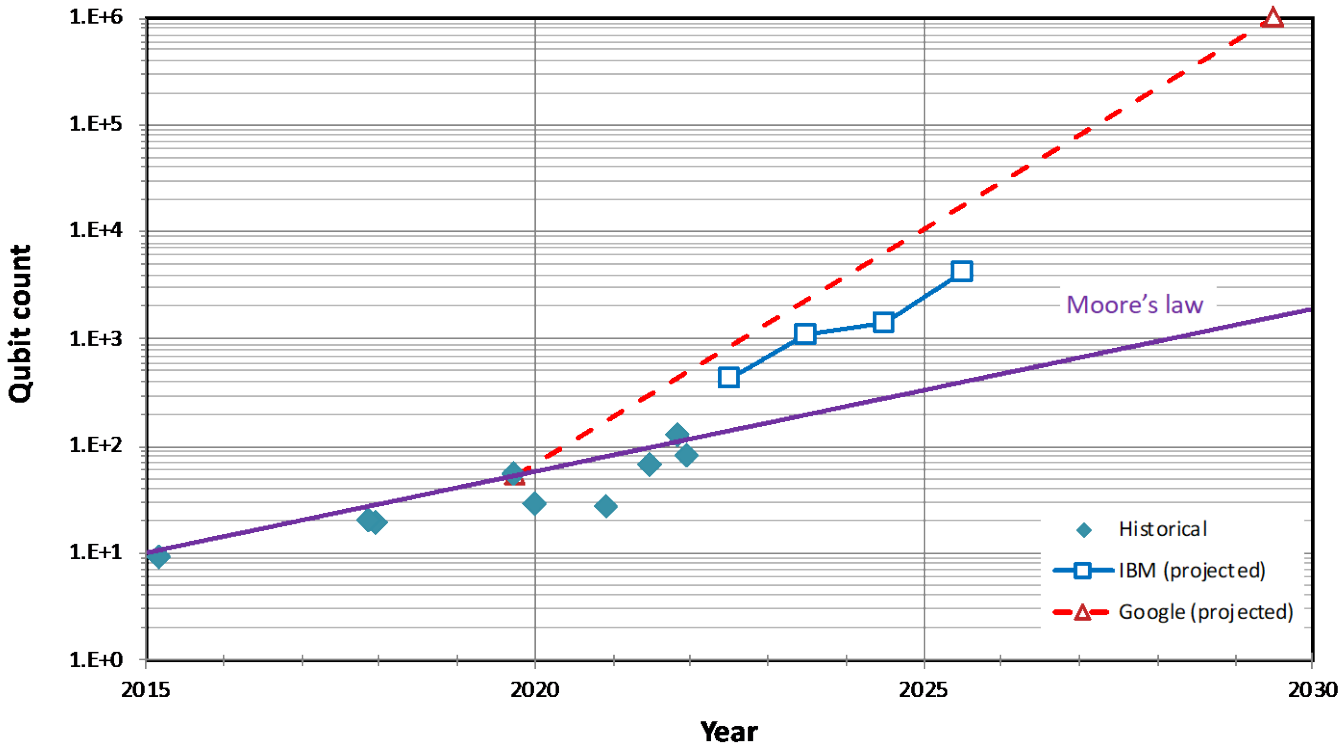


Figure CEQIP-8 Superconducting Qubit Trends

Note: Moore's law has not been proven to apply to qubits and the trend line is provided for reference only.

Table CEQIP-24 Quantum Computing Roadmaps: Superconducting

Superconducting Devices: Superconducting quantum computing systems are built from modules containing qubits and other superconducting components or devices. In the circuit quantum electrodynamics (cQED) architecture pioneered in 2004 [801], the qubits, which are inherently nonlinear devices, are coupled to linear resonant structures, which can be used for coupling between qubits, as well as the measurement of qubits for transferring readout results to the outside classical world [802]. Commonly these linear resonators are formed from thin-film coplanar waveguide (CPW) resonators, which are straightforward to fabricate with quite low microwave losses [803], although to obtain the proper resonance frequencies for integrating with qubits, these CPW resonators must be rather long, typically several mm, posing a challenge for reducing device areas. Inserting a Josephson junction in such a CPW resonator allows one to tune or modulate its resonance frequency [804]. Alternatively, lumped-element linear resonators offer the ability to form significantly more compact structures for coupling and measuring qubits. However, fabricating lumped-element resonators with sufficiently low microwave loss can be challenging [805]. Fully superconducting indium-bump interconnects have been demonstrated that allow for the three-dimensional integration of quantum circuits without introducing lossy amorphous dielectrics [806]. Superconducting through-substrate vias (TSVs) enable higher levels of chip stacking and have been demonstrated using TiN [324, 325] and Al [326].

Measuring the state of a quantum system in general requires more care than detecting a classical bit due to subtleties of the fundamental quantum measurement process. For superconducting qubits in a cQED environment, measurement is typically done with extremely weak microwave signals that must then be amplified by another class of superconducting devices that work very close to the quantum limit [807]. This includes Josephson parametric converters [808], Josephson parametric amplifiers [809, 810] and traveling wave amplifiers [811]. This amplifier-based measurement approach requires strong microwave pump tones for driving the parametric nonlinearity of the amplifier. In order to prevent these pump tones or other noise processes in the amplifier from perturbing the qubit, it is necessary to include significant amounts of non-reciprocal elements, such as microwave isolators or circulators, between the amplifiers and qubits and resonator circuits. Conventional cryogenic microwave isolators and circulators are bulky, magnetic, and difficult to thermalize at millikelvin temperatures,

posing a challenge for scaling to large systems. Alternative approaches to forming non-reciprocal elements are currently being developed using superconducting circuitry and parametric active devices [812].

An alternative to amplifier-based qubit measurement involves the use of a microwave photon detector, the Josephson photomultiplier (JPM) [813], which can provide a digital result from qubit measurement at the millikelvin stage of the cryostat [814] for interfacing with a cryogenic digital coprocessor in the low-temperature environment [815]. In addition, because no parametric pump tone is needed, JPMs can be coupled to superconducting qubits and resonators without the need for intervening isolators or circulators [814].

The conventional approach to the control of superconducting qubits and the implementation of quantum gates involves the use of resonant microwave pulses with carefully controlled amplitude and phase. Microwave-based gates have been refined to the point where gate errors are less than 0.1% [816], exceeding the fault-tolerant threshold for implementing quantum error correction. However, the generation of microwave signals for qubit gates requires a significant hardware overhead of room-temperature equipment outside of the cryostat, including microwave sources, arbitrary waveform generators, mixers, and amplifiers. An alternative approach currently being explored involves the use of SFQ-based superconducting digital electronics to drive quantum gates using resonant trains of SFQ pulses [817, 818, 819], thus greatly reducing the requirements for room-temperature hardware and moving much of the control elements into the low-temperature environment [815].

Communication of entangled qubit states through a one-meter-long superconducting cable has been demonstrated [820]. Use of photonic quantum interconnects for longer distance communication requires efficient transducers. Recent developments include [821, 822, 823, 824].

4.3.3.2. Trapped Ion Qubits

Trapped ion qubits encode quantum information in the electronic energy levels of ions such as Ca^+ or Yb^+. The ions are suspended in ultra-high vacuum using electromagnetic fields and two-qubit gate operations can be performed between nearby ions. Lasers and photon detectors are typically used for qubit control and readout. Operation at cryogenic temperatures helps to achieve the necessary vacuum conditions and reduces electronic noise. Operation at 50 to 100 K provides significant benefits; however, operation in the 1 to 10 K range might prove necessary, especially for early systems. For reviews, see [722, 761, 825].

An 11-qubit quantum computer has been demonstrated with all-to-all qubit connectivity [826]. Coherence times of trapped ion qubits is typically long (> 1 s), but gate times have also tended to be long (~ 50 μs). Fast (~ 1 μs) and high-fidelity two-qubit logic gates have been demonstrated by using amplitude-shaped laser pulses [827]. Quantum teleportation has been demonstrated using the ability to move individual ions [828].

Linear ion traps have worked well and allow all-to-all entanglement of 10 to 20 qubits. Current efforts are focused on scaling up to the range of 50 to 100 qubits [829]. Scaling to significantly larger numbers of qubits requires physical movement of ions between linear traps or some other method for transporting quantum information between modules [825, 830]. Challenges include the scalability of systems with multiple linear traps.

4.3.3.3. Quantum Dot Qubits

Quantum dots confine one or more electrons or holes within a region of host material both small enough that quantum effects are significant and large enough to allow control. Semiconductors are commonly used as the host material. Electrodes can be used to control the electron number or spin state in the quantum dot [831]. Other names for quantum dot qubits include spin, silicon, or semiconductor qubits.

Several types of quantum dot qubits are under investigation [832, 851, 852, 833]. Spin-based quantum dot qubits have demonstrated long coherence times due to their relative insensitivity to charge fluctuations; however, their gate times have been slower than desired because an oscillating current applied to the electrodes is used to produce an oscillating magnetic field to interact with the electron's spin. Charge-based quantum dot qubits allow much more rapid manipulation using electric fields; however, they suffer from rapid decoherence due to sensitivity to charge noise. A balance of desired characteristics might be achievable with hybrid qubits [853].

Nuclear spin can also be used in quantum dots qubits, although these are considered to be hybrids with the nuclear magnetic resonance (NMR) approach to quantum computing. Nuclear spin qubits have potential advantages but are still in early stages of development [834, 835].

Semiconductor materials: GaAs was used initially as it can make high quality quantum wells for trapping electrons; however, both Ga and As have a net nuclear spin that interacts with and causes the electron spin to rapidly lose quantum phase coherence. Currently favored semiconductor materials include Si, Ge, SiGe, and isotopically purified ^{28}Si [836, 837, 838]. Challenges for quantum dot qubits in silicon include control over location of quantum dots, control of 2-qubit coupling strength, and lack of

significant spin-orbit coupling for electrons, which can result in relatively long interaction times. Carbon nanotubes are also under development for use in quantum dot qubits [833].

One- and two-quantum-bit gates for quantum computation can be implemented using the spin states of coupled single-electron quantum dots [839, 840] and have recently been demonstrated with error ratios approaching the threshold for error correction and system scaling [841, 842]. The fastest demonstrated 2-qubit gates with Si qubits are 800 ps with error ratio < 1e-3 [843]. Coupling of quantum dot qubits over distances much longer than the size of a single quantum dot has been demonstrated using a superconducting microwave resonator [844, 845, 846]. A device with 4 interacting quantum dot qubits has been demonstrated [847].

Architectures for quantum computers based on quantum dots are an active area of research [848, 849, 850, 851, 852, 853]. Quantum dots both require and benefit from advanced semiconductor manufacturing processes [549, 849, 854]. Operating temperatures for quantum dot qubits could be as high as the 1 K range [855] and could allow integration with control electronics on the same chip [856]. Systems capable of controlling many quantum dot qubits have been demonstrated [649, 652, 653] or proposed [857, 858] and seem scalable to thousands of qubits. Together, these characteristics might enable the construction of more complex processing architectures.

4.3.3.4. PHOTONIC QUBITS

Photons have some advantages as qubits, including stability at room temperature and long quantum coherence time. A significant problem has been the lack of a natural two-qubit gate due to the fact that photons do not interact with each other. Conventional circuit-based approaches (quantum gate network based) are challenging as, to date, no natural two-qubit gate is available due to the fact that photons do not strongly interact with each other. Groups are working to develop non-linear elements necessary for two-qubit photonic gates, but progress had been slow [738, 859]. Nevertheless measurement-based or one-way quantum computing models have recently appeared as a viable alternative, as they do not require specific gate operations, while shifting the computational complexity to hyper entanglement generation [675, 860]. In all cases, integration technologies are required for scalability. Multi-photon entanglement in silicon devices and chip-to-chip quantum teleportation was reported in 2020 [861] and might provide a scalable platform for quantum computing or for more general quantum information processing [862]. A quantum sampling algorithm demonstrated in 2021 [863] on a programmable photonic chip using highly squeezed states is promising, yet the quality of the qubits needs to be improved considerably and photon losses reduced if the technology is ever to scale to practical problems [864]. Also, continuous-variable optical systems might provide the necessary combination of universality, scalability, and fault tolerance for quantum computation [865]. Monolithic integration of photonic circuits is nevertheless challenging due to competing requirements, which might favor heterogeneous integration [866].

4.3.4. OTHER GATE-BASED QUANTUM COMPUTING: STATUS

Nitrogen-vacancy (N-V) or color centers in diamond are solid-state ‘artificial atom’ qubits that could enable on-demand remote entanglement, coherent control of over ten ancillae qubits with long coherence times, and memory-enhanced quantum communication. Challenges have included qubit inhomogeneities, low device yield and complex device requirements. A heterogeneous process integrating diamond waveguide arrays on a photonic integrated circuit (PIC) has been demonstrated with a 128-channel array of N-V centers [867].

4.3.5. TOPOLOGICAL QUANTUM COMPUTING: STATUS

Majorana bound states (MBS), also called Majorana zero modes (MZM), are expected to be the simplest and most controllable types of anyons, although they do not provide the full power of topologically protected quantum computation. Approaches to creating Majorana bound states include fabrication of superconductors on top of 2D or 1D semiconductors that exhibit the quantum Hall effect [868]. Efforts to develop topological qubits using Majorana bound states in topological superconductors have not yet succeeded but show some promise [869, 870]. Getting the required physical properties together in one device has been challenging. Microsoft issued a press release in early 2022 announcing demonstration of a quantum phase with Majorana zero modes and a measurable topological gap, a major step towards a topological qubit [871]. Scientific confirmation awaits. A hybrid qubit integrating a topological insulator into a conventional superconducting qubit was demonstrated in 2022 and might serve as an experimental platform for further development [872]. Alternative designs for topologically protected qubits are also being pursued [690, 873, 874].

Scalable architectures based on topological qubits are in the early research stage [691, 693].

4.3.6. QUANTUM COMMUNICATION AND SENSING: STATUS

Quantum communication technologically ranges from point-to-point quantum key distribution to fully quantum networks [875, 876]. The most important applications of cryoelectronics in this field are single photon detectors based on superconducting nanowires [877]. A cryogenic microwave-based quantum communication scheme has been proposed and is being researched in the EU [878].

Technologies for quantum communication relevant to current quantum information technology developments include quantum key distribution, quantum interconnects, and quantum repeaters; each covered in following sub-sections along with quantum sensing.

4.3.6.1. QUANTUM KEY DISTRIBUTION

Quantum key distribution has moved from the research arena now to the product development phase where market alignment is highly essential. Further technology developments to higher generation rates over long distance are important and necessary. For long distance QKD systems, there are two directions currently being investigated: trusted relay optical-fiber-based networks and satellite communications which could be combined in the future. These technologies are in principle only based on the superposition of quantum states and do not rely on quantum entanglement. The challenge is to go beyond 10 Mbit/s for 50 km, and 1 kbit/s for satellite communications. To eliminate trusted nodes, which inherently severely compromise key security, the move to quantum repeater technology is needed.

Quantum key distribution utilizing quantum repeaters naturally allows extending the communication distance significantly without compromising key security. The challenge is to develop the key technology necessary in quantum repeaters. Limiting the use of quantum repeaters to only QKD allows elimination of several components including technologically difficult quantum memories with long storage times. Another possible quantum communication approach including QKD is a quantum sneakernet, a system based on physical movement of quantum memory [879]. This is a quantum-memory-based quantum communication system whereas quantum repeaters are communication-channel-based system. Quantum sneakernets require an extremely long-lived quantum memory with coherence time sufficient for a quantum signal to be physically delivered from the sender to the receiver. This necessitates either a fault-tolerant quantum error corrected qubit (composed of many physical qubits) or an exceptionally long coherence for the quantum memory (possibly weeks).

4.3.6.2. QUANTUM REPEATERS

Quantum repeaters are a core technology for quantum communication. Any direct quantum communication between two parties has a distance limitation as the success rate decreases exponentially with the communication distance. To overcome this fundamental limitation, waystations are required in the communication channel, similar to amplifiers in classical communication channels. However, unlike amplifiers used for classical signals, it is impossible to amplify a quantum signal due to the no-cloning theorem. Hence quantum repeaters work by generating and then swapping entanglement between waystations to extend the range of quantum correlations. Quantum repeaters allows the generation of entanglement over the entire communication network. The deterioration of the fidelity of entanglement can be recovered by distillation (purification) of the quantum state.

Quantum relays are a precursor technology to full quantum repeaters. They are in a sense quantum pre-repeaters or primitive quantum repeaters with limited functionality. It does not show the scalability that a true quantum repeater-based network would exhibit (polynomial resource usage with the quality of the entangled resource not scaling exponentially with overall communication distance) but it can scale polynomialy if the quantum memory has an infinite coherence time. Typical technological requirements for the relays are single photon sources, single photon detectors, quantum memories, and an interface between the matter-based qubit and photon. The requirements include optical cavity developments, control of matter qubits with optical transitions as such as NV centers in diamond, and lossless fiber-cavity coupling. Quantum relays and quantum repeaters share many of the basic hardware technology components, though the architectures of the communication systems are vastly different.

Quantum repeaters need to have at most a polynomial scaling in terms of resources required while at the same time establishing entangled states whose quality does not scale down exponentially with the number of repeater nodes in the network. A quantum repeater system consists of three distinct operations: entanglement distribution, entanglement swapping, and entanglement distillation (purification) and error correction. Although quantum repeaters employ error correction, the implementation is much simpler than in quantum computation and fault tolerance is not necessary.

4.3.6.3. QUANTUM INTERCONNECTS

Quantum interconnects are components of quantum communications systems used to transport entanglement between quantum devices. In particular, they can be used to fundamentally change the connectivity for quantum adiabatic computation, quantum

annealing, and quantum simulation, providing significant benefits in this era of noisy intermediate-scale quantum (NISQ) computing [684]. In the longer term, quantum interconnects allow distributed quantum computation. For a review and roadmap of quantum interconnects, see [880].

Quantum interconnects can be implemented on chip and between chips for short distances that do not require quantum repeaters. For example, entangled superconducting qubit states have been communicated through a one-meter-long superconducting cable [820]. Long distance quantum interconnects are expected to use photons. Use of photonic quantum interconnects by non-photonic qubits requires efficient transducers.

The quantum internet is a network of quantum computers connected by quantum communication channels. On the quantum internet, quantum computers are connected coherently and one can distribute quantum correlations and consume them in a global fashion. Such a network of coherently connected quantum computers would allow global distribution and consumption of quantum correlations.

4.3.6.4. Quantum Sensing

Quantum sensing is an area of active research [17, 881, 882].

4.4. Benchmarking and Metrics for QIP

Quantum information processing is rapidly progressing through an exploratory stage of engineering research, and there is widespread consensus that significant development across many different technologies remains necessary to meet the long-term expectation of fault-tolerant, universal quantum devices. Recent experimental demonstrations have passed significant milestones in the design, fabrication, and operation of noisy intermediate-scale quantum (NISQ) computing devices [684]. These efforts have been highlighted by the recent public announcement of an experimental demonstration comparing the time and power performance of a 53-qubit superconducting processor to the world's fastest supercomputer [773] as well as the doubling of a device-specific benchmarks for another 20-qubit processor [883]. Quantum engineering advances underscore the importance of tracking the rapid technical progress in quantum information processing and to forecast future developments in quantum engineering research. These insights are necessary to monitor the overall growth in sophistication of quantum engineering. A five-layer system to that end has been proposed in Germany [738].

Methods for tracking the development of quantum information processing are under active development by the research community [760, 826, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893]. Those methods seek to evaluate the salient features and behaviors of quantum information devices as well as the performance for their expected usage. Many metrics and benchmarks for quantum information processing are intended to be representative of device growth and device performance by building on techniques used for device characterization, verification, and validation. In addition, metrics tailored to device usage draw from monitoring conventional notions of time, accuracy, and precision. More broadly, metrics for quantum information processing have been defined at different levels of abstraction including the physical, logical, and system levels. These metrics represent the concerns of information processing as well as the concerns that are unique to quantum information. The IEEE has engaged in several efforts to build a structured community for discussing these points and building scientific consensus [894].

Presently, the global community is debating the metrics and benchmarks designed around the expected use cases and technology layers for quantum information processing devices. In this description, use cases represent a category that identifies a designed purpose for a quantum computing device or system. Common examples include noisy, intermediate-scale quantum devices, quantum annealers, and quantum simulators. Technology layers identify the levels of design complexity in a quantum computing device or system. These layers include the low-level physical registers storing quantum states, the integrated control systems expressing quantum operations, and the system-level performance concerns for specific applications.

Existing metrics for quantum devices characterize the noise in the physical register and the errors observed from low-level physical gate operations. Methods for characterizing noise are generally device dependent and the results tailored to the specific device instance. The aggregate effects of sources of errors also have been proposed for evaluating device performance, but outstanding questions remain on how to connect these metrics to application performance. In the context of application performance, time-to-solution has been used as a device-agnostic method of comparison across solution methods. However, current devices are too small to enable broad ranges in problem evaluation and the comparison of quantum technologies against conventional devices is complicated by vastly different levels of technology maturity. While all leading demonstrations focus on advancing a chosen metric, there remains a lack of direct connection between experimental achievements and the forecasting of fault-tolerant quantum information processing [895]. The related topics of device verification and validation have also emerged as important to quantum engineering research [896].

4.5. ACTIVE RESEARCH QUESTIONS FOR QIP

Superconducting quantum computing requires further development, lower error rates, and scale (number of qubits) to clearly demonstrate the improved performance of important applications. Integrated circuit technologies are required that are scalable and address the special needs of quantum circuits [897]. More work is needed to explore potential applications for quantum algorithms and to develop suitable quantum processor architectures. As mentioned above, the integration of superconducting digital electronics with superconducting qubits for control and readout holds promise for scaling to significantly larger systems than is possible with present state-of-the-art approaches [815].

Table CEQIP-25 Difficult Challenges for QIP

Near-Term Challenges: 2022–2028	*Summary of Issues and Opportunities*
Physical qubits	Design and fabrication of qubit devices with enhanced qubit coherence times and gate fidelities
Logical qubits	Implementation of fully error-corrected logical qubits and protected gate operations
Readout of qubits	Development of scalable, cryogenic qubit readout hardware
Interconnects, cryogenic to room temperature	Development of low thermal conductance and high bandwidth interconnects between different temperature stages of cryogenic- and room-temperature electronics

5. CHALLENGES

The top near term challenges for superconductor electronics (SCE) and quantum information processing (QIP) are given in the table below. These are a very high-level summary of challenges that the industry needs to address for this IFT.

Table CEQIP-26 Difficult Challenges Summary

Near-Term Challenges: 2022–2028	*Summary of Issues and Opportunities*
SCE: Integrated circuit fabrication	Foundries for commercial production now process 200 mm or smaller wafers using equipment lacking state-of-the-art capability. Achieving the yield and throughput for large-scale applications will require process improvements and, possibly, a move to 300 mm wafers. Planarization and thickness control is challenging in stacks of multiple superconductor layers when the layer thicknesses remain the same, rather than increasing with layer number as in CMOS back-end processes.
SCE: Device variability	Variation in device parameters reduces the operating margins of circuits. Needed is better process control, better device designs, or circuit designs that tolerate or compensate for device variability.
SCE: High critical current density junctions (J_c > 100 μA/μm^2)	The AlO_x barrier in Josephson junctions with J_c = 100 μA/μm^2 is now approximately 1 nm thick. Thinner barriers increase J_c, allowing smaller and faster JJs. For J_c > 500 μA/μm^2 the sub-gap resistance can be sufficiently low to eliminate the need for shunt resistors. Uniformity control will be challenging as defects typically dominate conduction through thinner barrier layers and thickness control is also difficult. Materials and process development is needed to improve uniformity and control of devices with high J_c.
SCE: Electronic design automation (EDA) tools	EDA tools for CMOS are not adequate for SCE. Inductance is critical in superconducting circuits and connecting wires must have inductance values within a specified range. Circuit simulators and timing analysis must be modified for pulse-based logic. Flux trapping analysis—both for trapping probability and the coupling of trapped flux in moats to circuits—is required, while analysis of the coupling of bias current and ground plane return currents to circuit structures are also important and difficult at chip level.
SCE: Packaging	Operation at cryogenic temperatures requires different materials, packaging, testing, and cooling systems, much of which will require new development. State-of-the art systems package a few superconductor ICs in a commercial cryostat. Scaling up to systems with higher complexity chips and multi-chip modules will require further reduction of power consumption by all components. Josephson junctions are extremely sensitive to magnetic fields and require shielding, which becomes more challenging as system volumes grow.
QIP: Qubit, physical	Identify qubit technology with the best overall characteristics for use in quantum computing.
QIP: Qubit, logical	Demonstrate logical qubits and error correction sufficient for scaling to larger systems.

6. SUMMARY

This IRDS chapter surveys Cryogenic Electronics (sections 2 and 3), and Quantum Information Processing (section 4), which include alternatives to conventional CMOS technologies. Although novel functionalities and applications have been a primary objective of cryogenic electronics and quantum information processing, high performance, large system energy efficiency, or low power dissipation at cryogenic temperatures could become important as well.

6.1. SUPERCONDUCTOR ELECTRONICS (SCE)

Logic families continue to develop with very different characteristics. The maximum number of Josephson junction switching elements in a circuit is around 1 million.

Cryogenic random-access memory (RAM) with sufficient density and capacity continues to be the most important need for superconductor electronics. Memory based on logic-style Josephson junctions is most developed but has not yet achieved 1 Mibit capacity.

Roadmaps for various aspects of SCE technology were introduced in the 2020 edition.

6.2. CRYOGENIC SEMICONDUCTOR ELECTRONICS (CRYO-SEMI)

Monitoring of applications, drivers, and technologies will continue. No areas seem ready for roadmapping at this time.

6.3. QUANTUM INFORMATION PROCESSING (QIP)

Monitoring of applications, drivers, and technologies will continue. No areas seem ready for roadmapping at this time, although some are close.

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