Advancing Technology for Humanity

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS™

2022 EDITION

LITHOGRAPHY

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Acknowledgments

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LITHOGRAPHY

1. INTRODUCTION

1.1. OVERVIEW

Historically, improvements in lithography have been key enablers to make improved chip technologies. The International Roadmap for Devices and Systems (IRDS) Lithography roadmap predicts how current patterning capability can support future chip generations and where challenges and improvements are needed. It gives a roadmap of expected key lithography requirements. It is intended to be used by semiconductor industry participants, by industry analysts, and by researchers who want or need to know how the industry will evolve in the future and what challenges need to be addressed.

1.2. DEVELOPMENT OF ROADMAP

This roadmap was developed through consultation with an international team of patterning experts and review of publicly available literature and other available documents. The current contributing membership is shown in the Acknowledgments. Contributing members come from Asia, Europe, and the United States and represent semiconductor, equipment, and material manufacturers, as well as research institutes. The IRDS More Moore focus team provides the device roadmap from which lithography requirements are derived. Through polls of the lithography team members the key options, their timing and their key challenges are developed. These are codified in a set of Excel tables and those tables were used to write this document. The table and this document undergo internal review by the team and by the overall IRDS before publication.

1.3. LITHOGRAPHY DRIVERS

This roadmap projects future patterning needs and where the key challenges are. In the past, both logic and memory devices have driven improvements in patterning technology. Currently, high-performance logic devices are leading the way to smaller critical dimensions and driving the introduction of novel patterning technology. New DRAM devices are continuing to be introduced with smaller critical dimensions (CDs), but trail logic in smallest resolution. Flash memory is scaling using 3D structures that have relatively large CDs and does not need higher resolution patterning to make progress.

1.4. INDUSTRY CHANGES SINCE 2020 LITHOGRAPHY ROADMAP

The biggest change since 2020 is the strong establishment of EUV lithography, which uses 13.5nm wavelength light for imaging. Advanced logic products are now dependent on it and DRAM makers are starting to use it. The number of EUV tools in service keeps growing, with over 100 EUV exposure tools in operation worldwide by the end of 2021. The challenges are now extending EUV to smaller dimensions and improving its productivity, rather than just making it work. EUV does use a lot of energy because the efficiency of light production is low, and this is an economic and environmental concern. As projected in the 2020 roadmap, there is a need for better EUV resist systems and work is underway on new chemistries for EUV patterning.

There was progress in alternative patterning technologies. Implementation of nanoimprint in flash memory manufacturing seems to have been delayed, but there is much reported activity improving the productivity of nanoimprint. There is also activity on electron-beam direct write with more tools being announced. This technology will not replace high volume lithography but hopes to provide cost effective chip personalization and perhaps chip prototype development. Optical direct write exposure systems have been developed for advanced packaging. [1,2]

2. TECHNOLOGY REQUIREMENTS

The table below shows the projected lithography technology requirements.

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Table LITH-1 *Lithography Technology Requirements*

Parameter	2022	2025	2028	2031	2034	2037
MPU / Logic						
Logic device technology naming [F}	G48M24	G45M20	G42M16	G40M16T2	G38M16T4	G38M16T6
Logic Industry "Node Range" Labeling	"3nm"	"2nm"	"1.5nm"	"1.0nm eq"	"0.7nm eq"	"0.5nm eq"
Logic device structure options	FinFETLGAA	LGAA	LGAA	LGAA-3D	LGAA-3D	LGAA-3D
MPU/ASIC Minimum Metal ½ pitch (nm)	12.0	10.0	8.0	8.0	8.0	8.0
Metal LWR (nm) [C]	1.8	1.5	1.2	1.2	1.2	1.2
Metal CD control (3 sigma) (nm) [B]	1.8	1.5	1.2	1.2	1.2	1.2
Contacted poly half pitch (nm)	24.0	22.5	21.0	20.0	19.0	19.0
Physical Gate Length for HP Logic (nm)	16.0	14.0	12.0	12.0	12.0	12.0
Gate LER (nm) [C]	1.1	1.0	0.8	0.8	0.8	0.8
Gate CD control (3 sigma) (nm) [B]	1.6	1.4	1.2	1.2	1.2	1.2
Overlay (3 sigma) (nm) [A}	2.4	2.0	1.6	1.6	1.6	1.6
Metal CDU (nm)	1.8	1.5	1.2	1.2	1.2	1.2
Metal LER (nm)	1.3	1.1	0.8	0.8	0.8	0.8
MPU/ASIC finFET fin minimum 1/2 pitch (nm)	12.0					
FinFET Fin width (nm)	5.0					
Fin CD control (3 sigma) (nm) [B]	0.5					
FIN LER (nm) [C]	0.35					
Lateral Gate All Around (LGAA) pitch		26.00	24.00	24.00	23.00	23.00
LGAA minimum width		7.0	6.0	6.0	6.0	6.0
LGAA CD control (3 sigma) (nm) [B]		0.7	0.6	0.6	0.6	0.6
GAA LwR (nm) [C]		0.7	0.6	0.6	0.6	0.6
MPU/ASIC minimum contact hole pitch (nm)	48	45	42	40	38	38
MPU/ASIC minimum contact hole CD (nm)	24	23	21	20	19	19
MPU/ASIC Via pitch	34	28	23	23	23	23
MPU/ASIC Via half pitch	17	14	11	11	11	11
MPU/ASIC minimum contact hole or via CDU (nm)	2.55	2.12	1.70	1.70	1.70	1.70
DRAM						
Dram Minimum 1/2 pitch (nm)	17	14	11	8.4	7.7	7.0
CD control (3 sigma) (nm) [B]	1.7	1.4	1.1	0.8	0.8	0.7
Mininum contact/via after etch (nm) [D]	17	14	11	8.4	7.7	7.0
Minimum contact/via pitch(nm)[D]	51	42	33	25	23	21
Overlay (3 sigma) (nm) [A]	3.4	2.8	2.2	1.7	1.5	1.4
Other Memory						
3D Cross Point technology node minimum feature CD (nm)	20	20	10	10	10	10
3D Cross Point ReRAM technology node minimum feature CD (nm)	20	20	10	10	10	10
Chip size (mm ^{2})						
Maximum exposure field width (mm) [E]	26	26	26	26	26	26
Maximum exposure field length, i.e. scanning direction (mm) [E]	33	16.5	16.5	16.5	16.5	16.5
Maximum field area printed by exposure tool (mm ^{2}) [E]	858	429	429	429	429	429

The key lithographic targets for 2022 and beyond are similar to those in our 2020 report.

Patterning resolution is not a key challenge until 2028 or 2031, when minimum half pitches are below 10 nm. Up to that time, multiple patterning with 0.33NA EUV can meet requirements. We project that EUV lithography will be extended by using multiple patterning and by using higher NA. Multiple patterning is the use of more than one exposure for one pattern to overcome tool resolution limits or the use of multiple process steps to increase the pattern density by chemical deposition and removal processes. Starting in 2025 0.55 NA EUV patterning is projected to be available and this will provide an alternative to 0.33 NA multiple patterning. Key challenges are CD control, LWR, LER and CDU and overlay. These challenges are discussed below.

3. Potential Solutions

EUV lithography using a numerical aperture (NA) of 0.33 is the current workhorse for leading-edge semiconductor manufacturing. Although 12-nm half-pitch is optically resolvable by 0.33 NA optics, limitations in EUV resists means that multiple patterning will most likely be used at this dimension. High-NA EUV exposure tools with NA = 0.55 are expected to be available for chipmaker use in 2024 and could potentially be used for patterning 10-nm half-pitch in 2025. Alternatively, such dimensions can be achieved using multiple patterning with NA = 0.33. For multiple patterning to involve only two EUV exposures, edge placement errors will need to be very small.[3] For extension long-term, high-NA EUV lithography, both single

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and multiple patterning could be used. A shorter EUV wavelength (λ=6.X nm) is also being investigated as a means of extending EUV lithography. Extensions of EUV lithography will be discussed further in the next section.

Table LITH-2 Potential Solutions for Leading-Edge Logic Lithography

	2022	2025	2028	2031	2034	2037
Logic node	3 nm	2.1 nm	1.5 nm	1.0 nm	0.7 nm	0.5 nm
Node	G48M24	G45M20	G42M16	G40M16T2	G38M16T4	G38M16T6
Minimum ½-pitch	12 nm	10	8 nm	8 nm	8 nm	8 nm
Primary options for logic	EUV 0.33.NA multiple patterning	EUV 0.33.NA multiple patterning EUV 0.55.NA single patterning	EUV 0.55.NA single patterning EUV 0.55.NA multiple patterning	EUV 0.55.NA single patterning EUV 0.55.NA multiple patterning Beyond EUVL (λ=6.X nm)	EUV 0.55.NA single patterning EUV 0.55.NA multiple patterning Beyond EUVL (λ=6.X nm)	EUV 0.55.NA single patterning EUV 0.55.NA multiple patterning Beyond EUVL (λ=6.X nm)
Potential solutions for cost reduction, LER reduction		Optical + DSA EUV + DSA	Optical + DSA EUV + DSA	Optical + DSA EUV + DSA	Optical + DSA EUV + DSA	Optical + DSA EUV + DSA

Potential solutions involving directed self-assembly (DSA) are also being explored as a means of reducing the cost of patterning. This approach remains immature and is not expected to be used in HVM prior to 2025.

Although the 5 nm and 3 nm logic nodes will use EUV and may use EUV multiple patterning for their smallest pitches, some critical levels could still use ArF immersion quadruple patterning, particularly where LER and LWR are important considerations, and the patterns are easily adapted to quadruple patterning.

In addition to lithography for the patterning of the critical layers of leading-edge semiconductor devices, there are lithography needs for special applications, such as custom logic, packaging, and photonics. These often have different requirements than for mainstream CMOS logic but are important, nevertheless. Potential solutions for special applications are shown in Table LITH-3. For memory products, nanoimprint is also under consideration.

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Table LITH-3 Potential Lithography Solutions for Special Applications

Application	Year						
	2020	2022	2025	2028	2031	2034	2037
Custom logic			Multi-electron beam	Multi-electron beam	Multi-electron beam	Multi-electron beam	Multi-electron beam
Packaging			Multi-electron beam, optical direct write	Multi-electron beam, optical direct write	Multi-electron beam, optical direct write	Multi-electron beam, optical direct write	Multi-electron beam, optical direct write
Photonics	Low-LER immersion	Low-LER immersion	Low-LER immersion, multi-electron beam, optical direct write	Low-LER immersion, multi-electron beam, optical direct write	Low-LER immersion, multi-electron beam, optical direct write	Low-LER immersion, multi-electron beam, optical direct write	Low-LER immersion, multi-electron beam, optical direct write

4. Current Challenges

4.1. Extensions of EUV

Lithographic technologies have long been extended by increases of numerical aperture, and prototype high-NA EUV lithography tools are currently being fabricated by ASML (with 0.55 NA optics made by Carl Zeiss) and will be available for use by chip makers in 2024. Because of the limited range of angles over which multi-layer reflectors have high reflectance, the lens reduction in the scan direction is increased to 8×, while maintaining a reduction of 4× in the perpendicular direction. This results in a maximum exposure field size on wafers of 26 mm × 16.5 mm, half that of current scanner field sizes. This has implications for fabricating large area chips, as well as for scanner throughput. In addition to the difficulties of building a very complex exposure tool, there are additional challenges for high-NA EUV lithography. These are summarized in the following table. While none of these challenges is considered to be a showstopper, solutions will be non-trivial. Fortunately, not all need to be solved when high-NA exposure tools are first introduced. For example, the benefits of polarized illumination will be small at the pitches at which we expect that high-NA EUV lithography will first be used but will be needed to take full advantage of 0.55 NA optics. Other challenges, such as computational lithography (particularly for addressing mask 3D issues) are already being addressed for EUV lithography at NA = 0.33, but will need to be extended for use at higher NA. The key challenge of stochastics is discussed in the next section.

Longer term, EUV could be further extended by developing tools with a higher NA than 0.55, such as a 0.70NA tool, or by going to smaller wavelength. A 0.70NA tool would use much of the infrastructure already in place for current EUV lithography. Changing to a shorter wavelength, such as 6.Xnm, is also under investigation, but would be a much bigger change than increased NA and be much more challenging. New light sources, multilayer coatings and photoresists would be needed. A shorter wavelength could improve depth of focus compared to high NA at 13.5nm wavelength but would also make stochastics worse.

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Table LITH-4 The Key Challenges of High-NA EUV Lithography

Key challenges
Resists meeting resolution requirements, with low levels of defects from stochastic phenomena and pattern collapse
Light sources that can support photon shot noise and productivity requirements
Solutions for meeting small depths-of-focus at 0.55 NA
Polarization control for maintaining high contrast at 0.55 NA
Computational lithography capabilities
Mask making and metrology infrastructure
Solutions for large dies
Cost of high-NA EUV lithography

4.2. STOCHASTICS

In the 2020 roadmap, we predicted increasing dose-to-print for EUV resists as printed critical dimensions become smaller. For the "3 nm" logic node with a minimum line and space half-pitch of 12 nm and a minimum contact hole pitch of 34 nm, we predicted a dose to print of 64 mJ/cm2 for contact holes. In recent results reported by ASML[4] , 40 nm pitch holes printed at 60 mJ/cm2 and 13 nm lines and spaces at 50 mJ/cm2. This matches the prediction in the 2020 lithography chapter of the IRDS. For the 2022 roadmap, the projected critical dimensions for new nodes are the same as in the 2020 roadmap and our dose to print projection for those CDs is the same as before. This is shown in the figure below.

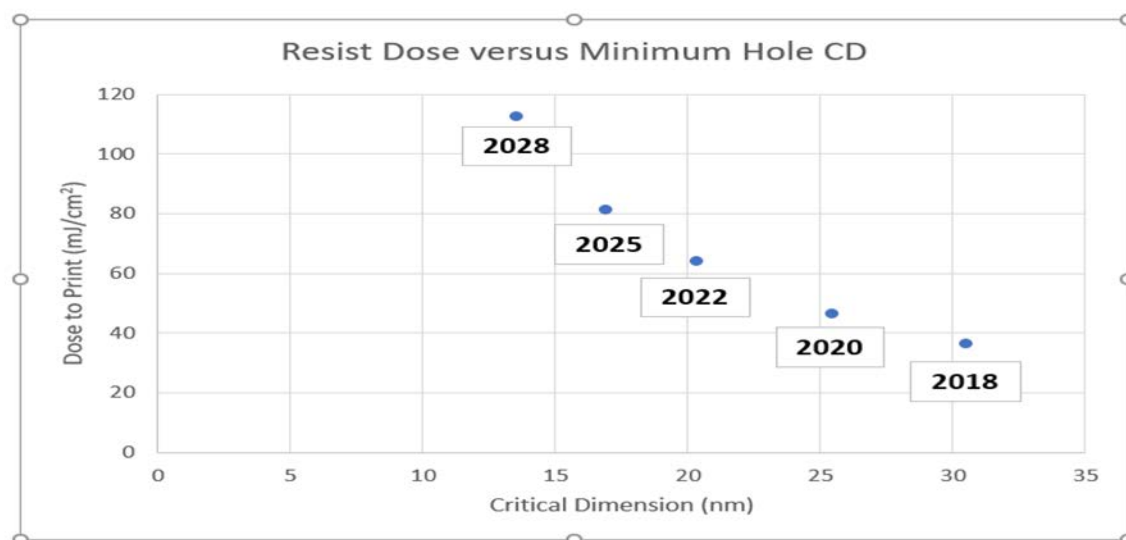

Figure LITH-1 2020 Projected EUV Photo-Speed as a Function of Printed Contact Hole Size

There is another issue that needs to be considered in predicting dose to print. The 2020 projections were based on the dose needed to provide adequate critical dimension uniformity. Lately there has been much work on stochastic defects that can occur, which are defects such as missing or bridged contact holes and bridged or broken lines. These get worse as the feature size is reduced and as the resist dose-to-print decreases. They are much more common than extrapolations assuming a Gaussian distribution would predict. These defects are related to the randomness of photo induced events in in the photoresist and come about when fluctuations in the positions of photo events within or next to a feature such as a contact hole create a barrier to development or

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a path of unwanted development.[5] More photochemical events in the volume of resist defining a printed feature make such defects less common, so resists that require a higher exposure dose to print to size will be needed to reduce these types of defects. For a given exposure dose and resist, a smaller feature will have fewer events so smaller features will have more defects. These defects tend to scale exponentially with feature size.

In order to maintain the same defect rate in a new generation of chips with smaller CDs one will have to maintain a constant number of photo events per feature. If the thickness and optical absorption of the resist remains the same, then the number of photochemical events will be proportional to the area of the feature. All things being equal, and assuming the aerial image improves so that normalized image log slope (NILS) remains constant, the dose-to-print will have to increase inversely to the square of the area of the feature to maintain the same number of photochemical events per feature. In the next two nodes, critical CD shrinks about 20% a node. This means dose to print will have to increase about 50% per node to maintain the same number of photo events per feature. This is a larger increase in dose to print from node to node than was predicted in the 2020 roadmap, but can be mitigated somewhat by an increase in resist optical absorption.

If the thickness of the resist shrinks in order to print the smaller feature, then we expect the resist developers will increase the resist absorption to maintain the same total absorption by the resist film, so the thickness change will not change the result describe above. But it should be noted that it is an optimistic assumption that the same defect rate in the new node as in the old node will be sufficient. If chip size remains the same, there will be more features per chip in the new node which could require a lower defect rate. Also, the More Moore roadmap predicts that chip sizes will get bigger each node, requiring an even lower defect rate. If the occurrence of stochastic defects is limiting the dose to print of EUV resists for the current generation, then dose-to-print could increase at a faster rate than is predicted in the graph shown above.

4.3. DISAGGREGATION

Logic chips typically contain sections requiring high performance such as cache, core, and GPU units and less lithographically demanding analog and I/O sections. The high-performance sections use new technology to shrink their dimensions and give better performance each successive logic node. However, the analog circuitry and the I/O areas don't scale the same way and don't require the smaller critical dimensions. Over time, this can mean that the high-performance sections of chips take up less of their physical area. The extra cost involved in patterning smaller high-performance features also increases the costs of the analog areas. There can be a cost benefit to separating the functions onto different chips as shown in the figures below. The analog and I/O parts can be made with less expensive processes. Then the dies containing the high-performance circuitry will be smaller and therefore less expensive to produce since more die will fit on a wafer. This scheme of making several small chips instead of one larger one is called disaggregation. It requires high performance packaging that is cost effective enough to lead to overall cost savings. If high NA EUV is successfully implemented in 2025, this will have a one half the maximum exposure field size of current EUV exposure tools. The maximum die size will have to be smaller unless some form of stitching between exposure fields is used. When high NA is introduced, the industry will confront either the challenge of making large chips using smaller exposure fields or the challenge of disaggregation when this field size transition occurs.

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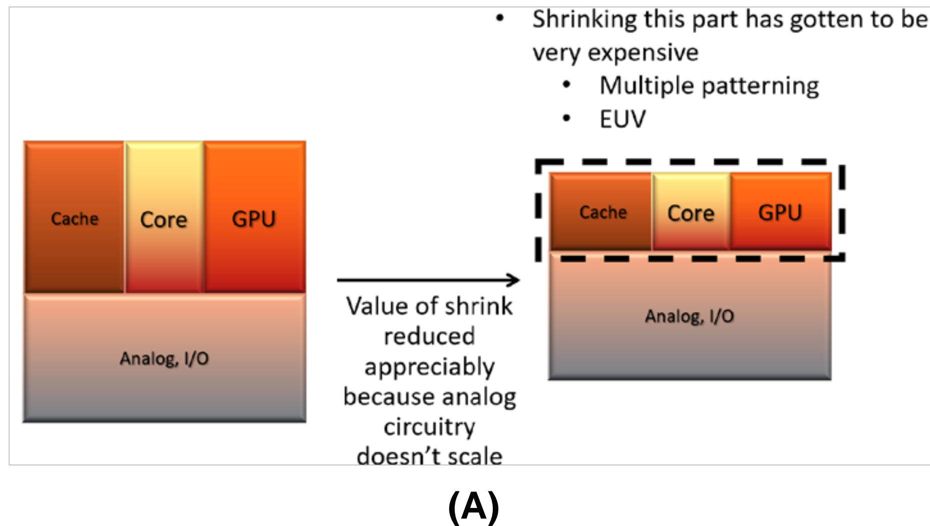
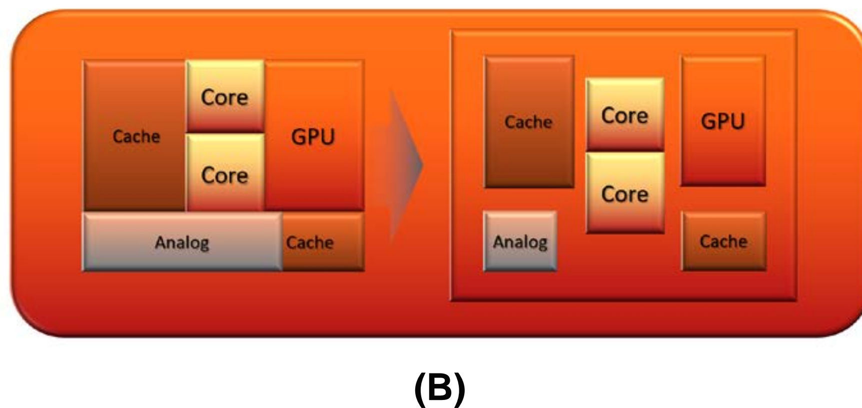


(A)

Figure LITH-1 A: Illustration of how advanced lithography can enable scaling for only for the fraction of chip area composed of high density logic and memory circuitry.[6]



(B)

Figure LITH-2 B: Graphic showing parts of circuits that were fabricated separately using cost-optimized patterning and then integrated using advanced packaging technology. [7]

4.4. MATERIALS

The stochastics calculations referred to above assume that resist technology improves over time. What are the prospects for improvement? Historically, resists have improved.[8] and the reference gives the impression that resist improves somewhat every year. However, for EUV, the reported improvements rates have varied a lot from year to year. Some years, EUV resists have seemed to improve very little when judged by their photospeed to resolution to roughness trade off.[9] Other years, excellent progress is reported.[10]

Comparisons of recent reports of resist performance to older reports is also difficult because recent papers have tended to use "unbiased" LER and LWR measurements instead of "biased" measurements. Using "unbiased" measurements means a procedure was used to remove SEM imaging noise. This gives lower LWR measurements than a "biased" measurement. It's possible that the year-to-year improvement is just inherently noisy, but it is also probably the case that the advent of "unbiased" LWR measurement enabled resist developers to see improvements they couldn't see before and this has improved resist development productivity. And with unbiased LWR measurements, the improvement is evident in the data.

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Current EUV resists in production are of two types, resists using chemical amplification that are related to the resists used for KrF and ArF lithography and resists based on metal compounds. There are several other types of resist chemistries being worked on in development, including different metal-based resists, and non-chemically amplified resists based on organic chemistries. We consider the prospects for improvement for chemically amplified resist to be different than prospects for the other types of resists. Chemical amplification is a well understood type of resist chemistry that has been in use for over two decades. Mathematical simulation of the performance can predict imaged feature dimensions to within a nanometer. Theoretical studies of varying chemically amplified resist parameters show a floor in LWR no matter what materials parameters make up the resist model. Of course, such chemistries need to be modified for EUV, but we believe there is a limit to how much better chemically amplified resist can be, other than making tradeoffs between sensitivity, resolution and LWR.

Dry deposited and developed resists are a different approach to creating a patterning material. They involve CVD deposition of the film to be patterned, followed by exposure, and then followed by wet or dry development. The dry development is done with a reactive ion etch (RIE) type process.[11]

The high energy of EUV photons in principle makes many new types of photoreactions available to the resist developer. Metal based resists are one new EUV chemistry that has been developed. Besides the tin-based materials that have the leading resolution of metal-based resists, there are other metal-based chemistries that are being investigated, and it is likely that these resists will improve their performance in the coming years. Metal based resists have the advantage that it is relatively easy to get enough EUV absorbance for thin film of resist. But high-resolution metal resists are currently only available in negative tone, unlike chemically amplified resists, which are available in both negative and positive tone. Because of EUV mask blank defects, it is currently not practical to use negative resists for contact or via layers, or any other layer that has a low percentage of mask area covered by absorber material.

Recently, dry deposited and developed EUV resists have been reported. They show excellent resolution but require different equipment than do current resists. Also, some non-chemically amplified resists are being explored.[12] They are often too slow in dose to print for use in current nodes, but could meet the expected dose to print for some future nodes. They potentially can have a simpler reaction mechanism than chemically amplified resists and thus have few sources of randomness and stochastic effects. But there are not enough data yet to determine if these new resist types have intrinsically better stochastics than chemically amplified materials or not. We look forward to seeing how these new technologies progress.

4.5. ALTERNATIVE PATTERNING METHODS

High resolution imprint lithography (NIL) uses field-by-field deposition, imprinting and exposure of a low viscosity resist with the imprinting template in place. It has demonstrated resolution of better than 10nm features and overlay sufficient for leading edge 3D NAND flash patterning. It promises a lower cost than alternative patterning methods for high resolution applications. NIL is currently being considered for memory applications such as 3D NAND flash, DRAM and cross point memory, where the requirements on defectivity and overlay are not as stringent as in logic devices. Overlay as low as 2nm mix and match has been demonstrated for full fields, but partial fields are more challenging, and work remains to reduce the errors in these fields. Productivity studies continue as well. Recently, Kioxia has published multiple papers on the subject, and has utilized multiple field printing, spin on NIL resists and gas permeable underlayers as a means of improving tool and process throughput.

While we know of no current program to design and make direct-write (mask-less) e-beam tools suitable (in place of optical exposure tools) for mass production of IC chips, there are multiple suppliers of such tools for advanced packaging and MEMS devices. Some suppliers are also targeting personalization of silicon wafer devices. This mask-less printing capability is complementary to conventional optical printing, with applications in the following areas: patterning full-wafers for low volume or fast design cycles; embedding unique security information into a chip during wafer processing; and patterning wafers with low feature counts of 1D line cuts or via holes to enable reasonable wafer throughput.[13] The initial resolution target for printing capability is sub-100nm with a multi-column design. Multi-beam direct write is already in widespread use for mask making, and approaches under development for personalizing chips, for MEMS or for packaging are also expected to use parallel writing approaches. Overall, direct write technology enables smart and agile digital lithography processing, and we expect it to continue to find applications.

4.6. LITHOGRAPHY ENERGY EFFICIENCY

The energy consumption of leading-edge logic fabs increases every node, with energy requirements increasing roughly 60% from the N7 node to the N3 logic node. EUV provides a simpler, fewer step process than multiple patterning, but the energy requirements of EUV are such that no energy is saved by utilizing EUV. Chip making in Taiwan already uses as much as 10% of the island's electricity.[14] This is a challenge for the environment and for the chip industry, and there are efforts to address this. For example, lasers with much higher electricity-to-light conversion are being investigated for use in laser-produced plasma

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EUV light sources.[15] Free-electron lasers are also expected to be much more efficient in converting electricity to EUV light, and there are multiple efforts world-wide for developing free-electron lasers as sources for EUV lithography.

5. Long term Challenges (2028 and on)

After 2029, logic is projected to scale through device stacking and the minimum half-pitch will not go below 8 nm. DRAM will continue to shrink and will catch up with logic in minimum pitch, but the minimum CD won't be below 8 nm until 2037, when it is projected to be 7 nm. Lithography technology developed for nodes before 2030 will be usable for both logic and DRAM nodes after 2030. The challenges from meeting the technical specifications in the requirements chart change to ones of cost, yield, and process complexity. If the device density doubles solely through doubling the numbers of layers and process steps, the cost per device will not go down and may increase if the yield of good die goes down. This will put pressure on finding ways to simplify processes and reduce processing cost. And a rising number of process steps will put pressure on the yield of each step in order to maintain reasonable device yield. In flash memory, clever device structures that enabled substantial process simplification for multiple layers of devices enabled 3D scaling at affordable device cost. Perhaps analogous innovations can be found for logic.

6. Summary and Key Points

It is expected that lithographic technologies will continue to meet the patterning requirements explicated in the More Moore chapter of the IRDS. Advanced patterning for high volume manufacturing will involve EUV lithography in some embodiment, be it multiple patterning, high-NA, shorter wavelength, or some combination of these. As with prior generations of semiconductor technology, numerous problems, outlined in this chapter, will need to be solved, but no showstoppers are seen. Issues related to stochastics in patterning are expected to be among the most challenging and will persist from node to node.

In addition to EUV lithography, alternative lithographic technologies, such as electron-beam direct write, nanoimprint, and directed self-assembly (DSA) may be applied for special applications. Advanced packaging will also benefit from innovations in lithography.

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7. Acronyms/Abbreviations

Term	Definition
ASIC	Application specific integrated circuit
CD	Critical dimension
CMOS	Complementary metal oxide semiconductor
CoO	Cost of ownership
DRAM	Dynamic random access memory
DSA	Directed self-assembly
EUV	Extreme ultraviolet
FET	Field effect transistor
FinFET	Fin field-effect transistor
GAA	Gate all around
HVM	High volume manufacturing
IC	Integrated circuit
IEEE	Institute of Electrical and Electronic Engineers
IEEE-SA	IEEE Standards Association
IFT	International focus team
IMEC	Interuniversity Microelectronics Centre
ILD	Interlevel dielectric
iNEMI	International Electronics Manufacturing Initiative
I/O	Input/output
IRC	International roadmap committee
IRDS	International Roadmap for Devices and Systems
ISSCC	International Solid-State Circuits Conference
ITRS	International Technology Roadmap for Semiconductors
LER	Line edge roughness
LGAA	Lateral gate all around
LWR	Line width roughness
MEMS	Micro-electro mechanical system
MRAM	Magnetic RAM
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
Mx	Tight-pitch routing metal interconnect
NA	Numerical aperture
NAND	A logic gate (NOT-AND) that produces an output that is false only if all its inputs are true
ORSC	Overall roadmap system characteristics
ORTC	Overall roadmap technology characteristics
OSC	Outside System Connectivity
SDRJ	System Device Roadmap Committee of Japan
VGAA	Vertical gate all around
VLSI	Very large scale integration

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