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INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

2021 UPDATE

LITHOGRAPHY

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LITHOGRAPHY

1. INTRODUCTION

Historically, improvements in lithography have enabled improved chip technologies. The International Roadmap for Devices and Systems (IRDS) Lithography roadmap predicts where current patterning capability can support future chip generations and where challenges and improvements are needed. It is intended to be used by semiconductor industry participants, by industry analysts, and by researchers who want or need to know how the industry will evolve in the future and what challenges need to be addressed.

1.1. LITHOGRAPHY DRIVERS

This roadmap projects how the patterning needs of new devices in the More Moore roadmap might be met and where the key challenges are. In the past, both logic and memory devices at different times have driven improvements in patterning technology. Key drivers of patterning technology have been high performance logic chips, DRAM memory and flash memory. Currently high-performance logic devices are driving the introduction of novel patterning technology. DRAM is continuing to introduce new devices with smaller critical dimensions (CDs), but trails logic in resolution required. Flash memory is scaling using 3D structures that have relatively large CDs and does not need higher resolution patterning to make progress. Memory chip producers are more sensitive to patterning cost than logic chip producers. The cost of patterning is driving flash memory producers to explore nanoimprint lithography.

1.2. DEVELOPMENT OF ROADMAP

This roadmap was developed through consultation with an international team of patterning experts and review of publicly available literature and other available documents. The current contributing membership is shown in the Acknowledgments. Contributing members come from Asia, Europe, and the United States and represent semiconductor, equipment and material manufacturers, as well as research institutes. The IRDS More Moore focus team provides the device roadmap from which lithography requirements are derived. Through polls of the lithography team members the key options, their timing and their key challenges are developed. These are codified in a set of Excel tables and those tables were used to write this document. The table and this document undergo internal review by the team and by the overall IRDS before publication. The tables follow the convention of the More Moore tables and have only columns for each year a new product node is expected to be introduced. Intervening years are omitted. However, in the potential solutions' charts the horizontal axis is time, so the intervening years are included so the reader can readily see the time frames required for innovation. There are two possible options charts, one for lines and spaces and one for hole type patterns such as contacts, vias, cuts and vertical gate all around devices, because these two types of patterning have very different requirements and the timing of innovation is different for each of them. This year is an interim year, so the requirements and possible options tables from last year have not been updated. This white paper and the critical challenges table are updated from 2020 and we have added a white paper on line edge roughness (LER).

2. TECHNOLOGY REQUIREMENTS

2.1. SUMMARY

The More Moore requirements related to lithography are shown in Table LITH-1 below, along with the Lithography team's color coding for feasibility. EUV has been used successfully in high-volume chip production for over a year. Feature sizes that can be done with extreme ultraviolet (EUV) single patterning are coded in white. Features that can be done with EUV multiple patterning are coded in yellow, meaning "manufacturing solutions are known," because both multiple patterning and EUV are established in volume manufacturing. Combining them is a question of cost, not feasibility. This means that all lines and space CDs in the roadmap are coded yellow, except for the 8-nm and 7-nm generation DRAM projected for manufacturing in 2031 and 2034, respectively, and the minimum metal half-pitch for logic nodes expected in 2028, 2031 and 2034. The logic contacted poly half-pitch and the physical gate length for high performance logic are coded white to the end of the table. This is because these two dimensions are set by thin film deposition processes and not set lithographically. The projected sizes of hole patterns, such as contacts, vias and cuts are more challenging. Cells are coded red where we judge EUV multiple patterning insufficient to reach the dimensions. Red cells for such CDs start appearing in 2025.

Line edge roughness (LER) and critical dimension uniformity (CDU) are the main challenges in the requirements other than reaching the desired critical dimension. Red coded cells start to appear in 2025.

High numerical aperture (NA) EUV exposure tools with a reduced field size are projected to be available in the second half of 2022, in time for the 2025 column shown in Table LITH-1. However, there are challenges associated with such lithography tools. Besides the normal challenges for new tool generations of overlay, resolution, aberrations and such, stochastic effects will be worse with smaller features. EUV masks will also need improvement. The reduced field size of high-NA exposure tools will necessitate stitching for the fabrication of chips that are too large to fit into a 26 mm × 16.5 mm exposure field. Multiple patterning with existing EUV could compete with high NA EUV as an option for 8 to 12 nm half-pitch lines and spaces. The choice of patterning option could be based on cost considerations rather than technical capabilities.

Overall, the successful implementation of EUV has meant that the roadmap's major challenges are no longer resolution. Instead, the major challenges are related to overlay, critical dimension uniformity (CDU), LER, and cost.

Table LITH-1 Lithography Technology Requirements

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
DRAM							
DRAM minimum ½ pitch (nm)	18	17.5	17	14	11	8.4	7.7
Key DRAM Patterning Challenges	Resolution improvements at reasonable cost						
CD control (3 sigma) (nm) [B]	1.8	1.8	1.7	1.4	1.1	0.84	0.8
Mininum contact/via after etch (nm) [H]	18	17.5	17	14.0	11	8.4	7.7
Minimum contact/via pitch(nm)[H]	54	53	51	42	33	25.2	23
Overlay (3 sigma) (nm) [A]	3.6	3.5	3.4	2.8	2.2	1.68	1.5
MPU / Logic							
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
Key MPU/Logic Patterning Challenges	EPE, Single Exposure for <36nm pitch, Cost of EUV patterning						
MPU/ASIC Minimum Metal ½ pitch (nm)	18	15	12	10	8	8	8
Metal LWR (nm) [C]	2.7	2.3	1.8	1.5	1.2	1.2	1.2
Metal CD control (3 sigma) (nm) [B]	2.7	2.3	1.8	1.5	1.2	1.2	1.2
Contacted poly half pitch (nm)	27.0	24.0	22.5	21.0	20.0	19.0	19.0
Physical Gate Length for HP Logic (nm)	20	18	16	14	12	12	12
Gate LER (nm) [C]	0.8	0.7	0.6	0.5	0.4	0.4	0.4
Gate CD control (3 sigma) (nm) [B]	1.1	1.0	0.9	0.7	0.6	0.6	0.6
Overlay (3 sigma) (nm) [A}	3.6	3.0	2.4	2.0	1.6	1.6	1.6
MPU/ASIC finFET fin minimum 1/2 pitch (nm)	16.0	14.0	12.0				
FinFET Fin width (nm)	8.0	7.0	6.0				
Fin CD control (3 sigma) (nm) [B]	0.80	0.70	0.60				
FIN LER (nm) [C]	0.80	0.49	0.42				
Lateral Gate All Around (LGAA) 1/2 pitch				11	10	10	10
LGAA minimum width				7	6	6	6
LGAA CD control (3 sigma) (nm) [B]				0.7	0.6	0.6	0.6
GAA LER (nm) [C]				0.49	0.42	0.42	0.42
MPU/ASIC minimum contact hole or via pitch (nm)	51	42	34	28	23	23	23
Via CD after etch (nm) [H]	18	15	12	10.0	8.0	8.0	8.0
Contact CD (nm)after etch - finFET, LGAA	18	16	17	18	20	18	18
Chip size (mm^2)							
Maximum exposure field width (mm) [E]	26	26	26	26	26	26	26
Maximum exposure field length, i.e. scanning direction (mm) [E]	33	33	33	16.5	16.5	16.5	16.5
Maximum field area printed by exposure tool (mm^2) [E]	858	858	858	429	429	429	429
Calculated values for figures							
minimum half pitch (DRAM, MPU metal) (nm)	18	15	12	10	8	8	8
minimum half pitch (Flash, MPU fin, LGAA) (nm)	15	14	12	11	10	10	10
minimum hole pitch (DRAM, MPU, VGAA) (nm)	51	42	34	28	23	23	23
minimum contact CD after etch (DRAM, MPU, Flash) (nm)	18	15	12	10	8	8	8
minimum CD control(DRAM, MPU, Flash) (3 sigma) (nm)	1.1	1.0	0.9	0.7	0.6	0.6	0.6
minimum required OL (DRAM, Flash, MPU) 3 sigma (nm)	3.6	3.0	2.4	2.0	1.6	1.6	1.5
Estimated Cut pitch (1.4 x minimum metal pitch)	51	42	34	28	23	23	22
minimum LER (nm)	0.8	0.5	0.4	0.5	0.4	0.4	0.4
Gate Pitch	54	48	45	42	40	40	40
One half gate pitch	27	24	23	21	20	20	20
Gate lentgh (nm)	20	18	16	14	12	12	12

3. POTENTIAL SOLUTIONS

3.1. LINE AND SPACE POTENTIAL SOLUTIONS

Lines and spaces are the flagship pattern of lithography. In practice, the minimum imageable half-pitch for lines and spaces is smaller than the minimum imageable half-pitch for contact hole patterns, so when leading edge resolution is discussed it usually refers to dense line and space capability. The roadmap predicts that logic metal levels will drive improvements in line and space resolution. Figure LITH-1 from the 2020 roadmap shows different product nodes and their projected time frames for implementation along with possible patterning options for each node. Note that the logic node names are the commonly used names for each node but are not the same as the minimum half pitches of those nodes. Resolution improves to 12 nm half-pitch in 2022. This corresponds to the logic "3 nm" node. The IRDS expects that this resolution will be achieved through EUV double patterning. Then there is a further decrease in line and space resolution of 2 nm per node until 2028, when minimum line and space resolution is expected to reach 8 nm half-pitch. The 8 nm half-

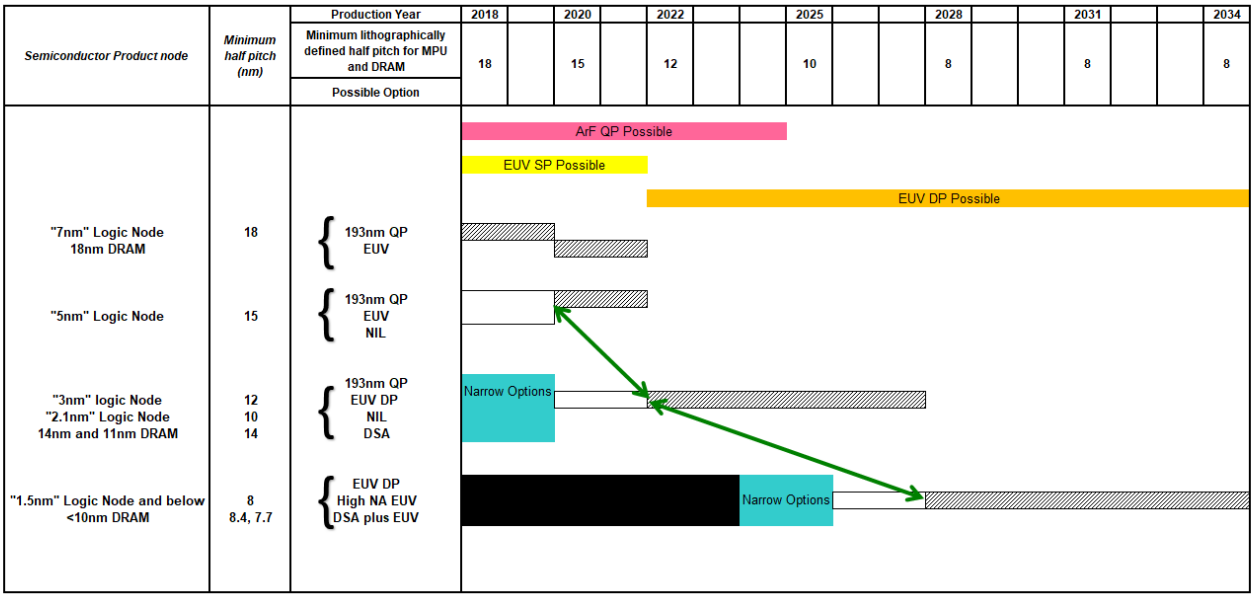

Figure LITH-1 Line and Space Potential Solutions

pitch could be achieved with EUV double patterning, but there is time to develop other methods also, such as high-NA EUV lithography. After that, no further improvement in required resolution is projected, although this is due to projected device requirements, not expected limitations in patterning capability. Although the 5 nm and 3 nm logic nodes will use EUV and may use EUV multiple patterning for their smallest pitches, some critical levels could still use ArF immersion quadruple patterning, particularly where LER and LWR are important considerations and the patterns are easily adapted to quadruple patterning. For multiple patterning to involve only two EUV exposures, edge placement errors will need to be very small.[1] It is also possible that improvements in EUV single patterning will occur, enabling smaller half-pitches with EUV single patterning. For DRAMs, either quadruple patterning with ArF immersion, EUV or nanoimprint lithography (NIL) will be used for nodes down to 10 nm half pitch.

3.2. CONTACT HOLE, VIA AND CUT TYPE PATTERN POTENTIAL SOLUTIONS

In the past, contact holes and other hole type patterns usually have had a larger minimum pitch than the lines and spaces in a memory or logic device. Double patterning of hole structures gives a 30% shrink of CD unlike pattern doubling of lines and spaces which gives a 50% shrink. More exposures are needed for multiple patterning of hole patterns than of line and space patterns. Hole patterns are therefore one of the first implementations of EUV. Potential solutions for hole type patterns are shown in Figure LITH-2. EUV double patterning will have adequate resolution through the "3 nm" logic node in 2022.

After that either high NA EUV or some other technique will be needed. Whatever technique that is used for the node after that, it will suffice for the rest of the projected roadmap.

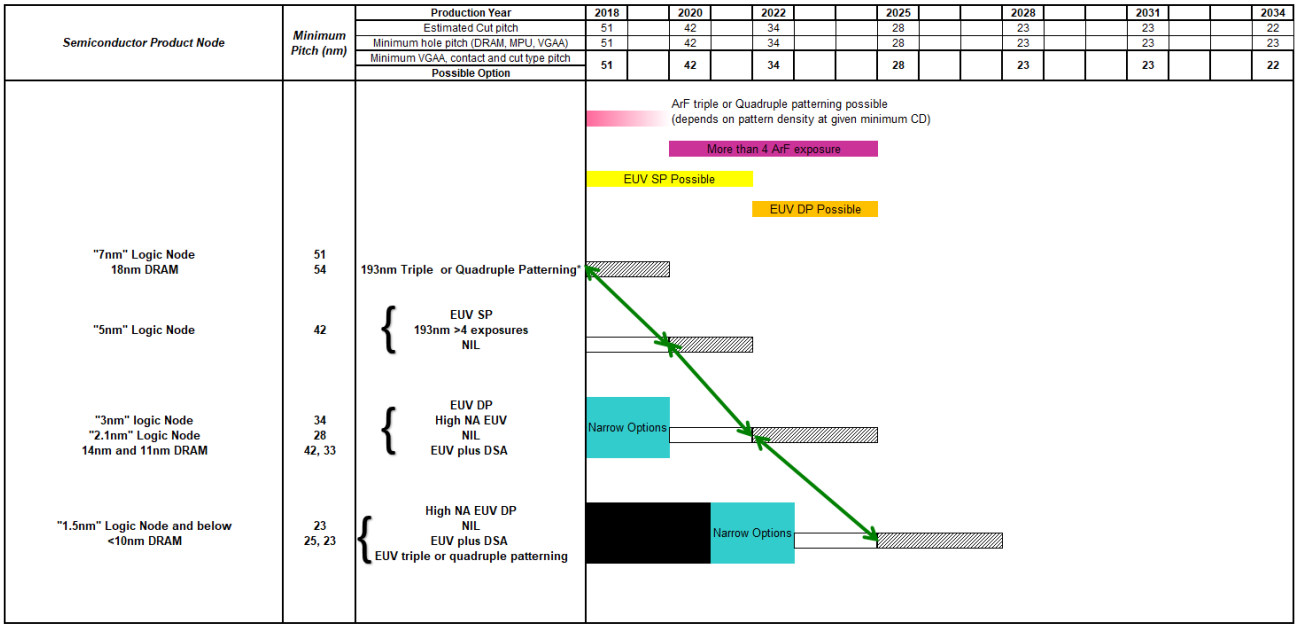

Figure LITH-2 Contact Hole, Via and Cut Type Pattern Potential Solutions

4. CHALLENGES

4.1. SHORT-TERM CHALLENGES (2020 TO 2025)

With the successful implementation of EUV in manufacturing, patterning challenges for logic and DRAM have shifted from resolution to noise, defects, overlay and edge placement. Noise is the variation in pattern placement, shape and size to the random nature of photon events, electron events, molecular positions and molecular quantities. For flash memory the challenges are cost and demonstrating nanoimprint lithography with sufficiently low defects and cost.

Some of the defect challenges relate to keeping masks clean. Although pellicles are available, their transmission is low, thereby reducing exposure tools throughput significantly. It is reported that EUV users have chosen not to use them because their light absorption has a substantial negative effect on throughput. Recently, IMEC has announced the promising results with pellicles based on carbon nanotubes that have up to 97% transmission, but this technology has not yet been commercialized.

Other defects are due to what are called stochastics, which are random variations in light exposure and in resist chemistry. Stochastic defects come from random variations in the number of photons and electrons in a discrete exposure of a small area and come from the random placement, reaction and dissolution of the various molecular components that make up photoresist. These defects can take the form of bridging between lines, missing contact holes, line opens or merged contact holes. Recent work has shown that they are actually more common than simple extrapolation of CD variation assuming a normal distribution would predict. These sorts of defects currently limit the usable resolution of EUV tools. There are fewer such defects with slower resist, so EUV users typically use slower resists than they would like. A slower resist is one that requires a higher exposure dose to define the desired pattern. This results in decreased exposure tool throughput and more expensive exposures. Long term, the need to utilize slower resists is expected to drive the development higher power light sources and/or a more efficient optical train in exposure tools to maintain current HVM (High Volume Manufacturing)_acceptable benchmark productivity.

Stochastic defects do not scale well. Even if stochastic variations were the same magnitude for smaller features, they would be a larger fraction of that features size. But in fact, as printed feature sizes get smaller, the variations get bigger rather than

smaller, so this is a twofold challenge. Photo-speed of the resist (relative to EUV light intensity at the wafer) is the limiting factor for EUV tool throughput and is a critical parameter for the cost and feasibility of an EUV process. The IRDS lithography team decided to prepare an EUV photo-speed roadmap.

To do the photo-speed roadmap we took the 7-nm logic node as a baseline. Since this node is in production that noise must be at an acceptable level for the 7-nm critical features and the photoresist used is as fast as it can be while still giving acceptable noise. We used a CDU specification of 15% of CD as an acceptable variation in HVM. The expected three sigma variation of 7-nm node contact hole critical dimensions is then 3.82 nm. The actual stochastic variation comes from both chemical noise and shot noise. It is instructive to consider the limiting cases. If all of the noise were due to random variation in the dose per hole due to shot noise effects, then effective resist doses at the wafer plane would have to double each node to come close to meeting projected CDU specifications for future nodes. If all of the contact hole CDU came from resist randomness, then the resist randomness would have to improve by about 20% each logic node to keep meeting CDU targets. If half the noise came from each factor, then neither 20% resist improvement per node by itself nor 100% effective wafer plane dose improvement per node by itself would enable new nodes to meet specifications. An improvement in both factors would be needed. How much noise is from photons and from resist chemistry separately is not agreed on in the literature. Estimates vary of how much of the variation is due to photons and how much is due to resist noise, but in all cases the photon noise is a significant part of the observed CD variation. Without an unexpected breakthrough, one cannot meet future specifications for critical dimension without slowing down the resist and using a higher exposure dose.

To estimate how much resist dose will need to increase, we used k_4 methodology[2] that has been recently described. The k_4 value is a measurement of the noise in a resist feature relative to the contrast in the aerial image, the exposure dose and the actinic wavelength. This methodology uses NILS, the normalized image log slope, as a measure of the quality of the aerial image. Our baseline numbers for the 7nm logic node were a NILS of 2.5, an exposure dose of 36mJ/cm^2 and a k_4 of 6. We project that NILS will stay constant from node to node at around 2.5 as improvements in EUV masks and exposure tools compensate for decreases in NILS due to decreasing feature size. The k_4 value is a measure of resist performance and we project an improvement of 6% per node. This number comes from studies of historical improvement in k_1, which is a dimensionless expression of imaging resolution performance adjusted for wavelength, exposure tool numerical aperture and feature size. It should be noted that this historical data comes from historical I line and KrF resist improvements. There are reasons both for optimism and pessimism about whether resist developers can match this rate of improvement in improving EUV resists The historical improvement rate occurred when resist developers had ready on-site access to exposure tools and the chemistries in use were newly under development. The first is not the case for EUV and the second is only partially the case, so this assumption of 6% improvement may be an optimistic assumption. On the other hand, metal based resists are a new class of resist and could have potential for much improvement, and new resist technologies could still appear. For example, recently LAM has described research on a dry deposited and developed resist for EUV. Based on these assumptions, we get the following projection for future EUV resist exposure doses. The effective exposure dose necessary is projected to increase roughly 33% each logic node, until logic switches to 3D device scaling in 2031.

Table LITH-2 EUV Dose to Print Roadmap

YEAR OF PRODUCTION	*2018*	*2020*	*2022*	*2025*	*2028*	*2031*	*2034*
	G54M36	G48M36	G45M24	G42M20	G40M16	G38M16T2	G38M16T4
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Calculated Resist Dose to meet target LCDU (mJ/cm2)	36	46	64	81	112	99	95
Node to node percent change in dose		27%	38%	27%	38%	-12%	-5%

The increase in printing dose is driven mostly by the decrease in minimum CD and somewhat by improvements in photoresist. The changes in predicted exposure dose from node to node are not always the same because the percent change in minimum CD is not always the same from node to node. After 2028, CDs stop shrinking but further improvements in resist are projected so doses decline a little. A graph of predicted lithographic printing dose necessary versus contact hole CD is shown below.

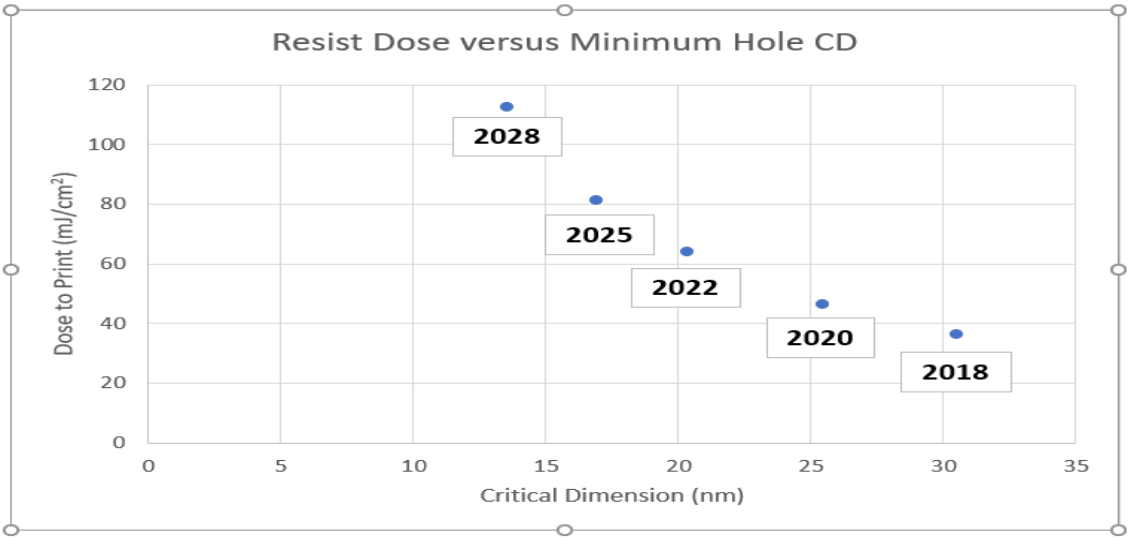

Figure LITH-3 Projected EUV Photo-Speed as a Function of Printed Contact Hole Size

Near term challenges, together with target applications and potential earliest timing for each of the options discussed above are shown in Table LITH-3 as a function of the patterning approach.

Table LITH-3 2021 Lithography Difficult Challenges

Next Generation Technology	First Possible Use in HVM	Feature Type	Device Type	Key Challenges	Required Date for Decision making
EUV Multiple Patterning	2022	12nm hp LS	"3nm" Logic Node	• Process control (EPE, overlay, CDU, LER/LWR) • Cost/throughput	2021
EUV high NA	2025	10.5nm hp LS	"2.1nm" Logic Node	• Resist capability (sensitivity, LER/LWR, resolution , defects) • Stitching of two mask patterns • Improved masks for high NA • Cost/Throughput	2024
NanoImprint	2021	20 nm lines and spaces 20 to 30nm contact holes	3D Flash Memory	• Defectivity • Overlay • Master Template fabrication and inspection <20nm • Defect repair • Mass-production capacity	Product Evaluation Underway
DSA (for pitch multiplication)	2022	Contact holes/cut levels for logic Possibly nanowire patterning	"3nm" Logic Node	• Defectivity and defect inspection • Pattern Placement • Design • 3D Metrology	2021

4.2. LONG-TERM CHALLENGES (2028 AND BEYOND)

After the "1.5 nm" logic node goes into production in 2028, logic dimensions will stop shrinking and improved densities will be achieved by increasing the number of devices vertically. DRAM will continue to shrink CDs after that, but the minimum lines and spaces will only shrink modestly and should be reachable by improved EUV and EUV double patterning. The large number of masking levels and the many steps for 3D stacking of devices will make yield and cost high priorities. So, potential patterning challenges will probably be related to cost, yield and defectivity, imaging over

topography, and alignment and overlay over complicated 3D stacks. Etch and deposition of sub 10 nm structures are also major challenges.

5. NOVEL TECHNOLOGIES

Nanoimprint lithography has made significant progress in recent years. Key challenges are defects, overlay and throughput. Recent reports show defects of 0.2/cm^2 for a wafer lot, 100 wafers per hour throughput and overlay of roughly 3 nm in x and y. These are close to the requirements for leading edge memory devices but are far short of logic requirements. This rate of progress suggest pilot production could be tested in 2021 or 2022 for memory applications.

While we know of no current program to design and make direct-write (maskless) e-beam tools suitable (in place of optical exposure tools) for mass production of IC chips, MultiBeam Corporation has several US government contracts to build a Multicolumn Electron Beam Lithography (MEBL) tool. This maskless printing capability is complementary to conventional optical printing, with applications in the following areas: patterning full-wafers for low volume or fast design cycles; embedding unique security information into a chip during wafer processing; and patterning wafers with low feature counts of 1D line cuts or via holes to enable reasonable wafer throughput. The initial resolution target for printing capability is sub-100 nm with a multi-column design.

Another maskless tool has just been announced by EV Group, based on clustered UV optical laser write heads with multiple-wavelength exposure optics and sub-2 μm resolution capability. The primary applications include 3D chip packaging technology and MEMS devices. This is another example of migration from conventional to smart and agile digital lithography processing.

Directed self-assembly (DSA) defines edges through a different mechanism than photoresist and thus has the potential to reduce noise in imaging. Defects from failed pattern formation are the issue with DSA, not stochastic defects. It can be used either to improve the quality of patterns such as hole patterns or to multiply pitches. Some years ago, it was tested for memory pitch multiplication but did not perform as well as multiple patterning. Less work on DSA was reported thereafter. But recently new work with DSA has been reported showing both the capability for rectifying defects in EUV patterns and the ability to accommodate multiple pitches and CDs in doing so. This suggests that DSA processes may have a place in process flows for future logic nodes.

6. SUMMARY AND KEY POINTS

DRAMs and logic are both driving higher resolution patterning, with logic devices slightly ahead of DRAMs in their critical dimension roadmap. EUV has been implemented for leading edge logic devices and will likely be used for DRAM production in the near future. The biggest challenges for EUV will be related to stochastics, defects and overlay. Stochastics and defects will force manufacturers to adopt slower resists as critical dimensions get smaller. Higher power EUV light sources and/or novel resist materials will be necessary to maintain economic throughput with decreasing CDs. Flash memory innovation has switched to 3D structures and is looking for lower cost patterning rather than higher resolution patterning. The leading candidate for novel 3D flash patterning is nanoimprint. EUV is now successfully implemented in logic device production. The roadmap shows continued resolution improvements through 2028. But after that, logic devices will switch to 3D architectures and DRAM minimum dimensions will shrink slowly. Long term patterning challenges will be related to etch, deposition yield and topography rather than minimum resolution.

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[1] H. J. Levinson, "The potential of EUV lithography." In *35th European Mask and Lithography Conference (EMLC 2019)*, Proc. SPIE **11177**, p. 1117702, 2019.

[2] Bernd Geh, "*EUVL: The natural evolution of optical microlithography*," Proc. SPIE Vol. **10957**, p. 1095705 (2019) https://doi.org/10.1117/12.2515791