INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

2016 EDITION

YIELD ENHANCEMENT WHITE PAPER

YIELD ENHANCEMENT

1. MISSION

The mission of the group is to provide a collaboration platform for industry experts to focus on nano-defectivity control for next generation of advanced semiconductor manufacturing technology

Yield Enhancement focus area is dedicated to ensure that semiconductor manufacturing set up is optimized towards identifying, reducing and avoiding yield relevant defects and contamination.

Yield in most industries has been defined as the number of products made divided by the number of products that can be potentially made. In the semiconductor industry, yield is represented by the functionality and reliability of integrated circuits produced on the wafer surfaces. During the manufacturing of integrated circuits yield loss is caused for example by defects, faults, process variations, and design. The relationship of defects and yield, and an appropriate yield to defect correlation, is critical for yield enhancement.

The Yield Enhancement (YE) section will display the current advanced and next generation future requirements for high yielding manufacturing of More Moore as well as More than Moore products separated in “critical process groups" including MEMS, back-end processes, e. g. packaging. Consequently, an inclusion of material specifications for Si, SiC, GaN etc. will be considered.

In the manufacture of integrated circuits yield loss is related to a variety of sources. During processes such as implantation, etching, deposition, planarization, cleaning, lithography, etc.., failures responsible for yield loss occur. Several examples of contamination and mechanisms responsible for yield loss are listed in the following: a) airborne molecular contamination (AMC); (b) airborne particular contamination (APC) of organic or inorganic matter caused by the environment, personnel or by the tools; c) process induced defects as scratches, cracks, and particles, overlay faults, and stress; d) process variations resulting, *e.g.*, in differing doping profiles or layer thicknesses; e) the deviation from design, due to pattern transfer from the mask to the wafer, results in deviations and variations of layout and critical dimensions; and f) diffusion of atoms through layers and in the semiconductor bulk material.

The determination of defects and yield, and an appropriate yield to defect correlation are essential for yield enhancement. This correlation is of major importance, because not all defects change device properties or cause failure of devices or integrated circuits. Therefore, the yield enhancement chapter addresses not only the identification of tolerable contamination limits for processes and media, but also the tolerable budgets for particulate contamination of tools. The specification of tools for defect detection and classification of defect for root cause analysis addresses the technology requirements for More Moore and More than Moore.

The YE section has two focus topics: “Surface Environment Contamination Control” (SECC) and “Characterization, Inspection and Analysis (CIA)”. These two topics crosscut front end process technology, interconnect processes, lithography, metrology, design, process integration, test, and facility infrastructures.”

Charter:

Enabling Yield improvement through defect reduction in high volume semiconductor manufacturing facilities via:

- Conducting ongoing risk analysis of the high purity materials, parts, utilities and environments involved in advanced semiconductor manufacturing.

- Proposing potential solutions and risk mitigations associated with technology gaps that limit measurement and control of environmental wafer, mask, or substrate contamination.

- Initiating and conducting collaborative experimental studies and models to better define and quantify exposure of environmental contamination to wafer surfaces. Communicate results of the risks and their mitigation strategies to the industry in the form of the International Roadmap for Devices and Systems (IRDS) published roadmaps, conference presentations, and technical journal presentations.

- Initiating SEMI standard development activities to address the risks;.

- Supporting new technology trials through benchmarking studies.

Physical device dimensions and corresponding defect dimensions continue shrinking, posing new challenges to detection as well as tolerable contamination. The wafer edges and backside were identified to show significant impact on yield as well as process variations and design. Additional new challenges arise specifically for MEMS manufacturing as well as assembly lines through the use of new material. Development of defect detection, defect review, and classification technologies showing highest sensitivity at high throughput solving those challenges is crucial for cost efficient manufacturing. Furthermore for efficient manufacturing the monitoring of contamination in the environment and on the wafer surface requires appropriate analytic capabilities. Automated, intelligent analysis and reduction algorithms, which correlate facility, design, process, electrical and virtual metrology results and their correlation to yield, test and work-in-progress data, will have to be developed to enhance root cause analysis and therefore enable rapid yield learning.

3. SCOPE

The scope of the Characterization, Inspection and Analysis (CIA) is to continue the defect detection and review roadmap to meet the More Moore requirements in close cooperation with the More Moore and Metrology team. Focus on describing new challenges coming out of MEMS, Assembly and the use of new materials. Therefore a new MEMS related CIA subgroup is built.

The following diagram (see Figure 1) illustrates the scope of the SECC formerly the ITRS's Wafer Environment Contamination Control (WECC). The scope is limited to the consideration of the next two generations of the most advanced semiconductor manufacturing technologies, as defined by the production node size. The scope is focused on critical surfaces of the manufacturing process, including but not limited to wafers, lithography reticles, and lithography lenses. The arrows on the diagram illustrate two typical sources of the contamination: the environments of the critical surface processing (water, chemicals, and gases) and the critical system components that may shed or outgas contamination into the environment and through it to the critical surface. It is also possible that the critical surface can contribute to the contamination to the environment and subsequently contaminate the surface.

The effort is intended to define quality parameters and allowable levels that will ensure proper contamination control at the critical surfaces to reduce defects and improve yield for cost effective semiconductor manufacturing.

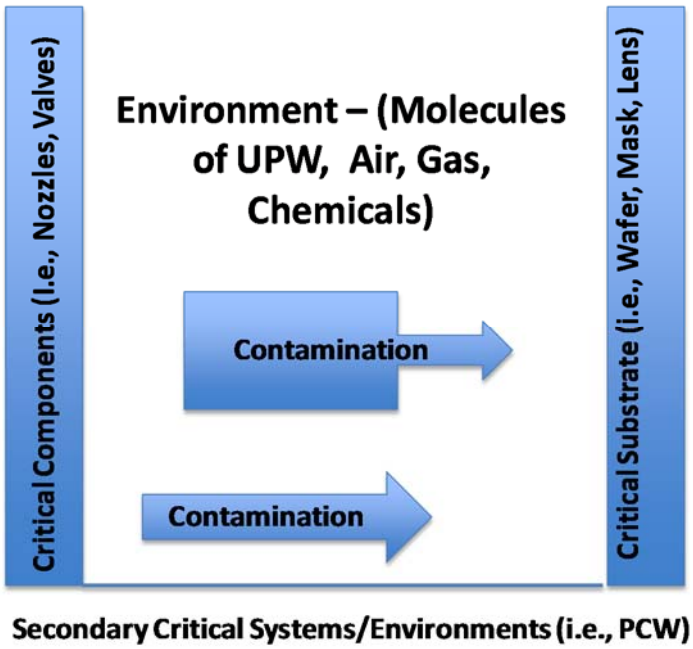

Figure 1. Scope of SECC

These parameters include impurities associated with chemistries in the critical surface environments, such as ultrapure water (UPW), liquid chemicals, gasses, thin film materials (precursors), AMC, and critical parts of the manufacturing tools used in vicinity of the critical surfaces. Typical quality parameters include the following:

- Concentration (number and size) of critical particles
- Organic compounds
- Ionic species
- Metals
- Silica (Coloidal and dissolved)
- Non-volatile residue
- Static charging

4. Cross Team Interactions

4.1 Cross team interactions within IRDS

As the Yield enhancement chapter focus is dedicated to ensure enhanced semiconductor manufacturing Yeild, establishing close interaction with various other teams is crucial:

Yield Enhancement group is expected to work with More Moore to define defectivity characteristics and required detection tool requirements. Metrology as characterization challenges will need to be addressed by Metrology and Yield enhancement together.

Factory integration as the requirements for data analysis and yield correlation are defined in that chapter, the input for yield enhancement needs to be defined by the Yield enhancement chapter. Assembly and packaging as yield becomes more and more important for them and the most effective methods need to be defined together.

Additionally with front end process technology, interconnect processes, process integration and test.

4.2 CROSS TEAM INTERACTIONS WITHIN SECC

Figure 2 illustrates the cross-functional team collaboration of SECC including interface with industry organizations such as SEMI that provide resources such as industry standards and guidelines helping to ensure quality throughout the supply chain.

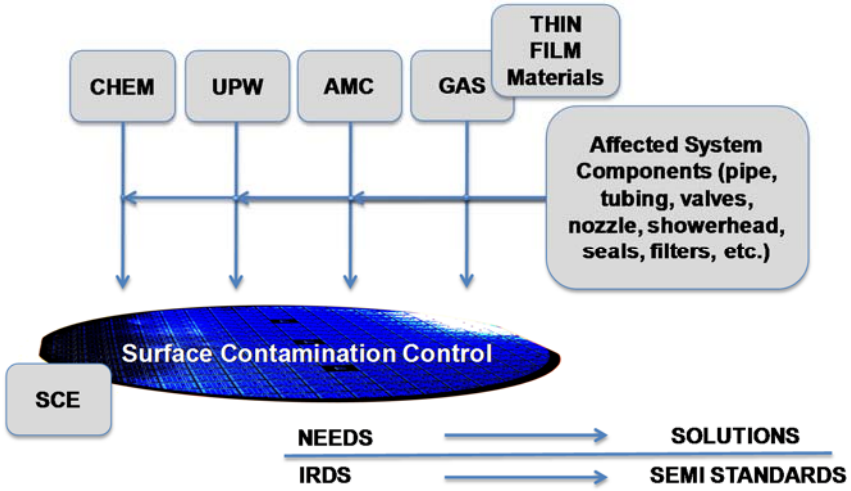

Figure 2. SECC cross team interactions

The cross-functional team collaboration is performed on an annual cycle with predefined deliverables as illustrated in Figure 3. According to this process the following cross team interactions take places during a one-year cycle:

Step 1: Surface Contamination Experts (SCE) provide their direction to environmental groups on the maximum level of contamination allowed on the critical surface to enable yield improvement of the next generation of the technology (critical surface environment implies UPW, Chemicals, AMC, and Gases). This takes into account the Yield targets and complexity of the manufacturing process.

Step 2: UPW, Chemicals, Gases, and AMC teams conduct experimental and theoretical analysis to define maximum projected level of impurities in the respective environments that would improve manufacturing yield. This step takes into consideration, the interactions between different environments, such as UPW rinse following chemical etch or processing wafers with exposure to simultaneous environmental process molecules (liquid/gas interfaces).

Step 3: Once quality targets are defined, each group identifies difficult challenges associated with reaching those targets. When challenges are defined, the groups search for potential solutions and risk mitigation steps to address those challenges. Each of the cross-functional teams utilizes the targets defined by SCE and data produced in the experimental analysis or theoretical models to define means to measure quantify and control contamination and improve yield. At this point, the targets, challenges, and the potential solutions are published as part of an IRDS roadmap. The technical experts involved in the roadmap development also publish the roadmap information via professional conferences and technical publications to better describe the details and results of the development work to the industry stake holders and supply chain.

Step 4: The IRDS roadmap information is used by the respective technology suppliers to focus their development activities and commercialize products to be used to address the industry needs. The groups participate in demonstration studies, when appropriate. This helps with both generating new data and helping suppliers to introduce new solutions to the market.

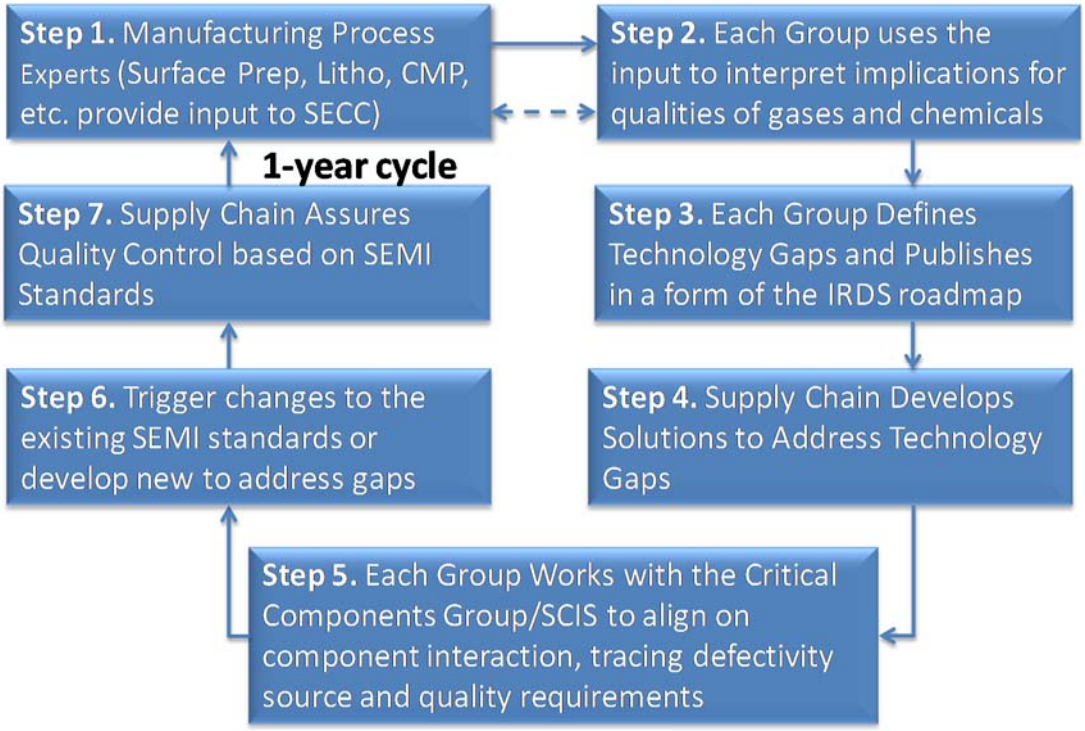

Figure 3. SECC Cross Team Interaction Process

Step 5. In addition to the development of new metrology and purification technologies, the groups collaborate with the material and critical components suppliers to define new materials quality and quality control requirements. This is commonly done via initiation of the SEMI standards updates or the development of new SEMI standards as needed. Currently SECC considers forming a new group of experts that would provide additional focus on the critical components and their effect to the critical surfaces.

Step 6. Members of the IRDS SECC groups help to facilitate new activities and develop SEMI documents.

Step 7. SEMI documents are approved and published. Industry adopts the document to ensure tight quality control throughout the supply chain.

The process illustrated in Figure3 is conducted on an annual cycle. Though all 7 steps are repeated on an annual basis, the goal is to support the cycle of new technology development, which typically occurs on a bi-annual basis. Key SEMI documents are expected to be reviewed bi-annually.

5. CUSTOMERS AND STAKEHOLDERS

The customers for this developmentIn general the major Customers and Stakeholders are

- IC manufacturing companies (from MEMS to Advanced SemiconductorIntegrated Circuit Manufacturing Companies and)
- Universities and other research institutions
- Major semiconductor manufacturing OEM tool vendors.
  - Analytical experts and metrology companies

- Facility vendors, material suppliers, consultants
- FEP and Litho experts, defining target levels

The main stakeholders involved in the SECC process are as follows:

1. IRDS sub teams, providing information on the manufacturing technology needs influencing Yield requirements.
2. SEMI, providing collaboration platform for standards development. SCIS (Semiconductor Components, Instruments, and Subsystems) is SEMI Special Interest Group, focusing on quality of the critical components. SCIS utilizes information generated by SECC to trigger or influence new or existing SEMI Standards. Figure 4 illustrates the focus of SCIS and the way SECC and SCIS interface at the wafer level.

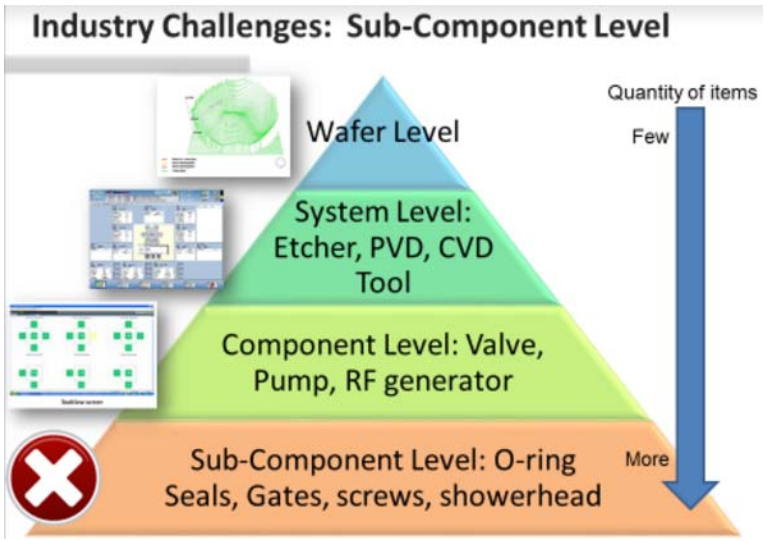

Figure 4. SCIS Focus on Process Equipment

3. Professional Conferences'Organizers in the respective technology areas, providing opportunity for the technology needs communication with the industry technology providers and end users.

6. TECHNOLOGY STATUS, NEW REQUIREMENTS AND POTENTIAL SOLUTIONS

6.1. TECHNOLOGY STATUS AND UPDATE

Yield Management for MEMS – Mems technology holds specific challenges for inspection and characterization based on structures at backside, capwafers and a need of inspection and characteriaztion of covered defects. The different MEMS technologies need to be separated in surface and bulk technologies for it causes different requirements to inspection and characterization.

Yield correlation/Data Mining – in the future the need for prediction will become even more important and the use of semi and unstructured data sources and unsupervised data mining will become necessary. Nonetheless a high level of process know how will still be required.

Electrical characterization methods and Virtual Metrology for Yield Control - In order to overcome the problems of low sensitivity and high effort of metrology for yield control, one focus of the YE group will be the partial replacement of physical based metrology with electrical diagnosis and virtual metrology wherever feasible. The use

of all available data sources and approaches for data analysis will be further elaborated for yield monitoring. Hereby, a better balance of defect/contamination detection and fault diagnostics/control of electrical characteristics should be established by including statistical and systematic approaches into YE activities. Furthermore, virtual metrology becomes more and more essential for yield considerations. Virtual metrology is defined as the prediction of post process metrology variables (either measurable or non-measurable) using process and wafer state information that could include upstream metrology and/or sensor data. Refer to Yield Enhancement Chapter for more information.

Wafer Defect Metrology - Defect metrology continues to be important towards smaller nodes, especially considering new yield challenges like multiple patterning. The main way to detect yield impacting defects in production is defect inspection. Therefore, the requirements are defined together with the *More Moore chapter.*

For Heterogenous Integration, 3D integration is the challenge. Finding the right solutions for those inspection requirements will be the focus for future roadmap development.

Yield management for packaging and assembly - As technology requirements in the assembly and packaging area increases, yield loss and therefore yield improvement methodologies become essential. Yet the most appropriate methodologies have to be selected and Front End (FE) yield tools need to be adapted to Back End (BE) requirements. The task will be to define a dedicated roadmap.

Critical surface environment control—environment control includes the ambient space around the wafer at all times, whether the wafers are open to the cleanroom air or stored in front opening unified pods (FOUPs). As the list of ambient contaminants to be controlled broadens, so must measurement capabilities. Affordable, accurate, repeatable, high capture rate, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport, store and even process wafers is expected to increase with process sensitivities. Pre-gate, pre-contact clean, salicidation, exposed copper, and reticle exposure are cited as processes that first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. Drier environments can contribute to static charging, so this needs to be considered. While closed carrier purging systems currently exist and wet processing tool environments are evolving into enclosed, low-O_2 single wafer processing chambers may need to become inert, such as needed wet sink end-stations, present a challenge. The safety when using inert purges must be carefully considered, including during maintenance. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low-outgassing, and non-absorbing material development are key to an effective wafer and reticle isolation deployment.

There are three primary sources of process environment contamination: One is the impurities in the process materials as supplied. The second is the delivery system or the process itself. The third is reaction, such as contaminant- or thermally induced decomposition, by process such as RIE (reactive ion etch) contamination of FOUPs. These contamination sources are found throughout the pathway from the delivered gas or chemical to the substrate surface.These contamination sources are found throughout the pathway from the delivered gas or chemical to the wafer surface.

6.1.1. ULTRAPURE WATER

UPW is purified water with most of the quality parameters below or near their detection limits of the most advanced metrology. Current state of UPW technology generally can provide effective control of contamination. However whereas some parameter are relatively easy to control, effect of others require further investigation.

Particle levels are reduced using the best available ultra-filtration (UF) technology, but today's particle detection and counting technology is not able to keep up with critical particle node due to continued scaling of critical semiconductor devices. Monitoring available for particles is limitated to laser particle counters capable of monitoring 20nm particles with limited counting efficiency. There are new measurement devices for smaller particle sizes under development and commercialization, but their capabilities have not been demonstrated yet.

Lack of proven particle metrology limits the ability to confirm whether UF is effective in controlling critical ("killer") size particles down to the critical particle size. At the same time, it is apparent that the killer size of the particles has approached filtration capability of the most advanced final filters, and while there is test data suggesting the particle challenge concentrations in the feed to the final filters from UPW system components can be very high. Current definition of the killer size of the particles is based on half-pitch DRAM and has already approach 10nm dimension. However, 3-D structure of new semiconductor devices may require revisiting approach to the definition of the critical particle size.

Silica is one of more complex impurities in UPW. Silica may occur in UPW in a form of reactive (dissolved) or colloidal silica. The main concern around colloidal silica is due to the fact that its occurrence in UPW is highly probable, its retention by final filters is more difficult than other particles, and also because it may adsorb metal ions, thus becoming more detrimental on the wafer (these effects are based on published data).

While it is easy to control reactive silica, colloidal silica is difficult to monitor at the level where it presents a problem. Traditionally colloidal silica has been measured as the delta between total and reactive silica in UPW. The killer particle size of currently considered generations became so small, making it impracticle to expect that the colloidal silica particles in critical concentration (posing risk to critical surface) could be measured as the delta of total and reactive silica (very small particles do not contain sufficient measureable amount of the silica compound). Since colloidal silica cannot be effectively monitored using state-of-the-art metrology neither as particle nor as the compound, further investigation of the colloidal silica occurrence is necessary for its effective control (focus on preventing occurrence and mitigating risks). .

Hydrogen peroxide has been recently reported to occur in final UPW as a by-product of UV (ultraviolet) reactors used to decompose UPW organics. There is technology available for removal of hydrogen peroxide in UPW. However its implementation requires major change and investment. Hence, the effect of hydrogen peroxide to critical surfaces needs to be better understood to allow for implementation of the effective solutions. Hydrogen peroxide monitoring methods have not been fully commercialized and standardized.

The UPW team is currently reviewing the need to define tighter target levels for **metals** for image sensors. At the considered levels, on-line monitoring of the metals is impossible using existing state-of-the-art metrology. Although metals monitoring requires more complex off-line lab tools, ability to control metals in UPW by state-of-the-art treatment technology has been generally demonstrated. The UPW team is currently focused on the investigation of the effect of high purity materials onto metal contamination during the critical time of initial system commissioning and factory ramp.

Organic contamination is currently measured in terms of its total organic carbon content or TOC. This measurement of the organic content does not account for the type of organic and how it may react with various wafer surfaces or how the reaction may impact device yield. While for most applications organic compounds in UPW are categorized as critical and non-critical based on their boiling point, immersion lithography lens hazing is driven by total organic carbon (TOC). Although controlling organics at the target levels is difficult, both treatment and on-line monitoring solutions are available.

Note: It is important to keep in mind that the SECC roadmap is focused on technology enabling, identifying the parameters that require new technologies for monitoring and control. For the practical purposes, SEMI F063 provides a guide that can be used as a reference specification for the UPW quality in design and operation of advanced semiconductor processes, considering feasibility of the existing technologies. The UPW team collaborates closely with the SEMI UPW Task Force to develop guides and test methods to mitigate existing risks and challenges.

6.1.2. AIRBORNE MOLECULAR CONTAMINATION (AMC)

Outgassing from materials of construction in the cleanroom, wafer processing equipment, post processed wafers, wafer pods, and wafer environmental enclosures, as well as inadequate exhaust and fugitive emissions from chemicals used in wafer processing and the presence of humans in these environments are the main sources of AMC. Makeup air is also a significant source for AMC.

Oxygen and water vapor as well as atmospheric contaminants (e.g., CO, O_3, SO_2, NH_3) can also be considered as part of the AMC burden. Acid vapors in the air have been linked to corrosion. The impact of amines on deep ultraviolet (DUV) photoresists is a well known example of AMC affecting wafer processing. Hydrocarbon films of only a few monolayers may lead to loss of process control, delamination of coatings and bumps, and may impact any nano-scale metrology readings. The impact of AMC on wafer processing can only be expected to become more deleterious. This is not only driven by device dimensions decreasing but also by the introduction of new chemistry and recipes for future technical nodes that exhibit new defect schemes.

Besides AMC creating defects to the wafer surface or bulk material yield enhancement engages on defects or shortfalls in productivity that originate from the impact of AMC to production tools such as reticles, metrology, corona ionizers, or exposure tools. AMC is in many cases a highly dynamic phenomenon, particularly in confined environments such as FOUPs and PODs, where critical surface chemistry interacts with the environment surfaces. It should be noted that there is not a certain critical level of contamination for each AMC. This is always seen in connection with the contact time of AMC and the materials. Ultimately a dose (concentration x time) of the AMC is to be considered.

AMC control deals with prevention of AMC release for which a tight source control is mandatory as well as mitigation and continuous removal through air recirculation. There is clearly a need for better AMC monitoring instrumentation in the clean room to measure AMC at the part per trillion level (by volume) in real time. Ion Mobility spectrometry techniques (IMS), Cavity Ring-down spectroscopy (CRDS), FTIR, UV chemiluminiscence instruments and various atmospheric pressure ionized mass spectroscopy (APIMS) have been used to measure low level AMC, but the former is too unspecific, the latter too involved. A larger variety of online methods and instrumentation is still needed, but current technology appears to perpetually lag behind technology needs., The main challenge is to combine high sensitivity with high specificity at manageable cost, maintenance and automated operation.. See also the link for *AMC monitoring programs.*

Humidity is extremely important in reticle environments and may be very important in wafer environs.

Clean room ambient conditions are regarded at Point of Entry (POE) to critical process steps that may involve further tool related measures of AMC protection and reduction, yet require controlled entry conditions to achieve proper process control. FOUP and reticle Pod interior limits are not only influenced by clean room environmental contamination but are depending heavily on remaining active material outgassing or re-evaporation of AMC attached to the containment walls, wafer surface or backside and edge of wafers.

The FOUP itself may be a source of contamination because of materials outgassing and also because it can trap AMC coming from contaminated wafers which will then be further outgassed. The defects due to AMC might be a result of a combination of critical contamination inside the FOUP, type of substrate and storage time. Some defects are also linked to humidity and temperature conditions. As a result, the measurement and control of the contamination inside FOUPs are key challenges for IDMs and foundries.

Static charging can lead to electrostatic attraction of particles to surface, and higher nanoparticle contamination, and also contribute to ESD defects"

"Thus, ionizers of various types are sometimes used to neutralize charge. Corona ionizers can interact with excess AMC of some types to create nanoparticles, or buildups on tips to hundreds of microns, that can shed then large particles, or lead to ionizer imbalances or long surface charge decay times. AMC's must be controlled for these ionizers to work optimally. Ionizer tip deposits can be analyzed to assess what elements of AMC are leading to deposits. Similar compounds in air might similarly affect energetic processes like DUV optics, masks, scanner, esp for 193nm, high voltage or high temperature surfaces"

Witness wafers have been used to link surface molecular contaminant (SMC) concentrations to specific defects. The surface concentrations are usually expressed in a maximum allowable number of molecules/cm^2, ions/cm^2, or atoms/cm^2 for elements or ng/cm^2 for organics. Airborne moilecular contamination can transform into SMC through reaction, SMC can become AMC through evaporation or sublimation, another dynamic aspect of chemical contamination, regardless of environment.

Corona ionizers can be used to control static charging, electrostatic particle attraction, but corona ionizers can react with some volatile AMCs for form non-volatile deposits that affect ionizer decay times and balance, and can shed um to nm sized particles if AMC not well controlled. If deposits form on ionizers, these added residues can be analyzed by SEM-EDS to assess what volatile compounds with elements in air are being deposited by reactions at the ionizer tip including with heat, UV, ozone, electrons, ions. For example, silicones or trimethylsilanol can form SiO_2 deposits on corona ionizer tips, and ammonia can form ammonium nitrate.

6.1.3 GASES, LIQUID CHEMICALS, AND PRECURSORS

The targeted purity levels can be reached either by bulk delivery of a fluid with required purity or through use of local purification/filtration step. Care should be taken, at a minimum, to maintain the quality of the gas and chemicals coming from the source, ensuring that contamination is not added downstream, as may occur due to particle generation at components (such as valve switching), moisture out-outgassing, byproduct generation due to incompatible materials, etc. Particle filtration as close to the POU (point of use) (POU) or chamber entrance as possible is generally advisable for gases. For the most critical applications a local purifier may be used to enhance or ensure ultimate purity at the POU. In those cases, the prevailing approach is to seek levels that are adequate for the process and to view the purifier as "insurance." The challenge to the purifier is minimal, and long purifier lifetimes can normally be expected.

An important exception to this guidance is for some specialty materials that undergo a variation in composition as they are distilled from the cylinder or other delivery vessel in a bulk vapor delivery set up. For example, anhydrous HCl, , is known to form very stable hydrates with water that result in changes in the concentration in the water content in the cylinder and gas phase as the original specified contents are removed. In this case, a combination of rigid specifications on how much of the contents can be used before moisture becomes unacceptable requiring application of moisture removal devices is needed in the vapor transport path. Liquid anhydrous ammonia is another specialty gas with this potential issue. Within the realm of relatively volatile liquids that are delivered in bulk, i.e., not by direct liquid injection, volatilization, aqueous hydrogen peroxide, aqueous ammonia and likely many of the amine-amide based CVD/ALD precursors, are expected to undergo similar distillative variation and/or thermal degradation under delivery conditions. Depending upon the process sensitivity this might be a source of poor film quality or process variability that can be addressed by attention to the delivery method. Reactivity of transport surfaces, as well as outgassing need to be considered, as well.

Point of use purifiers and filtration units are finding application in newer atomic layer deposition techniques (ALD), for example, where the films are deposited as monolayer and incorporated impurities can be especially destructive. Purifiers must not add any new contaminants. A near/medium term challenge is filtration of the precursor vapor. The sources can be sublimable solids or readily condensable vapors of low volatility liquids. These can resolidify or reliquify causing plugging and instability in fluid transfer to the substrate surface.

6.1.3.1 BULK AND SPECIALTY GASES

increased levels of purity requirements are expected in advanced processes. This type of improvement might be anticipated, based upon historical trends as design rules tightened, but there is again little objective evidence to support the need for improvements across the range of bulk gases. For very special applications where extraordinarily higher purities are critical, special purity grades or additional purification will be required.

The situation is similar for many of the Specialty Gases. Statistical Process Control (SPC) for process gases and liquids was implemented by large semiconductor manufacturer for a selection of critical process fluids, e.g., TEOS. Rather than simply meeting specification values for a set of quality control parameters, the materials were selected against specifications dictated by statistical control of variability of the materials. The utilization of SPC selection criteria continues and has expanded, but there are still no standards accepted across the industry that define the SPC process.

The promise of providing "in control" process fluids is anticipated to improve process yields by either minimizing the overall variability of the manufacturing process or in simply reducing the likelihood of a process crash resulting from large variations in material quality that would still nominally have met a more standard specification.

For some processes, such as advanced lithography (especially 193 nm), very small quantities of "high molecular weight/high boiling point" (*e.g.*, C_6-C_{30}) hydrocarbons in supply gases are detrimental because of increased adherence to the exposed surfaces, and potential for photochemical degradation to leave non-volatile residues on lenses, masks, mirrors, etc. However, any organics, even ones with retention times less than C_6 are considered detrimental if they can result in refractory deposits. For the same reason, other potential impurities such as siloxanes or organophosphates can also be very detrimental in extremely small quantities. In order to detect such species with sufficient sensitivity, it is necessary to directly detect the relevant species and calibrate the analyzer with the appropriate standard near the quantitation limit. The methods used are analogous to those for AMC, such as thermal desorption (TD) gas chromatography (GC), mass spectrometry (MS) or TD GC with flame ionization detector (FID), photo ionization detector (PID), or ion mobility spectrometry (IMS). Even these approaches may miss some heavier hydrocarbons and/or polar species that tend to remain in the column or emerge as very broad peaks, if not optimized. For methods using adsorbent traps, it is very important to determine the trap efficiency. Using APIMS to provide real time measurement of individual hydrocarbons is possible, in principle, but very involved and calibration is difficult, because larger hydrocarbons may be collisionally dissociated in the ionization process.

A compromise approach that has gained some acceptance is to use TD GC/MS and sum all peaks corresponding to C_6 and higher. The instrument is usually calibrated with a multi-component standard and results are reported as "toluene" or "hexadecane" for wafers or as toluene for CDA or gases. While the quantization provided by this method is approximate, and some species may be overlooked, it does at least provide a metric for contamination level and a straightforward calibration.

Historically, applications for both O_2 and H_2 generally tolerate higher levels of N_2 contamination than other contaminants; however, H_2 as a carrier for Epitaxy now requires more stringent N_2 levels and the table reflects this observation. Requirements for critical clean dry air (CDA), lithography purge gases, and supercritical CO_2 supply are included. Whereas critical CDA may not always be conveniently or cheaply available, there is no technological barrier to its production. Analytical methods are usually the same as used for airborne molecular contamination in clean room air, such as bubbling through ultra pure water (for metals, acids, amines, etc.) or trapping on an adsorbent trap for organics. In each case, the sampler concentrates impurities so that requisite sensitivities are achieved when the sample is introduced to the analyzer (ICP-MS or ion chromatography for aqueous samples, GC-MS for desorption of organics). Such methods are time consuming by nature, and direct methods would be preferred if available. However, there is no apparent pressing need for real-time analysis. For SO_2 there are convenient on line methods, *e.g.*, UV fluorescence.

For specialty gases, contaminant values in etchants, dopants, and deposition gases have been expanded in Table YE3 to reflect the increase number of different materials in use, and to better delineate the processes in which they are used. Particulate contamination is omitted, since online monitoring of particle concentrations is not commonly practiced and the efficacy of POU particle filters is well established. Whereas there is evidence that the most demanding applications, such as low temperature epi and its cleaning gases, will continue to benefit from improvements in purity as deposition temperatures are lowered, this is expected to be reflected in wider use of the best available purity rather than substantial improvements of those levels.

Tighter control over the variation in purity in both bulk and specialty gases is more important than improvement in absolute purity levels. However, the often more chemically reactive specialty gases present a more formidable challenge for maintaining of POS (point of supply) purity levels throughout the delivery to the point of process. Selected specialty gases, *e.g.*, HCl are now commonly under statistical process control at the POS.

Novel materials— More detailed consideration of the impurity levels found in the growing number of novel materials used in processing will be increasingly important. Requisite purity levels for critical materials such as novel metal oxides, chemical mechanical planarization (CMP) slurries, low/high k dielectric materials, precursor materials (such as chemical vapor deposition (CVD), atomic layer deposition (ALD), and electroplating solutions) for barrier and conductor metals (such as Cu, Ta) have not been widely studied, and many of these materials have not been called out in Table YE3. An early attempt to start to catalogue and characterize the properties of the thin film precursors utilized in semiconductor processing is found in the supplementary material for this chapter.

Deposition precursors for thin film materials are often sensitive to moisture, air and high temperatures. Control over the delivery process from the POS to the reaction chamber is critical to high yielding performance. The use of very high purity carrier and purge gases in these systems isare often required to prevent decomposition that can contribute detrimental molecular and particulate impurities. Traditionally bulk purifiers were used in the bulk gas delivery systems to remove particles and other homogeneous chemical contaminations like oxygen, or moisture present in the supply gases. However, with the development and commercial availability of point-of-use (POU) purifiers, there is a strong interest from end users to utilize POU purifiers particularly for specialty gases needed for critical process steps with very critical level of contamination control. These point-of-use purifiers POU are highly effective to remove chemical contaminants to extreme low level (~ ppt), easy to use, easy to replace, with low cost-of-ownership. The capability of placing those POU purifiers very close to inlet of process chamber, assures least travel path (less contamination) for process gases after chemical purification and filtration.

6.1.3.2 LIQUID CHEMICALS

Pre-diffusion cleaning and extreme ultraviolet (EUV) mask blank cleaning requirements drive the most aggressive impurity levels. Liquid particle level requirements are expected to become tighter each technology generation. These target values are derived from the purity requirements on a wafer as calculated by the surface preparation experts assuming a linear relationship between the concentration in the liquid and on the wafer. Particle counters are currently only capable of measuring down to 30-40 nanometers (nm for) in liquid chemicals. By assuming a particle size distribution, it should be possible to infer particle concentrations to smaller particle sizes, but this will be influenced by the level of filtration utilized. Another measurement challenge for several chemicals is the differentiation between particles and bubbles, which is currently not possible, although solutions can be degassed and/or pressurized to dissolve gases.

The ability to accurately analyze organic, anion, and cation contamination in process chemicals is becoming more critical to successful wafer processing. In the supplementary links an ion table and a mixing calculation are provided that show which chemicals with which ions are important and in which chemicals they could actually occur/have been observed. With the increased use of CMP and plating chemicals, there must be a better understanding of purity requirements for the delivered chemicals.

The performance characteristics of many of the processes chemicals that are used for etching, plating, CMP and cleaning depend heavily on the amount and type of foreign material present as well as the consistency from batch to batch that is used in the process. The integrated effects of variability in the performance of these chemistries will play a significant role in the defect control within the manufacturing process. The process flow is designed based on the premise that each process stop is stable and repeatable. Any deviations from these integrated design parameters will most likely have adverse effects of other process steps in the process flow which includes wafer defect impacts.

The ability to detect, control and protect the process from adverse defect conditions relies on both the sensitivity of liquid defect metrology to detect the critical size of particle but also in the ability for the various metrologies to have the same or similar response to a change in the population and size distribution of these particles. Too often particle distribution baseline shifts occur at the end user's detection point with no signal observed at the chemical source location. By the time the chemical distribution system has detected this change, it is too late to protect the manufacturing process from the impacts of this increased defect level. Furthermore, many defect elevations occur in the wafer process with no detectable shift in any of the online liquid particle counting systems due to a mismatch in the sensitivity of the liquid particle counting metrology and the wafer defect sensitivity.

6.1.3.3 ALD/CVD PRECURSORS

At recent nodes ALD processes have been adopted aggressively and that proliferation is expected to accelerate in the future. ALD processes will therefore constitute a growing subset of the processes used in HVMhigh volume manufacturing (HVM) and some discussion of common/unique aspects of ALD processes with respect to SECC is warranted.

For the vast majority of semiconductor processes, gaseous reactants are delivered to the processing chamber at atmospheric or superatmospheric pressures. However, for most ALD processes, the precursor is delivered at pressures typically in the range of 5 Torr to 100 Torr to the reactor, which is processing typically less than 1 Torr. To minimize

precursor deposition/condensation within a delivery system, the equipment is typically heated to 100°C or greater. At such conditions, the gas flow through many of the delivery system sub-components is in the slip flow regime. In the slip flow regime, there is a non-zero boundary velocity at solid surfaces and a thinner boundary layer. This significantly alters both the fluid dynamics and heat transfer properties of the system. Additionally, ALD precursors can readily form particles in the precursor delivery system through both condensation and reaction with residual oxygen-containing species. With solid precursor sources, there is an added risk that source material particulate can be entrained by the carrier gas.

Furthermore, metallic impurities in inorganic, metalorganic, organometallic or organometalloid precursors are typically orders of magnitude higher in concentration than in most non-metal containing gas streams and can be a source of metallic contamination in the resulting films. In addition, thermal decomposition of precursors on the wafer or in the gas phase can produce particles, or provide another source of in-film contamination. OEMs and precursor suppliers should keep these complexities in mind when designing or modifying precursor delivery sub-components and systems. Semiconductor manufacturers should consult with their suppliers if they are interested in re-engineering or adapting their precursor delivery systems since changing the pressure drop or flow dynamics of a vapor delivery system for a sensitive precursor may have unintended negative consequences.

Due to the low vapor pressure of many ALD precursors, the process canisters are usually kept at elevated temperature (>90°C) at the point of use in the tool gas box. Many ALD precursors will have a slow rate of decomposition at these temperatures and extra care should be taken to adjust the size of the on-board source canister to consume the source before process deteriorating decomposition starts. In many cases smaller heated onboard source canister that is refilled by a bulk deliver system or a liquid injection system without tank are preferred solutions.

When supplying the precursor from a bulk delivery system in the sub fab, extra care should be taken to avoid release of bubbles from the push gas into the liquid precursor. The bubbles are released due to the pressure drop going from the point of push gas insertion (sub fab) up to the tool. These bubbles will typically disturb the liquid flow controllers in the tool gas box or direct liquid injection systems resulting in a disturbed fluctuating delivery flow of precursor into the reaction chamber and possible particle generation in the injection system if the injection is over flown with precursor above it is optimal working conditions.

Downstream of the ALD reactor, the relatively low vapor pressure ALD precursors and process by-products tend to condensate at the first point of temperature drop. Therefore, the pump stack and pressure control should be heated above the condensation temperature and all the way to preferably a cold trap that condensate the precursor in a controlled manner to avoid back streaming particles into the reactor.

Finally, semiconductor manufacturers should conduct due diligence audits of any analytical methods or techniques used to screen precursor quality with the understanding that many of the possible errors made while analyzing the precursors (e.g. incomplete digestion, failing to account for sample matrix effects, etc.) can lead to results that under-report the true impurity level. Many manufacturers are adopting ship to control standards individually with their suppliers in order to minimize any precursor variation associated yield loss in their factories.

6.1.3.4 CRITICAL COMPONENTS

The roadmap for cleanliness of critical components does not currently exist. The technology related to critical components focuses on the semiconductor manufacturing process. The cleanliness requirements have not been effectively standardized. SCIS defined the need to improve definitions for the cleanliness and establish adequate standards.

6.2. NEW REQUIREMENTS & DIFFICULT CHALLENGES

Currently, the most important key challenge will be the detection of multiple killer defects and the signal-to-noise ratio. It is a challenge to detect multiple killer defects and to differentiate them simultaneously at high capture rates, low cost of ownership and high throughput. Furthermore, it is difficult to identify yield relevant defects under a vast amount of nuisance and false defects. As a challenge with second priority the requirement for 3D inspection was

identified. This necessitates for inspection tools with the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The demand for high-speed and cost-effective inspection tools remains, especially in the area of 3D inspection as the importance of 3D defect types increases. In subchapter to Characterization, Inspection and Analysis another key challenge was identified: Detection of organic contamination on surfaces – The detection and characterization of non-volatile organics on surfaces is currently not possible in the fab. There are few laboratories or fab scale instrumentation available or implemented except ToF-SIMS, and XPS

MEMS technologies have different challenges. Inspection and review tools need to be able to handle a broad range of wafer thicknesses. Infrared inspection is required as an automatic and full wafer scan option. Review options need to be able to have solely edge grip handling and an automatic focus adjustment for a considerably wafer bow.

Other topics challenging the Yield Enhancement community are prioritized as follows in the near term:

- Process Stability versus Absolute Contamination Level
- Wafer Edge, Backside and Bevel Monitoring and Contamination Control
- Development of sub 10 nm water and chemical liquid particle counter as well as tight particle control technologies (new, tighter filters with low particles sheding and minimal contribution of metal and organic species)
- Correlation Yield and Contamination Levels

Data, test structures, and methods are needed for correlating critical tool parts quality as well as process fluid contamination types and levels to yield and to determine the required control limits. The issues for this challenge are to define the relative importance of different contaminants to wafer yield, a standard test for yield/parametric effect, and a maximum process variation (control limits). The fundamental challenge is to understand the correlation between impurity concentration in key process steps and device yield, reliability, and performance. This correlation will determine whether further increases in contamination limits are truly required. The challenge increases in complexity as the range of process materials widens and selection of the most sensitive processes for study will be required for meaningful progress.

Furthermore, in the long term the following key challenges were identified:

- In-line Defect Characterization and Analysis

Monitoring and Controling hydrogen peroxide in UPW will likely become a new requirement in UPW.

6.3 POTENTIAL SOLUTION

For pattern wafer inspection the requirements the next years will be to overcome issues of detection of the defects within the nuisance signal. This is correlated to the issue to obtain high sensitivity at high throughput. Major breakthroughs are required to achieve the required throughputs at roadmap sensitivities for yield ramp and volume production. The high aspect ratio inspection is still requiring for high yield at high throughput due to the high cost of ownership of the inspection tools. This requires also a good separation of the defect signals from the noise. The introduction of advanced lithography process using high energies has a potential to initiate chemical reactions and layer modification on the surface. Therefore the detection of volatile and non-volatile organics is crucial. Currently, only synchrotron radiation based facilities have the potential to analyze traces of non – volatile organic surface contamination. This is with respect to qualification and quantification.

Process Equipment—Defect reduction in process equipment remains paramount to achieving defect density goals. Solutions and technology developments are expected to provide major enhancement capabilities in the next 15 years and continue to enable cost-effective high volume manufacturing for critical device dimensions for advanced semiconductor manufacturing. Vertical faults, particularly as they apply to the gate stack, metallic, and other non-visual contaminants, and parametric sensitivities need to be understood. New cleaning chemistries, *in situ* chamber monitoring, materials development, and other techniques including improved techniques of parts cleaning can help

maintain chamber cleanliness run-to-run and dramatically reduce the frequency of chamber wet cleans. These developments will also act to increase equipment utilization. Backside wafer contamination control must drive both measurement technology and fundamental changes in equipment. Metal/particle cross contamination from backside to next wafer front-side, hot spots/depth of focus in lithography, and punch through on electrostatic chucks are all examples of issues that must be addressed in future tools. Particle avoidance techniques (o-ring material selection, gas flow/temperature management, wafer chuck optimization) will continue to play a key role in meeting defect densities. It is believed that a more fundamental understanding of reactor contamination formation, transport, and deposition will be required to enhance current equipment and process design and aid in the placement and interpretation of data from *in situ* sensors. These fundamental physical, chemical, and plasma reactor contamination models must be employed. *In situ* process control will become increasingly important to reduce process-induced defects and to minimize requirements for post-measurements. Intelligent process control at a tool requires a fundamental understanding of how parameters impact device performance. Open tool control systems that allow both users and equipment suppliers to easily integrate new sensor and new control software will be necessary to enable intelligent process control.

Process critical materials—studies into device impact are necessary to validate any need for increased purities. System concerns such as corrosion or haze potential may lead process concerns in seeking higher purities.

In order to accelerate yield enhancement for processes that incorporate new materials, it is very desirable that development studies include purity data as much as is practical. Studies of new materials (*e.g.*, for gate dielectrics) are initially concerned with basic process performance, and later with integration issues. During those stages of development contamination is a relatively minor concern. However, if no information is collected, later yield enhancement efforts proceed with inadequate technical basis. Collecting and reporting both environmental and material contamination data whenever practical will lead to long-term benefits.

UPW— Effect of UPW quality to wafer defects for most advanced device geometries is unknown. Particles (including colloidal silica) are considered to be high risk. Potential solution for the particle control is due to reduction of the particle challenge in the final filters and application of the POU filtration, providing additional layer of protection. Use of SEMI C079 and SEMI C093 guides are recommended for the particle challenge reduction. Proactive colloidal silica control using frequent regeneration of the ion exchange resin is also recommended.

Although target levels for hydrogen peroxide have not been defined, system performance optimization is encouraged to reduce H_2O_2 presence in UPW.

Chemicals information pending…

Surface environment control—As the list of ambient contaminants to be controlled broadens so must measurement capabilities. Affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly necessary. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate and pre-contact clean and salicidation are cited as processes to first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving. Wet clean and etch, tool environments have also transitioned that may need to single-wafer and use of closed processing systems are becoming more prevalent for corrosion sensitive layersbecome inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low outgassing of volatile contaminants, and non-absorbing materials development are a key to effective wafer isolation deployment.

7. SUMMARY

IRDS Yield Enhancement Chapter continues depelopment of the previous ITRS YE effort. Current advanced and new generations of semiconductor manufacturing technologies poses new challenges for defect characterization and control. Metrology has become a substantial challenge at all levels from critical facility system, tool environments, to critical surface analysis. New definitions of defects are needed for 3-D and heterogeneous integration.

Tighter environment contamination control is needed for more complex devices. UPW, Gases, AMC, and Chemicals subteam continue using previous ITRS methodologies. At the same time better standardization is needed to ensure quality assurance throughout supply chance under conditions of metrology limitations.

In addition to tradional focus teams of former ITRS, the IRDS YE forum also includes considerations of critical components that may contribute contamination into the wafer environment and as a result impact the process yield as well as new focus activities around Mems and 3D challenges.

Unless IRDS capabilities teams may help with definitions of the defectivity requirements, the YE will also onclude development in this area as part of the Critical Surface focus team.

8. REFERENCES

www.itrs2.net

10.0 ACKNOWLEDGMENTS

This white paper is the result of the communications and input of large group of industry experts involved in YE focus teams. It also includes information from 2015 ITRS documents.