INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

2016 EDITION

METROLOGY WHITE PAPER

METROLOGY

1. CHARTER

Identify emerging measurement challenges from devices, systems, and integration in the semiconductor industry and describe research and development pathways for meeting them. This includes, but not limited to, measurement needs for extending CMOS, accelerating Beyond CMOS technologies, novel communication devices, sensors and transducers, materials characterization and structure function relationships. This includes metrology required in research and development and for providing process control in manufacturing, yield, and failure analysis.

2. MISSION

Identify metrology requirements, materials characterization and research needed to address emerging measurement challenges for the next 15 years.

3. SCOPE

The scope include metrology for critical dimension related parameters CD, LER, LWR and overlay; 3D Nanometrology (physical and chemical parameters); film thickness, reference materials, materials and contamination analysis; metrology for emerging research materials and devices; metrology requirements for system integration, emerging computing, communication architectures and technologies.

4. CROSS TEAM INTERACTIONS

The Metrology working group will align with international focus teams (IFT) within IRDS such as Beyond CMOS (ERD), Heterogeneous Microsystems, Outside System Connectivity, More Moore, Lithography, PIDS, FEP, Interconnect, Yield, and ESH on capabilities required to meet future metrology needs. Due to the complexity and scope of IC metrology, we will also interact and align with other measurement and characterization related roadmap efforts and organizations as needed.

Cross team interactions areas include, but are not limited to:

ERM: Metrology will align with IRDS ERM IFT to identify measurement solutions needed to characterize and understand the composition, properties and structure of emerging materials. These include but are not limited to evaluating critical material and dimensional properties of directed self-assembly (DSA) lithograpghy; non-destructive methods for imaging and/or characterizing nanoscale structures, embedded nanostructures, materials and interfaces defects; and interconnect materials metrology among others.

Beyond CMOS (ERD): Metrology will align with ERD IFT to identify solutions to emerging research devices metrology issues. Some areas that have been identified include 3D atoms positions, contact resistance, and spin and magnetic properties at nanoscale, among others.

Outside System Connectivity: Metrology will align with IRDS Outside system connectivity (OSC) on capabilities required to develop, design, manufacture and test future RF, wireless, and photonic communication capabilities. Topics include precise wavelength measurement methods, testing coupling efficiency, minimally invasive metrology, and measurement of complex material layers for bipolar/CMOS (RF devices). For photonic interconnects, metrology is needed to measure sub micrometer scale variations of optical properties, and to detect local sources of losses in development and in manufacturing and assembly process.

Factory Integration (FI): Metrology will work and align with IRDS Factory Integration to identify requirements needed to fully integrate metrology systems within the factory. These include but are not limited to leveraging metrology process control knowledge, big data, virtual metrology, and capabilities such as smart sensors to improve overall factory performance. Other areas include defect reduction and yield improvement; and leveraging metrology nanomaterials characterization techniques for ESH purposes.

More Moore: Metrology will align with all the IFTs within More Moore (Lithography, PIDS, FEP, Interconnect) to identify metrology requirements to support current and next generation IC manufacturing technologies. Some examples include*: (Lithography):* Metrology to support new process technologies for 3D structures such as FinFET & MuGFET; directed self assembly; and other device structures such as vertical gate all around (VGAA), Nanowire, Lateral gate all around (LGAA), and monolithic 3D features. (*FEP*) Measurement of complex material stacks and interfacial properties including physical and electrical properties. (*Interconnect*) Metrology for layered architecture for 3D stack.

Heterogeneous Microsystem: Metrology will align with IRDS Heterogeneous Microsystem as needed to identify measurement capabilities required for MEMS and Sensors critical device performance characterization.

5. STAKEHOLDERS

Stakeholders for the Metrology IFT include IC design & manufacturing companies, metrology equipment manufacturers and vendors, semiconductor foundries, metrology and materials characterization researchers, and standards organizations.

6. TECHNOLOGY STATUS, NEW REQUIREMENTS AND POTENTIAL SOLUTIONS

6.1. TECHNOLOGY STATUS AND UPDATE

Broadly speaking, scaling is expected to reach its physical limits within the next few IC generations. As such, feature size reduction will no longer be the main technology driver for the industry. Applications such as Cloud Computing, Mobile Communication and Information, Smart Automotive/Vehicular Technologies, Green Energy Technologies, and Medical and Health Technologies among others are expected to be the key drivers. Going forward, these new system-level drivers will greatly reshape semiconductor technology requirements and road mapping activities.[1] The new drivers will likely have implications for metrology with respect to the pace, timing, and types of new technologies adopted. In addition, the metrology needs of the high performance computing (HPC) systems required to meet the challenges of these new drivers would require investments in foundational measurement science.[2]

6.2. NEW REQUIREMENTS & DIFFICULT CHALLENGES

Device and integrated circuit technology has rapidly evolved toward the use of complex 3D structures fabricated using new materials and processes with ever decreasing dimensions. The 3D nanoscale nature of these structures provides considerable challenges for all areas of metrology. Several examples of new process technology help describe the new challenges facing metrology. Research into new patterning processes covers the use of directed self-assembly of block copolymers, extreme ultra violet (EUV) lithography, and 3X and 4X multiple patterning.

All of these methods result in different challenges for measurement of critical dimensions (CD), overlay, and defectivity. FinFET transistors are now the dominant microprocessor device architecture, and the challenges associated with 3D nature of all measurements are amplified by shrinking dimensions. Adding to the challenges facing Front End Processes (FEP) metrology are control of the fabrication processes for memory structures which are among the most complex 3D device structures. On-chip and off-chip interconnect materials continue to evolve and interconnect metrology challenges continues to include process control for 3D interconnect. For Beyond CMOS R&D, many areas of graphene metrology have advanced but putting them into volume manufacturing will require challenging R&D. The need for understanding large area graphene uniformity is driving both physical and electrical metrology. In addition, new characterization techniques are required for a whole range of emerging materials. New metrology techniques are needed to adequately characterize device structures such as vertical gate all around (VGAA), Nanowire, Lateral gate all around (LGAA), and monolithic 3D features. Hence, in addition to small sizes engendered by years of aggressive scaling, feature shape and integration complexities would require a new metrology landscape.

Many short-term metrology challenges listed below will continue beyond the 7 nm ½ pitch[3]. Metrology needs after 2023 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table 1 presents some major challenges for metrology.

TABLE 1 METROLOGY DIFFICULT CHALLENGES

Difficult Challenges (2016-2023)	*Summary of Issues*
Factory level and companywide metrology integration for real-time *in situ*, integrated, and inline metrology tools.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Reduction of scrap, increased product quality and cycle time. Standards and best known methods for handling big data. Virtual Metrology (with standards) to support emerging sensor and smart technology capabilities.
Starting materials metrology and associated manufacturing metrology.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI, III-V, GeOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools.
Control of new process technology and 3D Interconnect	The use of complicated 3D structures such as FinFET & MuGFET places increased emphasis on the near term need for in-line metrology for dimensional, compositional, and doping measurements. The materials properties of block co-polymers for DSA result in new challenges for lithography metrology. The increased use of multi-patterning techniques introduces the need to independently solve a large set of metrics to fully characterize a multi-patterning process. 3D Interconnect comprises a number of different approaches. New process control needs are not yet established. For example, 3D (critical dimension (CD) and depth) measurements will be required for trench structures including capacitors, devices, and contacts.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI, III-V, GeOI, and other substrates, or for measurement of barrier layers. Metal gate work function characterization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced, especially in the scribe lines. Measurements on test structures located in scribe lines may not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges (2024- 2031)	

Nondestructive, production worthy wafer and mask-level metrology for CD measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for overall feature profile. Metrology tool imaging resolution must improve to be able to discern 3D information. It is important to have both imaging and scattering techniques available for any given process control situation. Focus, exposure, and etch bias control will require better precision and 3D capability. Potential metrology solutions have to be able to characterize complex shape structures with sub-atomic resolution. These include vertical gate all around (VGAA), Nanowire, Lateral gate all around (LGAA), and monolithic 3D features
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as devices shrink. Sampling plan optimization is key to solving these issues.
Statistical limits of sub-10 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, surface, sidewall and edge roughness of very small structures. Complementary, and hybrid metrology combined with state of the art statistical analyses would be required to reduce the measurement uncertainty.
Structural and elemental analysis at device dimensions and measurements for *beyond CMOS, and emerging materials and devices.*	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.
Directed Self Assembly (DSA)	Key measurands such as size, location, and alignment need to be better defined. Some of the measurands are also material and system dependent. Many of the materials are similar enough that identifying a property with the required contrast may be difficult. A key question seems to be if we can detect low densities of surface and buried defects.
Defects	Defect detected capabilities over a wide range of technology areas. These include, but are not limited to: Trace contamination measurements on interconnects; Sidewall Damage – Particles on the sidewall, thickness of the damage layer; Particle detection below < 30 nm and its chemical composition (3 Dimensions at Planar Devices, and on 3D Devices); Embedded defects – voids; Defect in DSA – buried defects are not easily characterized using standard detection strategies., 3D information for particle detection.

6.3 POTENTIAL SOLUTIONS

Table 2 summarizes potential solutions that cut across different areas, with some examples. The information in Table 2 cover two broad categories: (1) Combining different measurement technologies in ways that increase the number and/or enhance the usefulness of specific parameters. (2) Increased range and resolution for available measurement technologies. These include not only possible new technologies, but also improving or adapting existing technologies to other uses.

Table 2 METROLOGY POTENTIAL SOLUTIONS

Potential Solutions	Examples
Improved Instrument Resolution	Better resolution for current technologies such as CD-SEM, CD-AFM, and optical CD among others. Increased range for high resolution instruments and vice –versa (This will greatly increase the ability to measure features such as TSVs) • *Introduction of aberration-corrected low energy SEM column* • *Utilization of high energy SEM* • *Enhanced CD-AFM tip technology* • *Reduced spot size and uniform intensity for optical instruments* • *Use of multi-column electron beam instrument for defect inspection.* • *Increased use of data fusion or image stitching to increase range.*

Improved X-ray metrology for Critical Dimensions and films characterization	Higher brightness sources. • *An X-ray source with >100x brightness of conventional rotating anode sources can enable new techniques such as CD-SAXS and X-ray tomography* • *Improved throughput and increased utilization of already-mainstream X-ray metrology solutions such as HR-XRD, XRF, TXRF, XRR, XPS among others.*
3D Metrology	Non raster capabilities for scanning instruments. • *This would allow extraction of information from non-orthogonal axes.* Multi head/column for scanning instruments: • *Each head could extract different types of information (dimensional, material ...etc),* • *Faster measurements of large areas of the wafer.* Hybrid Metrology: • *Increased use of a combination of instruments to achieve the desired resolution, speed, or low levels of uncertainty needed to characterize different aspects of a feature.*
Plasmonic Assisted Optical Focusing	Plasmonic structures are able to focus radiation to sub wavelength size. This may enable measurement of optical properties and losses in small local regions

7. SUMMARY

The Metrology chapter of the IRDS focuses on identifying emerging measurement challenges from devices, systems, and integration in the semiconductor industry and describe research and development pathways for meeting them. The chapter outlines and describes technology requirements for the next 15 years. This include difficult challenges, possible solutions, methods and tools. The overall scope includes, but not limited to, measurement needs for extending CMOS, accelerating Beyond CMOS technologies, RF and photonic communication devices and technologies, materials characterization and structure function relationships, as well as provide the measurement capability necessary for cost-effective manufacturing.

8. REFERENCES

[1]J-A. Carballo, W-T J.Chan, P.A. Gargini, A.B. Kahng, S.Nath , ITRS 2.0: Toward a Re-Framing of the Semiconductor Technology Roadmap *Proc. 32nd IEEE International Conf. on Computer Design (ICCD)*, pp139-146 (2014)

[2]Executive Order (EO) 13702, "CREATING A NATIONAL STRATEGIC COMPUTING INITIATIVE"
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[3]B.Bunday, T.A. Germer,V.Vartanian, A. Cordes, A. Cepler, and C. Settens, Gaps analysis for CD metrology beyond the 22nm node, *Proc. SPIE* 8681, 86813B (2013)