INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

2016 EDITION

BEYOND CMOS (EMERGING RESEARCH DEVICES, ERD)

WHITE PAPER

BEYOND CMOS (EMERGING RESEARCH DEVICES)

1. CHARTER

The Beyond CMOS (BC) chapter surveys emerging research devices for information processing and storage applications, identifies promising device technologies, maps a variety of device options with emerging architectures, and defines research needs from devices to architectures.

The chapter evolves from the Emerging Research Devices (ERD) chapter of ITRS. It adopts the same methodologies from the ERD chapter: selection, categorization, and evaluation of emerging device options. However, traditional CMOS-based evaluation criteria are not sufficient for the evaluation of novel computing paradigms. New device benchmarking methods and criteria need to be developed in the Beyond CMOS chapter.

2. MISSION

Identify beyond-CMOS devices for information processing and storage to enable novel computing paradigms beyond the capabilities of conventional CMOS technologies and architectures.

3. SCOPE

The Beyond CMOS chapter will identify research opportunities for beyond-CMOS devices to enable high-performance computing, energy-efficient computing, non-von-Neumann architectures, and alternative computing paradigams (e.g., cognitive computing, quantum computing, *etc*.). Included are novel devices for information processing, sensing, and communication, novel memory and storage devices, and devices to enable functional diversification ("more than Moore"). The chapter will assess devices for different applications with recommendations of the most promising candidates and map emerging devices with novel architectures to identify research opportunities for co-optimization.

4. CROSS TEAM INTERACTIONS

The beyond CMOS chapter will closely interact with other IRDS chapters, as illustrated in Figure 1. "System design", "Outside system connectivity", and "Architecture" defines device requirements that the BC chapter will refer to, and BC chapter provides inputs on device opportunities. These device options target transfer to "More Moore" chapter when they are sufficiently mature. "Yield" is one of the factors to measure the maturity of BC devices.

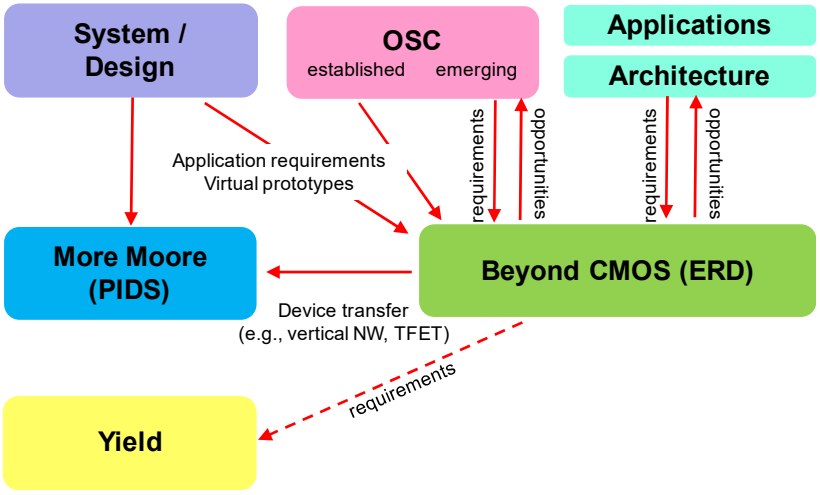

Figure 1. Illustration of cross-team interactions for Beyond CMOS (BC).

5. STAKEHOLDERS

The BC chapter is intended to provide an objective, informative resources for the nanoelectronics communities pursuing: (1) research, (2) tool development, (3) funding support, and (4) investment. The stakeholders for the BC chapter include universities, research institutes, industrial research laboratories, tool suppliers, research funding agencies, and the semiconductor industry. The potential and maturity of each emerging research device and architecture technology are reviewed and assessed to identify the most important scientific and technological challenges that must be overcome for a candidate device or architecture to become a viable approach.

6. TECHNOLOGY STATUS, NEW REQUREMENTS AND POTENTIAL SOLUTIONS

The continued scaling of CMOS has driven information processing technologies into a broad spectrum of applications enabled by the performance gains and/or complexity realized by scaling. Because dimensional scaling of CMOS will eventually approach fundamental limits, new information processing devices and architectures have to be explored for existing and new applications to sustain performance gain beyond CMOS scaling. This has driven interest in new devices for information process and memory, new technologies for heterogeneous integration of multiple functions ("More than Moore"), and new paradigms of computing architectures.

6.1. TECHNOLOGY STATUS AND UPDATE

The BC chapter will address four research directions: (1) emerging memory devices, (2) emerging information processing or logic devices, (3) more-than-Moore device technologies, (4) interface between emerging devices and novel computing paradigms and architectures. The Emerging Research Devices (ERD) chapter of ITRS has surveyed, assessed, and categorized viable emerging devices for memory, information processing, and more-than-Moore applications up to 2015 [1]. Figure 2 and 3 summarize emerging memory and logic devices as reported in the 2015 ERD chapter. A focus of the BC chapter will be tracking of the status and progress of the devices covered as well as updating the taxonomy of devices. However, the assessment criteria for BC chapter needs to be broadened from the conventional focus on performance-power-area (PPA) metrics to more functional metrics mandated by new computing paradigms. For example, systems with cognitive and learning capabilities need new performance metrics to measure efficiency and accuracy of the learning process. A challenge is to

translate these system or architecture functional metrics to quantitative device parameters for technology assessment.

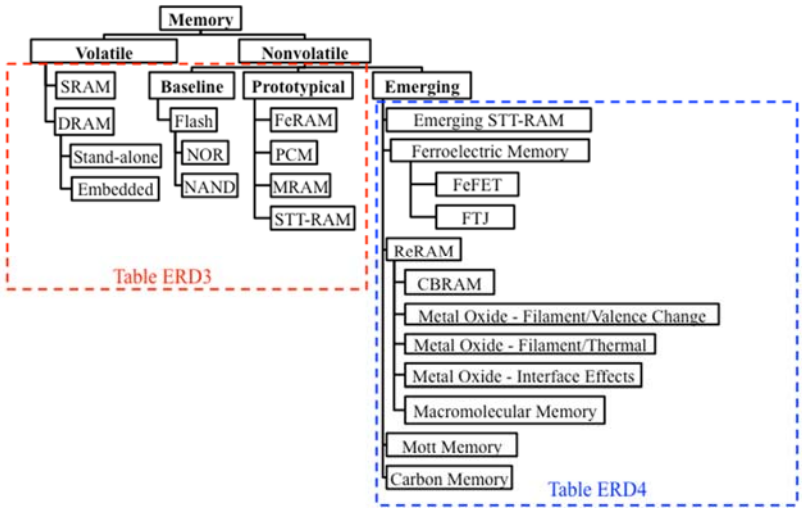

Figure 2. Taxonomy of emerging memory devices in 2015 ERD chapter.

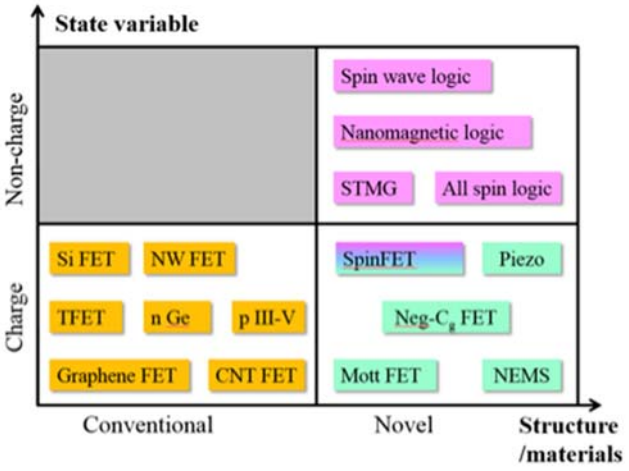

Figure 3. Taxonomy of options for emerging logic devices in 2015 ERD chapter. The devices examined here are differentiated according to (1) whether the structure and materials are conventional or novel, and (2) whether the information carrier is electron charge or some non-charge entity. Since a conventional FET structure and material imply a charge-based device, this classification results in a three-part taxonomy.

The 2015 ERD chapter address three groups of devices for more-than-Moore: (1) emerging devices for hardware security, (2) emerging devices with learning capabilities, and (3) emerging devices for low-power sensor nodes. Heterogeneous integration and functional diversification based on ultimately scaled CMOS is an important research direction. The BC chapter will continue broadening the scope of more-than-Moore devices to address research needs in this area.

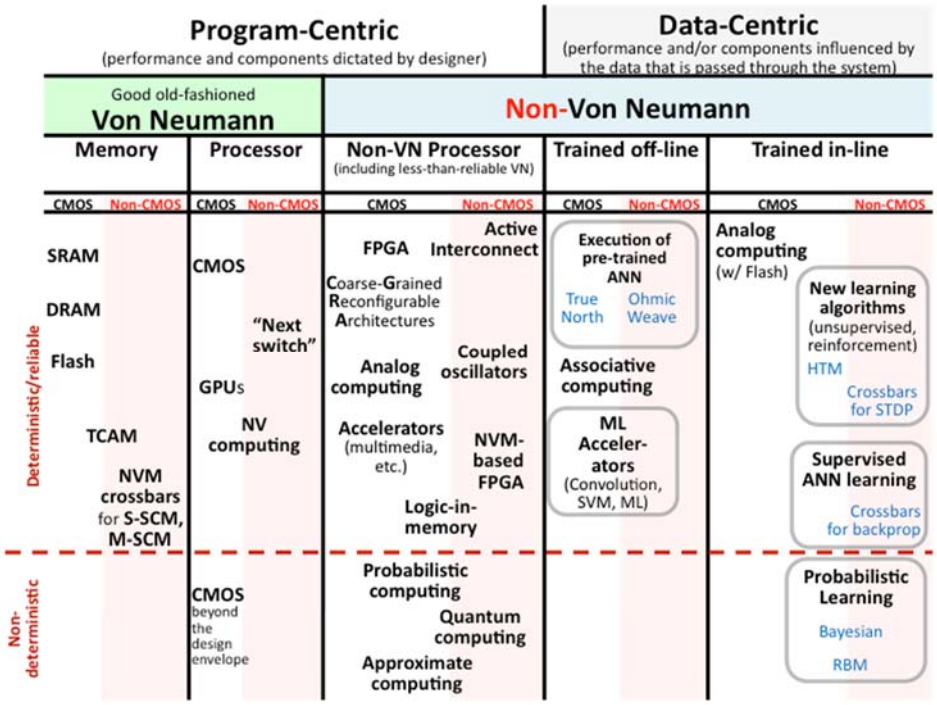

Figure 4. Categories of emerging computing architectures in 2015 ERD chapter.

The ERD chapter also addressed research needs in architectures in the Emerging Research Architectures (ERA) section. The 2015 ERA section covers storage class memory architectures and emerging computing architectures. The emerging computing architectures are divided into program-centric architectures and data-centric architectures, each with sub-categories of architectural concepts, as shown in Figure 4. An important focus of the BC chapter will be to map the emerging devices to these novel architectures to identify both device options for these novel architectures and the technology requirements on emerging devices.

6.2. NEW REQUIREMENTS & DIFFICULT CHALLENGES

Table 1 summarizes some of the difficult challenges for beyond CMOS devices and key issues and opportunities.

Table 1 Difficult challenges of beyond CMOS devices

Difficult Challenges – 2020– 2030	*Summary of Issues and opportunities*
Scale volatile and nonvolatile memory technologies to replace SRAM and FLASH in appropriate applications.	SRAM and FLASH scaling in 2D will reach definite limits, which has driven the needs for new memory technologies to replace SRAM and FLASH memories. Identify the most promising technical approaches to obtain electrically accessible, high-speed, high-density, low-power, (preferably) embeddable volatile and nonvolatile memories. The desired material and device properties must be maintained through and after high temperature and corrosive chemical processing. Reliability issues should be identified and addressed early in the technology development.
Extend ultimately scaled CMOS as a platform technology into new domains of application.	Develop materials and devices to extend CMOS scaling, increase the saturation velocity, reduce V_{dd} and power dissipation, while minimizing leakage current. Control the variability of critical dimensions and statistical distributions (e.g., gate length, channel thickness, S/D doping concentrations, etc.) Reliability issues should be identified and addressed early in this development. Discover and reduce to practice new device technologies and primitive-level architecture to provide special purpose optimized functional cores (e.g., accelerator functions) heterogeneously integrable with CMOS.
Continue functional scaling of information processing technology substantially beyond that attainable by ultimately scaled CMOS. Enable new computing paradigms by device technology breakthroughs.	Invent and reduce to practice a new information processing technology eventually to replace CMOS as the performance driver. Ensure that a new information processing technology has compatible memory technologies and interconnect solutions. A new information processing technology must be compatible with a system architecture that can fully utilize the new device. Non-binary data representations, non-Boolean logic, or non von Neumann architectures may be required to employ a new device for information processing, which will drive the need for new system architectures. Map desirable device properties to the design and architectural requirements of new computing paradigms, new algorithms, and new computing models. Develop methodologies for the co-optimization of devices and architectures for different applications. Bridge the gap that exists between material behaviors and device functions. Reliability issues should be identified and addressed early in the technology development.
Develop materials and devices to enable more-than-Moore solutions.	More than Moore" (MtM), or functional diversification, adds value to devices by incorporating functionalities that do not necessarily scale according to "Moore's Law." Heterogeneous integration of digital *and* non-digital functionalities into compact systems that will be the key driver for a wide variety of application fields, such as communication, automotive, environmental control, healthcare, security, and entertainment. Accommodate the heterogeneous integration of dissimilar materials, devices, and circuit components.

6.3 POTENTIAL SOLUTIONS

Beyond CMOS devices will continue to be categorized as: (1) memory devices, (2) information process (logic) devices, (3) more-than-Moore devices. However, these emerging devices may provide more complex functions than simple data storage or arithmatic computing in the context of novel computing architectures and paradigms. The same devices may provide both computing and storage functions (e.g., nonvolatile logic) or combine digital and analog functions (e.g., spin logic). The analog feature of some memory components is utilized to implement synaptic functions in neuromorphic computing (e.g., RRAM). Going beyond conventional storage and logic applications, these emerging devices have demonstrated promising potential for novel computing paradigms to enable new functions and to improve system efficiency. To fully utilize beyond-CMOS devices in these new computing paradigms, it is important to co-optimize devices and architectures.

The BC chapter will track a new set of emerging devices starting from candidates in 2015 ERD chapter, filtering out irrelevant and outdated devices, and adding new promising devices. New assessment parameters, criteria and methodologies compatible with IRDS mission will be defined. Methods to map emerging devices with architectures and to translate architectural metrics to device parameters will be developed.

The chapter will broaden the range of beyond CMOS devices. For example, devices for superconducting electronics (SCE), e.g., SFQ (Single Flux Quantum) and AQFP (Adiabatic Quantum Flux Parametrons), are suitable for applications where advantages such as speed, power, or energy efficiency outweigh disadvantages such as cryogenic temperature operation, low maturity, and lower density. Interface between cryogenic SCE and room temperature electronics presents a challenge and also an opportunity because SCE is a credible option when computing must be done in cryogenic environments, for example cooled sensors or terrestrial quantum information processing. The challenge is that existing solutions do not scale to high data rates. SCE also requires compatible memory solutions.

7. SUMMARY

The beyond-CMOS chapter inherits from the Emerging Research Devices (ERD) chapter of ITRS key methodologies and is built upon the latest ERD technology entries. The chapter will survey, assess, and catalog viable device options for both traditional and novel computing architectures. The chapter will benchmark these device options with broadened criteria and new methodology to address technology requirements of novel computing architectures and paradigms. The chapter will provide key reference to identify research needs from devices to architectures, for developing computing solutions beyond the capabilities of conventional CMOS technologies.

8. REFERENCES

[1] Emerging Research Devices, the Intentional Technology Roadmap of Semiconductors (ITRS), 2015.

9. ACKNOWLEDGMENTS

An Chen, Matthew Marinella, Shamik Das, Paul Franzon, Geoffrey Burr, Erik Debenedictis, Douglas Holmes, Sapan Agarwal